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CUSTOMER APPROVAL SHEET

Company

Name

MODEL A035QN05 V0

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APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.4)

APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.4)

APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.4)

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Product Specification
3.5" COLOR TFT-LCD MODULE

Model Name :	A035QN05 V0
Planned Lifetime:	From ~~F~~ 2010/08 To 2012/09
Phase-out Control:	From 2012/03 To 2012/09
EOL Schedule:	2012/09

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	20100727		1st release
0.1	20101101	27	Update Chromaticity
0.2	20101102	8	IVDD
0.3	20110211	Cover page	Update Planned Lifetime
		32	Update the condition of low temperature in operation mode.
0.4	20110216	6	modify 1. Dot pitch unit :（mm）

Contents

A. General Information

NO.	Item	Specification	Remark
1	Display resolution（dot）	320 RGB (H)×240(V)	
2	Active area（mm）	70.32x52.74	
3	Screen size（inch）	3.5(Diagonal)	
4	Dot pitch（mm）	0.073(H)×0.219(V)	
5	Color configuration	R, G, B strip	
6	Overall dimension（mm）	76.90(H)x63.90(V)x4.07(T)	Note 1
7	Weight（g）	40	
8	Panel surface treatment	Hard Coating	

Note 1: Refer to F. Outline Dimension

B. Electrical Specifications

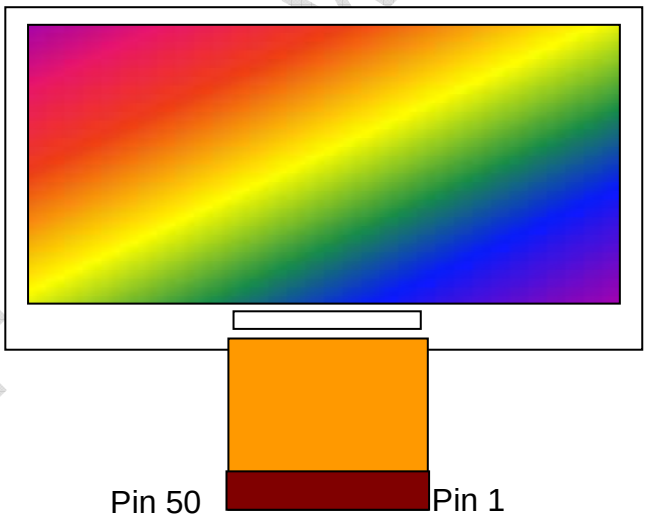
1. Pin Assignment

No.	Pin Name	I/O	Description	Remarks
1	VLED+	P	Backlight LED anode	
2	VLED-	P	Backlight LED cathode	
3	X1	I/O	Touch panel right electrode (R)	
4	Y2	I/O	Touch panel bottom electrode (B)	
5	X2	I/O	Touch panel left electrode (L)	
6	Y1	I/O	Touch panel top electrode (U)	
7	VCOM	I	Common electrode driving voltage	
8	GND	G	Power Grounding	
9	DOTCLK	I	Data clock Input	
10	GND	G	Power Grounding	
11	VSYNC	I	Vertical sync input	
12	HSYNC	I	Horizontal sync input	
13	DATA0	I	Serial data	
14	DATA 1	I	Serial data	
15	DATA 2	I	Serial data	
16	DATA 3	I	Serial data	
17	DATA 4	I	Serial data	
18	DATA 5	I	Serial data	
19	DATA 6	I	Serial data	
20	DATA 7	I	Serial data (MSB)	
21	VDDIO	P	Voltage input pin for logic I/O	
22	RESET	I	System reset pin	Fixed to VDDIO if not used.
23	SCL	I	Clock input pin in serial mode	
24	CSB	I	Chip select pin of serial interface	
25	SDA	I	Data input pin in serial mode	
26	GND	G	Power Grounding	
27	VDD	P	Booster input voltage pin	
28	VCC	C	Stabilizing capacitor	
29	C4M	C	Pins to connect capacitance for power circuitry	
30	C4P	C	Pins to connect capacitance for power circuitry	
31	VINT3	C	Intermediate voltage for charge pump	

32	VDD	P	Booster input voltage pin	
33	VINT1	C	Intermediate voltage for charge pump	
34	C2P	C	Pins to connect capacitance for power circuitry	
35	C2M	C	Pins to connect capacitance for power circuitry	
36	C1P	C	Pins to connect capacitance for power circuitry	
37	C1M	C	Pins to connect capacitance for power circuitry	
38	GND	G	Power Grounding	
39	C3P	C	Pins to connect capacitance for power circuitry	
40	C3M	C	Pins to connect capacitance for power circuitry	
41	VINT2	C	Intermediate voltage for charge pump	
42	C5P	C	Pins to connect capacitance for power circuitry	
43	C5M	C	Pins to connect capacitance for power circuitry	
44	VGH	C	Pins to connect capacitance for power circuitry	
45	C6P	C	Pins to connect capacitance for power circuitry	
46	C6M	C	Pins to connect capacitance for power circuitry	
47	VGL	C	Pins to connect capacitance for power circuitry	
48	VCOMH	C	Power setting capacitor for VCOM	
49	VCOML	C	Power setting capacitor for VCOM	
50	VCOM	I	Common electrode driving voltage	

I：Input, O：Output, C：Capacitor, P：Power, D：Dummy

Note: Definition of scanning direction, Refer to figure as below：

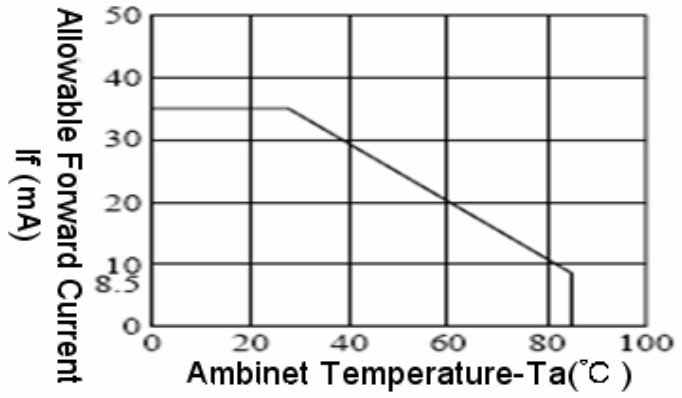


2.Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VCI / VDDIO	-0.3	4	V	
LED Reverse Voltage	Vr		5	V	One LED
LED Forward Current	If		22	mA	One LED, Note 2

Note 1.If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

Note 2. If LED current exceeds the limit curve, the lifetime will drop dramatically.



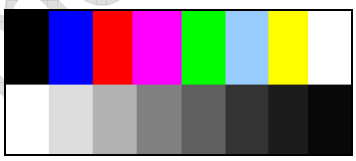
3. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

a. TFT- LCD Panel (GND=0V)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Power Supply		VDD	3.0	3.3	3.6	V	
		VDDIO	1.65	3.3	3.6	V	
Frame Frequency		f_{Frame}		60		Hz	
Dot Data Clock	8 bits serial without dummy	DCLK		27		MHz	
	8 bits serial with dummy			24.53			
Input Signal Voltage		Vi	0		0.3 x VDDIO	V	
		VI	0.7 x VDDIO		VDDIO	V	
Current Consumption		IVDD		15		mA	

Note 1: Frame rate is 60Hz. Test pattern is the following picture.

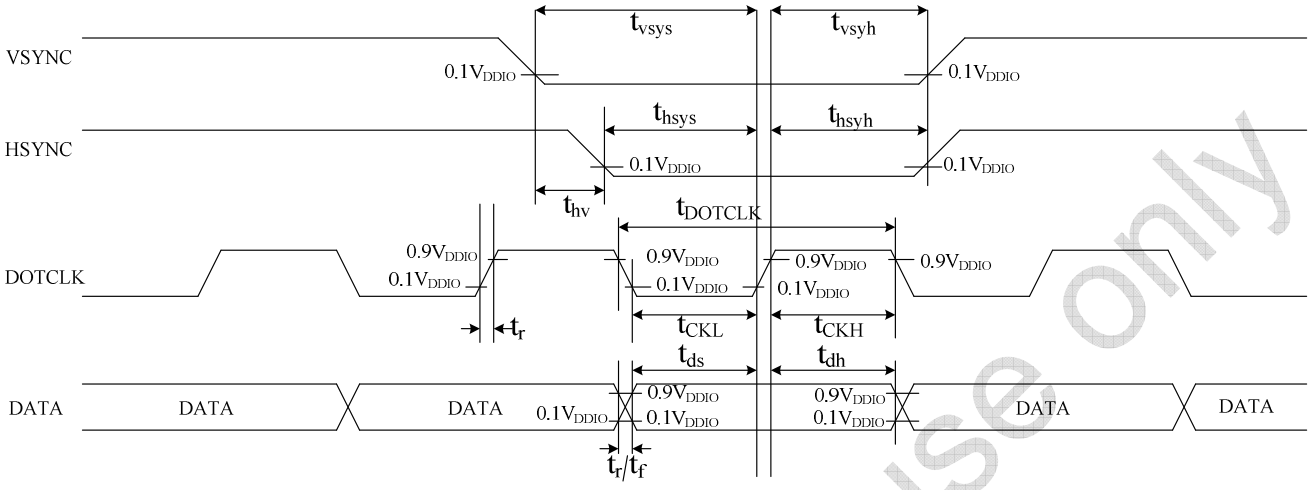


b. Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.[Note1]	Unit	Remark
Backlight Current			20	22	mA	
Backlight voltage	V_L		(19.2)	21	V	

4. AC Timing

a. Display General Information



Characteristics	Symbol	Target Min	Target Typ	Target Max	Units
Vertical Sync. Setup Time	t_{vsys}	12	-	-	nSec
Vertical Sync. Hold Time	t_{vsyh}	12	-	-	nSec
Horizontal Sync. Setup Time	t_{hsys}	12	-	-	nSec
Horizontal Sync. Hold Time	t_{hsyh}	12	-	-	nSec
DOTCLK Low Period	t_{CKL}	20	-	-	nSec
DOTCLK High Period	t_{CKH}	20	-	-	nSec
Data Setup Time	t_{ds}	12	-	-	nSec
Data Hold Time	t_{dh}	12	-	-	nSec
Rise/Fall Time	t_r/t_f	5	-	10	nSec

b. 8-bit Serial Interface

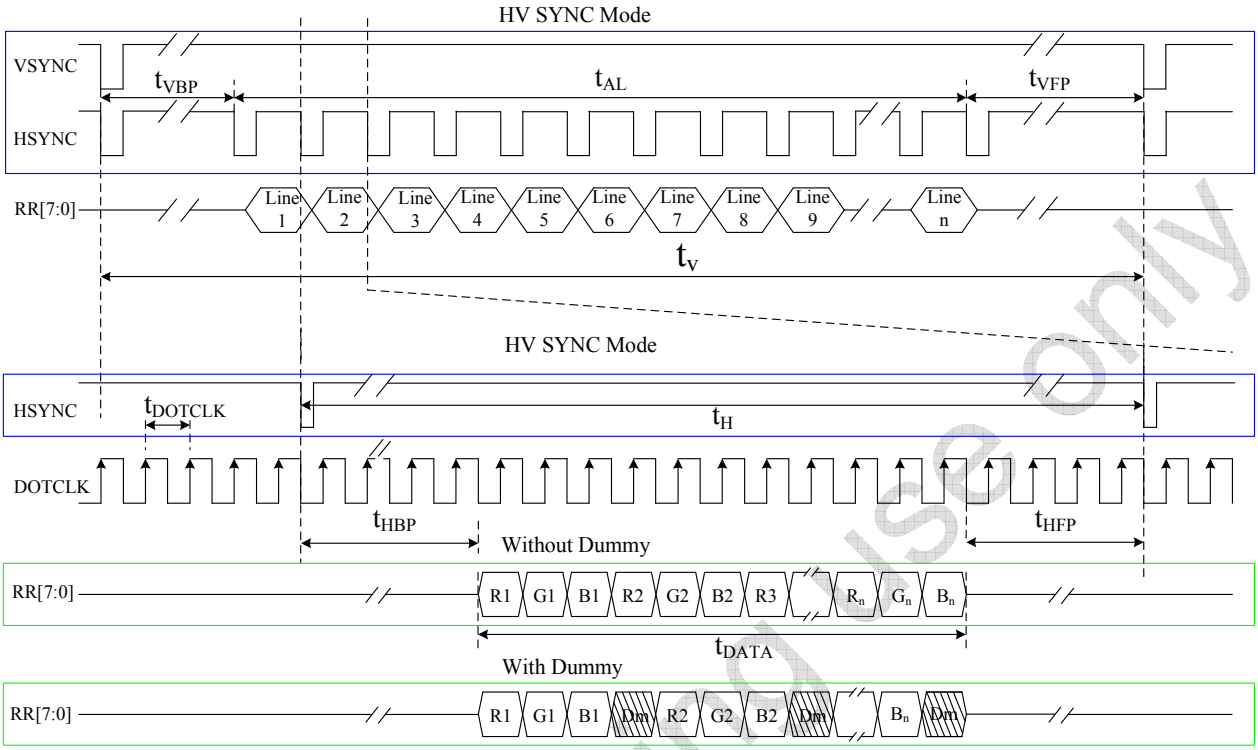


Table: 8-bit Serial Interface HV Sync. Mode without Dummy Timing Characteristics

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency			$1/t_{DOTCLK}$	13.5	27	30	MHz	
HSYNC	Period		t_H	1024	1716	1728	t_{DCLK}	
	Display period		t_{DATA}	960			t_{DCLK}	
	Back porch		t_{HBP}	50	70	255	t_{DCLK}	Note 1
	Front porch		t_{HFP}	14	686	718	t_{DCLK}	
	Pulse width		t_{HSW}	1	1	t_{HBP} - 1	t_{DCLK}	
VSYNC	Period	Odd	t_V	247.5	262.5	276.5	t_H	
		Even						
	Display period	Odd	t_{AL}	240			t_H	
		Even						
	Back porch	Odd	t_{VBP}	6	21	31	t_H	Note 2
		Even		6.5	21.5	31.5		
	Front porch	Odd	t_{VFP}	1.5	1.5	-	t_H	
		Even		1	1	-		
	Pulse width	Odd	t_{VSW}	$1t_{DCLK}$	$1t_{DCLK}$	$1t_H$		
		Even						

Note 1: The t_{HBP} time is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{VHP} time is adjustable by setting register VBLK.

***Frame rate = DCLK frequency/(tH * tV). The condition (70Hz≧Frame rate≧55Hz) must be satisfied.**

Table: 8-bit Serial Interface HV Sync. Mode with Dummy Timing Characteristics

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency			$1/t_{DotCLK}$	20.54	24.535	30	MHz	
HSYNC	Period		t_H	1354	1560	1907	t_{DCLK}	
	Display period		t_{DATA}	1280			t_{DCLK}	
	Back porch		t_{HBP}	50	241	255	t_{DCLK}	
	Front porch		t_{HFP}	24	39	372	t_{DCLK}	
	Pulse width		t_{HSW}	1	1	t_{HBP} - 1	t_{DCLK}	
VSYNC	Period	Odd	t_V	247.5	262.5	276.5	t_H	
		Even						
	Display period	Odd	t_{AL}	240			t_H	
		Even						
	Back porch	Odd	t_{VBP}	6	21	31	t_H	
		Even		6.5	21.5	31.5		
	Front porch	Odd	t_{VFP}	1.5	1.5	-	t_H	
		Even		1	1	-		
	Pulse width	Odd	t_{VSW}	1 t_{DCLK}	1 t_{DCLK}	$1t_H$		
		Even						

***Frame rate = DCLK frequency/(tH * tV). The condition (70Hz≧Frame rate≧55Hz) must be satisfied.**

c. YUV Interface

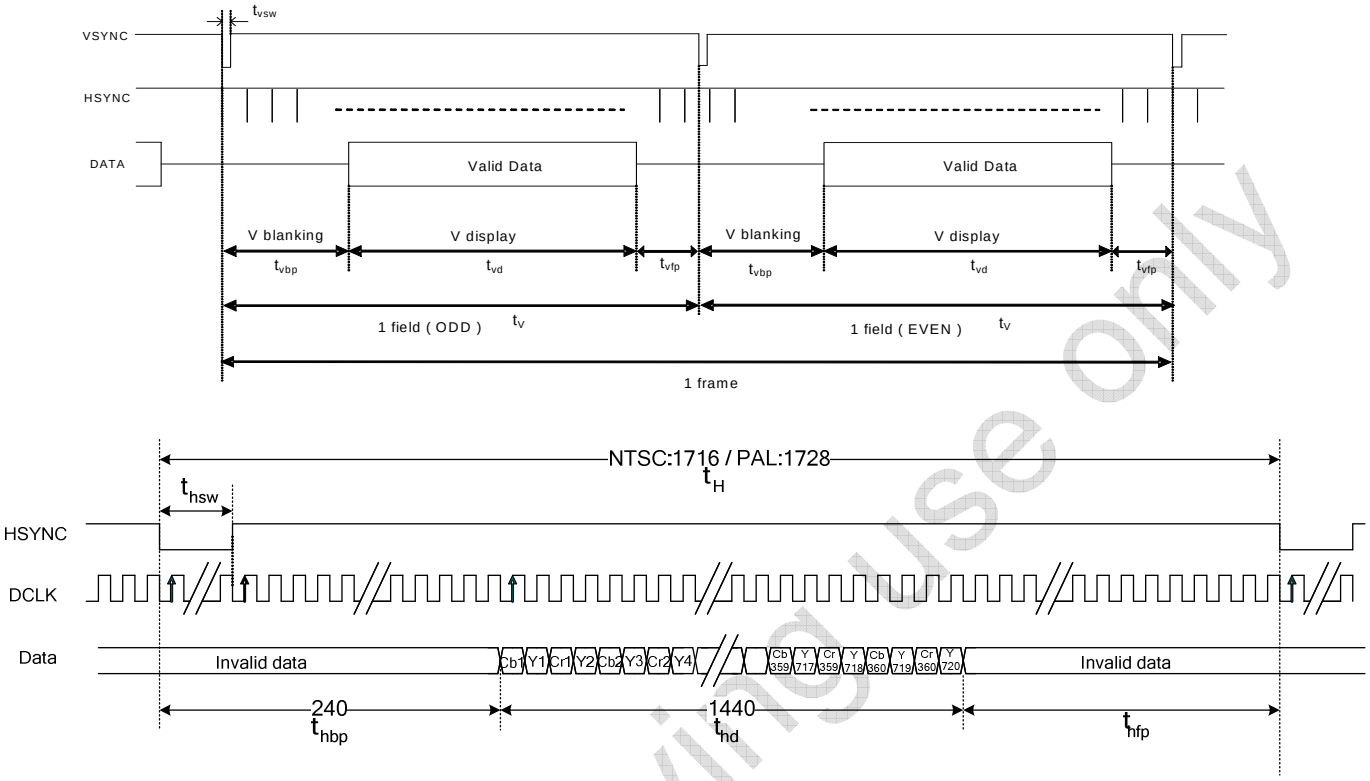


Table: YUV640 Interface HV Sync. Mode Timing Characteristics

Parameter			Symb	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency			$1/t_{DCLK}$	20.65	24.535	30	MHz	
HSYNC	Period		t_H	1362	1560	1907	t_{DCLK}	
	Display period		t_{hd}	1280			t_{DCLK}	
	Back porch		t_{hbp}	50	240	255	t_{DCLK}	
	Front porch		t_{hfp}	32	40	372	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	247.5	262.5	276.5	t_H	
		Even						
	Display period	Odd	t_{vd}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	6	21	31	t_H	
		Even		6.5	21.5	31.5		
	Front porch	Odd	t_{vfp}	1.5	1.5	-	t_H	
		Even		1	1	-		
	Pulse width	Odd	t_{vsw}	-	1	-	t_{DCLK}	
		Even						

Table: YUV720 Interface HV Sync. Mode Timing Characteristics

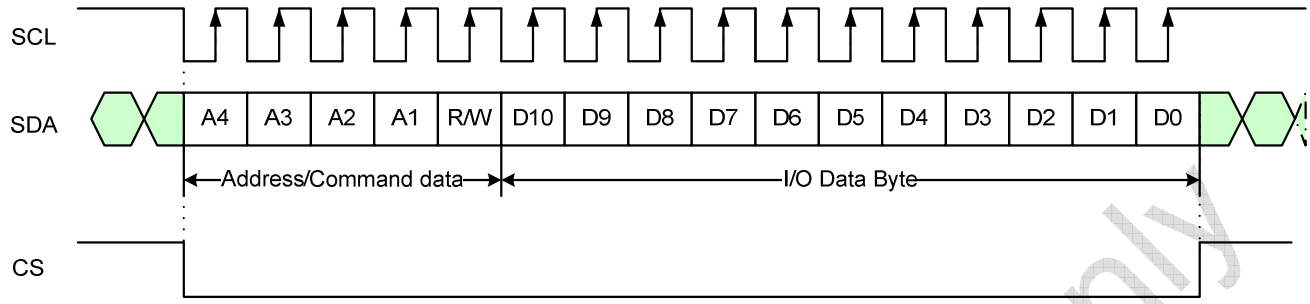
Parameter			Symb.	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency			$1/t_{DCLK}$	23	27	30	MHz	
HSYNC	Period		t_H	1524	1716	1907	t_{DCLK}	
	Display period		t_{hd}	1440			t_{DCLK}	
	Back porch		t_{hbp}	50	240	255	t_{DCLK}	
	Front porch		t_{hfp}	34	36	212	t_{DCLK}	
	Pulse width		t_{hsw}	-	1	-	t_{DCLK}	
VSYNC	Period	Odd	t_V	247.5	262.5	276.5	t_H	
		Even						
	Display period	Odd	t_{vd}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	6	21	31	t_H	
		Even		6.5	21.5	31.5		
	Front porch	Odd	t_{vfp}	1.5	1.5	-	t_H	
		Even		1	1	-		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	$1t_H$		
		Even						

Note 1: The t_{HBP} time is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

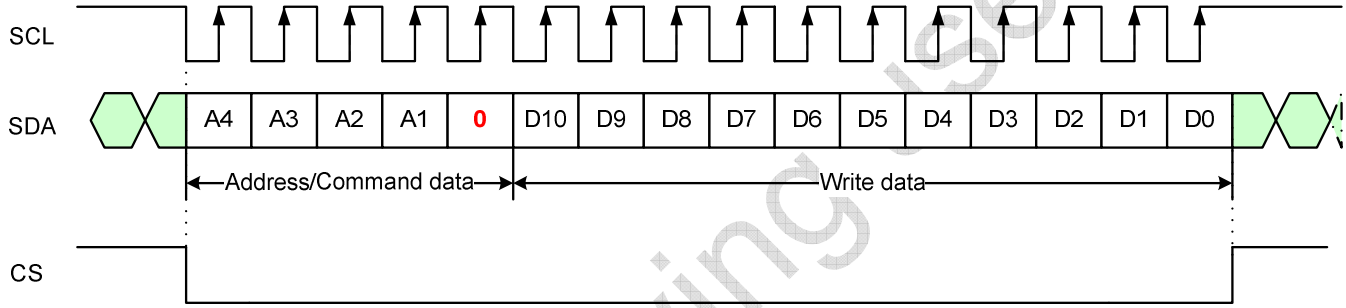
Note 2: The t_{VHP} time is adjustable by setting register VBLK.

***Frame rate = DCLK frequency/(tH * tV). The condition (70Hz≧Frame rate≧55Hz) must be satisfied.**

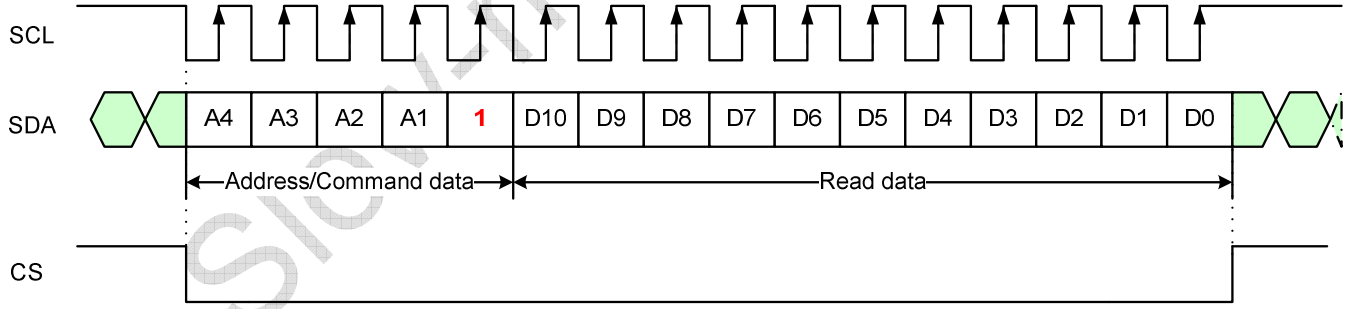
d. SPI Timing Diagram



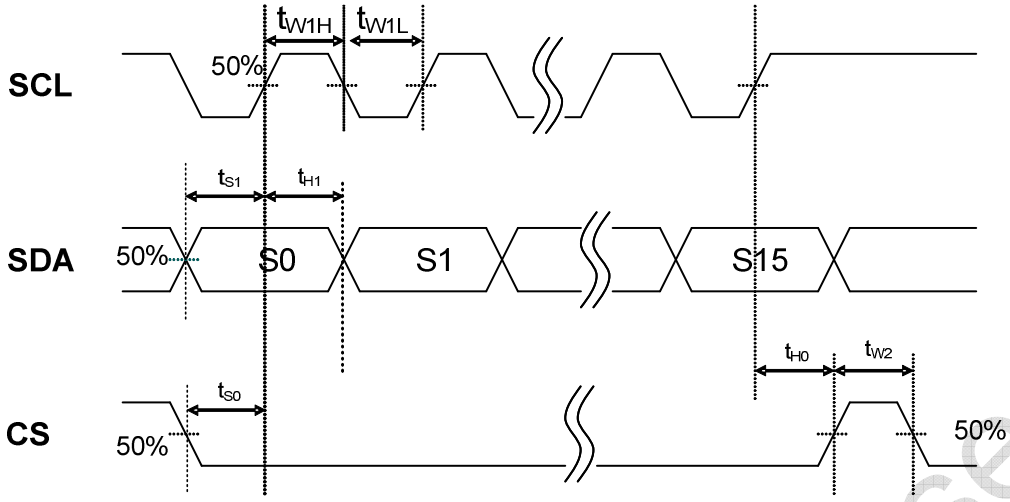
Write Mode:



Read Mode:



e. SPI Timing Specification



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	50			ns
CS input hold Time	t_{H0}	50			ns
CS pulse high width	t_{W2}	1			us
Serial data input setup Time	t_{S1}	50			ns
Serial data input hold Time	t_{H1}	50			ns
SCL pulse low width	t_{W1L}	50			ns
SCL pulse high width	t_{W1H}	50			ns

5. Command Register Settings

a. Serial setting map

- ( ) is default

No.	Register address					MSB			Register data							LSB
	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	0	0	0	0	0	UD (1)	SHL (1)	GRB (1)	STB (0)	SHDB (0)	SHCB (1)
R1	0	0	0	1	R/W	x	x	x	Y_CbCr (00)		1	1	1	SEL (000)		
R2	0	0	1	0	R/W	x	x	1	HBLK (01000110)							
R3	0	0	1	1	R/W	x	x	x	x	0	0	VBLK (10101)				
R4	0	1	0	0	R/W	x	1	1	1	1	0	0	1	0	1	AVGY
R5	0	1	0	1	R/W	x	x	x	x	x	x	x	CONTRAST (1000)			
R6	0	1	1	0	R/W	x	x	x	x	BRIGHTNESS (1000000)						
R7	0	1	1	1	R/W	x	x	x	x	OP (000)			VGL_SEL (10)		VGH_SEL (11)	
R8	1	0	0	0	R/W	x	x	x	1	VCOMH (1000001)						
R9	1	0	0	1	R/W	x	x	x	x	VCOML (1000001)						
R10	1	0	1	0	R/W	x	x	x	PWM_400K (0)	DC_F (1)	CLK_ChP_M (10)		0	1	1	0
R11	1	0	1	1	R/W	x	GMA_M (1)	GMA_V4 (011)			GMA_V1 (011)			GMA_V0 (011)		
R12	1	1	0	0	R/W	x	x	GMA_V48 (011)			GMA_V36 (011)			GMA_V16 (011)		
R13	1	1	0	1	R/W	x	x	x	x	x	GMA_V59 (011)			GMA_V55 (011)		
R14	1	1	1	0	R/W	x	x	x	x	x	GMA_V63 (011)			GMA_V62 (011)		
R15	1	1	1	1	R/W	x	x	x	x	x	VENDOR (00)		VERSION (0000)			

NOTE:

1. “X”: don’t care => Please set to ‘0’.
2. “0*”and “1*” is for engineering reserved register setting, and please follow the suggested value.
3. Please refer to our recommended register settings section for better performance.

b. Description of serial control data

I. R0 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	0	0	0	0	0	UD (1)	SHL (1)	GRB (1)	STB (0)	SHDB (0)	SHCB (1)

UD: Vertical shift direction selection

UD	Function
D5	
0	Shift from down to up, Last line = G1←G2…G239←G240 = First line
1	Shift from up to down, First line = G1→G2…G239→G240 = Last line **(Default)**

SHL: Horizontal shift direction selection

SHL	Function
D4	
0	Shift from right to left, Last data = S1←S2…S959←S960 = First data
1	Shift from left to right, First data = S1→S2…S959→S960 = Last data **(Default)**

GRB: Global reset

GRB	Function
D3	
0	Reset all registers to default value
1	Normal operation **(Default)**

STB: Standby mode setting

STB	Function
D2	
0	Standby (Display OFF); timing control, DAC, and DC/DC converter are off, and register data should be kept **(Default)**
1	Normal operation (Display ON), with power on/off sequence

SHDB: DC-DC converter shutdown setting

SHDB D1	Function
0	DC-DC converter is off. **(Default)**
1	DC-DC converter is on. DC-DC controls by STB and power on/off sequence.

SHCB: Charge Pump shutdown setting

SHCB D0	Function
0	Charge Pump converter is off.
1	Charge Pump converter is on. **(Default)** Charge Pump controls by STB and power on/off sequence.

II. R1 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R1	0	0	0	1	R/W	x	x	x	Y_CbCr (00)		1	1	1	SEL (0)		

Y_CbCr: Y & CbCr exchange position (only valid for YUV640 / YUV720)

Y_CbCr D7~D6	Function								
00	Cb1	Y1	Cr1	Y2	Cb2	Y3	Cr2	Y4	**(Default)**
01	Cr1	Y1	Cb1	Y2	Cr2	Y3	Cb2	Y4	
10	Y1	Cb1	Y2	Cr1	Y3	Cb2	Y4	Cr2	
11	Y1	Cr1	Y2	Cb1	Y3	Cr2	Y4	Cb2	

SEL: Input data timing format selection

SEL	Function
000	HV mode without dummy.**(Default)**
001	HV mode with dummy.
100	HV mode with YUV640
101	HV mode with YUV720

III. R2 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R2	**0**	**0**	**1**	**0**	**R/W**	**x**	**x**	**1**	**HBLK (01000110)**							

HBLK: Horizontal blanking setting.

HBLK(D7~D0)	HBLK	Unit	Remark
00110010	50	DCLK(*)	Without dummy
01000110 **(Default)**	70**(Default)**		
11111111	255		
00110010	50	DCLK(*)	With dummy
11110001 **(Default)**	241**(Default)**		
11111111	255		
00110010	50	DCLK(*)	YUV640 YUV720
11110000 **(Default)**	240**(Default)**		
11111111	255		

IV. R3 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R3	**0**	**0**	**1**	**1**	**R/W**	**x**	**x**	**x**	**x**	**00**		**VBLK (10101)**				

VBLK: Vertical blanking setting

VBLK(D4~D0)	VBLK	Unit
00001	1	t_H
10101	21 **(Default)**	
11111	31	

V. R4 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R4	1	0	0	0	R/W	x	1	1	1	1	0	0	1	0	1	AVGY

AVGY: Average luminance Y setting

AVGY	Function
D0	
0	Only used odd Y sample for YUV to RGB conversion
1	Used odd and even Y sample for YUV to RGB conversion **(Default)**

Note: This function is only used for YUV640, YUV720.

AVGY='0'

$R_n=1.164*(Y_{2n-1}-16) + 1.596*(C_{rn}-128)$

$G_n=1.164*(Y_{2n-1}-16) - 0.813*(C_{rn}-128) - 0.392*(C_{bn}-128)$

$B_n=1.164*(Y_{2n-1}-16) + 2.017*(C_{bn}-128)$

Where Y:16~235 C_r:16~240 C_b:16~240

AVGY='1'

$R_n=1.164*[(Y_{2n-1}+Y_{2n})/2-16] + 1.596*(C_{rn}-128)$

$G_n=1.164*[(Y_{2n-1}+Y_{2n})/2-16] - 0.813*(C_{rn}-128) - 0.392*(C_{bn}-128)$

$B_n=1.164*[(Y_{2n-1}+Y_{2n})/2-16] + 2.017*(C_{bn}-128)$

Where Y:16~235 C_r:16~240 C_b:16~240

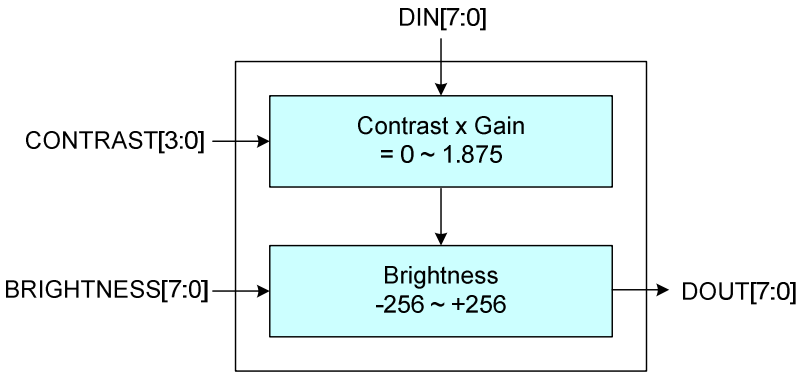
VI. R5 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	0	1	0	1	R/W	x	x	x	x	x	x	x	CONTRAST (1000)			

CONTRAST: RGB contrast level adjustment

CONTRAST	Function
D3~D0	
0000	0
1000	1 **(Default)**
1111	1.875

Note: each step is 0.125/LSB.



8-bit serial setting to control the contrast (gain) for RGB signals

DOUT [7:0] = DIN[7:0] x Contrast[0 to 1.0 to 1.875]

Note: output value above “255” is clipped

VII. R6 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	1	1	0	R/W	x	x	x	x	BRIGHTNESS						

BRIGHTNESS: RGB brightness level adjustment

BRIGHTNESS D6~D0	Function
00h	-256
40h	0 **(Default)**
7Fh	+256

Note: each step is 4/LSB.

8-bit serial setting to control the RGB brightness level

DOUT[7:0] = DIN [7:0] + BRIGHTNESS[-256 to 0 to +256]

Note: output value above “255” is clipped

VIII. R7 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R7	0	1	1	1	R/W	x	x	x	x	OP (000)			VGL_SEL (10)		VGH_SEL (11)	

OP: DAC output driving capability selection

OP D6~D4	Function

0XX	Controlled by input pin OP0 and OP1**(Default)**
100	-25%
101	Normal
110	+25%
111	+50%

VGL_SEL:VGL voltage selection

VGL_SEL	**Function**
D3~D2	
00	-8V
01	-9V
10	-10V **(Default)**
11	-11V

VGH_SEL:VGH voltage selection

VGH_SEL	**Function**
D1~D0	
00	12
01	13
10	14
11	15**(Default)**

IX. R8 Register

No.	**A4**	**A3**	**A2**	**A1**	**R/W**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R8	**1**	**0**	**0**	**0**	**R/W**	**x**	**x**	**x**	**1**	**VCOMH (1000001)**						

VCOMH: VCOMH level adjustment

VCOMH	**Voltage(V)**	
D6~D0	**MVA/TN Normal**	**TN LV**
00h	3.162	1.362
:	:	:
41h	4.332 **(Default)**	2.532 **(Default)**
:	:	:
7Fh	5.448	3.648

Note: Step is 18mV/step.

X. R9 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R9	1	0	0	1	R/W	x	x	x	x	VCOML (1000001)						

VCOML: VCOML level adjustment

VCOML	Voltage(V)	
D6~D0	MVA/TN Normal	TN LV
00h	-2.358	-2.628
:	:	:
41h	-1.188 **(Default)**	-1.458 **(Default)**
:	:	:
7Fh	-0.072	-0.342

Note: Step is 18mV/step.

XI. R10 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R10	1	0	1	0	R/W	x	x	x	PWM_400K (0)	DC_F (1)	CLK_ChP_M (10)		0	1	1	0

PWM_400K: PWM frequency selection

PWM_400K	Function
D7	
0	Around 200KHz. **(Default)**
1	Around 400KHz.

DC_F: DCDC frequency selection

DC_F	Function
D6	
0	Operating frequency is base on 13.5MHz.
1	Operating frequency is base on 27MHz. **(Default)**

CLK_ChP_M: Charge pumping frequency selection

CLK_ChP_M	Function
D5~D4	
00	F(Chp)= f(Hsync)/2
01	F(Chp)= f(Hsync)
10	F(Chp)= f(Hsync)*2. **(Default)**
01	F(Chp)= f(Hsync)*4

XII. R11~14 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R11	1	0	1	1	R/W	x	GMA_M (1)	GMA_V4 (011)			GMA_V1 (011)			GMA_V0 (011)		
R12	1	1	0	0	R/W	x	x	GMA_V48 (011)			GMA_V36 (011)			GMA_V16 (011)		
R13	1	1	0	1	R/W	x	x	x	x	x	GMA_V59 (011)			GMA_V55 (011)		
R14	1	1	1	0	R/W	x	x	x	x	x	GMA_V63 (011)			GMA_V62 (011)		

GMA_M: Gamma adjustment selection

GMA_M	Function
D9	
0	Manual adjust by registers R11~R14.
1	Auto set to gamma 2.2 by LC type. **(Default)**

C. Optical Specification (Note1, Note 2 and Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ=0°	 -- --	 10 15	 20 25	 ms ms	 Note 4
Contrast ratio		CR	At optimized viewing angle	150	300	--		Note 5,6
Viewing Angle	Top	Φ_T	CR≧10	35	50	--	deg.	Note 7
	Bottom	Φ_B		40	55	--		
	Left	Φ_L		45	60	--		
	Right	Φ_R		45	60	--		
Brightness		Y_L	θ=0°	200	250	--	cd/m^2	Note 8
Chromaticity	White	X	θ=0°	0.265	0.315	0.365		
		Y	θ=0°	0.290	0.340	0.390		

Note 1. Ambient temperature =25℃.

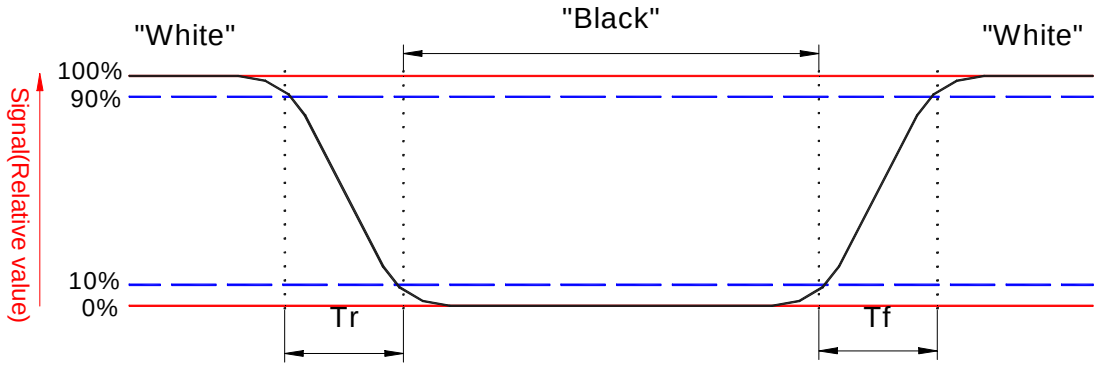
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-5A, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White $Vi=V_{i50} \overline{\pm} 1.5V$

Black $Vi=V_{i50} \pm 2.0V$

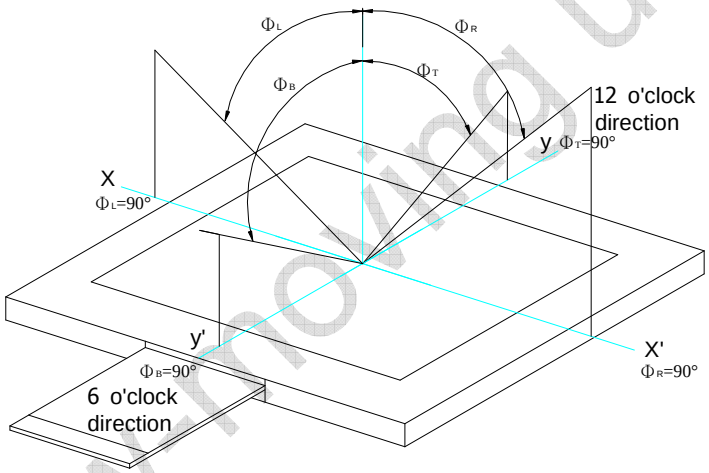
“±” Means that the analog input signal swings in phase with COM signal.

“$\overline{\pm}$” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

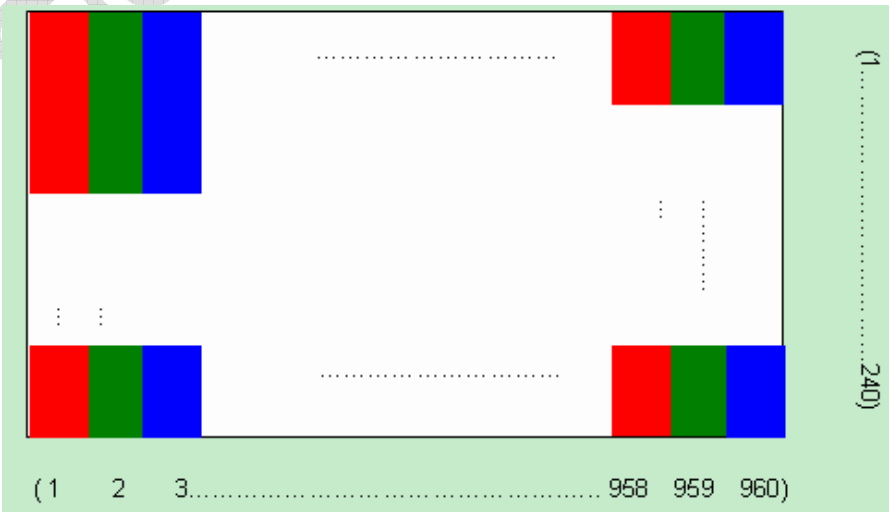
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle, Φ, Refer to figure as below.



Note 8. Measured at the center area of the panel in gray level 255

Note 9. Color Filter Arrangement

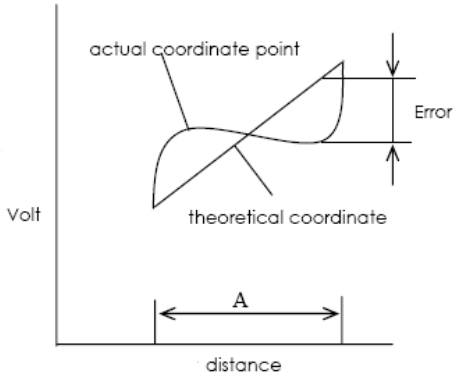


D. Touch Screen Panel Specifications

1. Electrical Characteristics

Item		Min.	Max.	Unit	Remark
Rate DC Voltage			5	V	
Resistance	X (Film)	100	1050	Ω	At connector
	Y (Glass)	100	600		
Linearity		-1.5%	1.5%	--	Note 1, test by 250 gf
Chattering			15	ms	At connector pin
Insulation Resistance		20M		Ω	DC 25V

Note 1: Measurement condition of Linearity: difference between actual voltage & theoretical voltage is an error at any points. Linearity is the value max. error voltage divided by voltage difference on active area.(Test location should keep at least 2mm from active area edge)

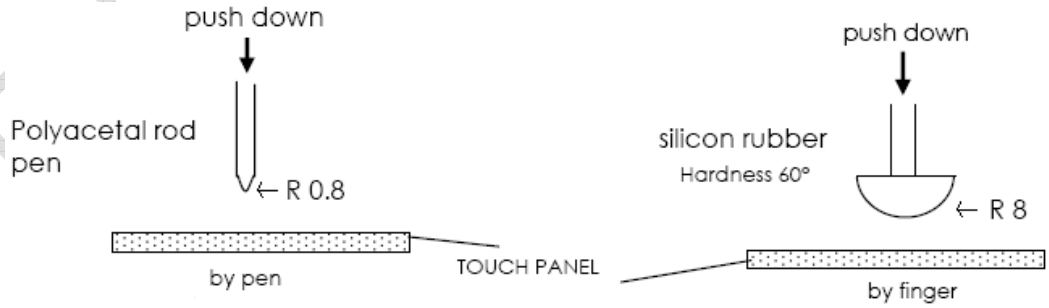


2. Mechanical Characteristics

Item	Min.	Max.	Unit	Remark
Hardness of Surface	3	--	H	JIS K-5400
Activation Force (Pen or Finger)	--	40	gf	Note 1

Note 1: Within ”guaranteed active area”, but not on the edge and dot-spacer.

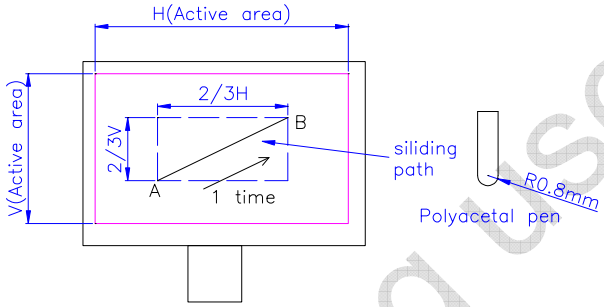
Note 2: Activation force measurement is under test condition as figure below.



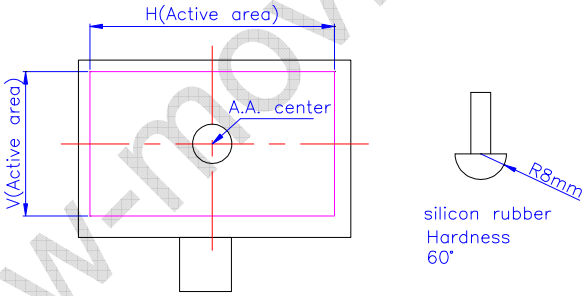
3. Life test Condition

Item	Min.	Max.	Unit	Remark
Notes Life	10^5	--	words	Note 2
Input Life	10^6	--	times	Note 3

Note 1: Notes Life test condition (by pen): slide on central 2/3 of active area and use R 0.8mm polyacecal pen, input force : 250gf, frequency : 60mm/sec. Sliding from A to B complete 1 time. shown as figure2.



Note 2: Input Life test condition (by finger): test position on active area center and use R8.0mm silicon rubber (hardness 60˚), test force: 250gf, frequency : 2times/sec. shown as figure.



4. Attention

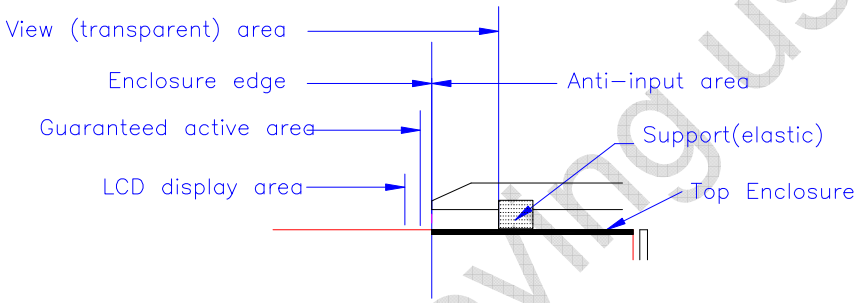
Please pay attention for below matters at mounting design of touch panel of LCD module.

1. Do not design enclosure pressing the view area to prevent from miss input.
2. Enclosure support must not touch with view area.
3. Use elastic or non-conductive material to enclosure touch panel.
4. Do not bond film of touch panel with enclosure.
5. The touch panel edge is conductive. Do not touch it with any conductive part after mounting.
6. If user wants to cleaning touch panel by air gun, pressure 2kg/cm2 below is suggested. Not to blow glass from FPC site to prevent FPC peeled off.
7. Do not put a heavy shock or stress on touch panel and film surface. Ex. Don't lift the panel by film face

with vacuum.

8. Do not lift LCD module by FPC.
9. Please use dry cloth or soft cloth with neutral detergent (after wring dry) or one with ethanol at cleaning. Do not use any organic solvent, acid or alkali liquor.
10. Do not pile touch panel. Do not put heavy goods on touch panel.
11. In order to get the optimal mapping between TFT-LCD and Touch Panel**,** each touch panel needs to be executed calibration (5 points at least) before operating touch functions..For detail calibration algorisms, please refer to touch panel driving IC user manuals.
12. The visible newton ring appearance on the surface of touch panel is predictable since the low activation force request.

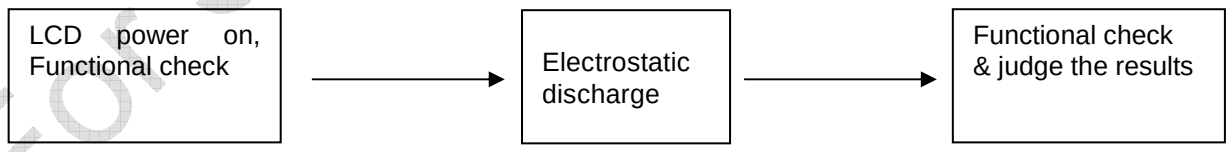
Recommendation of the cushion area:



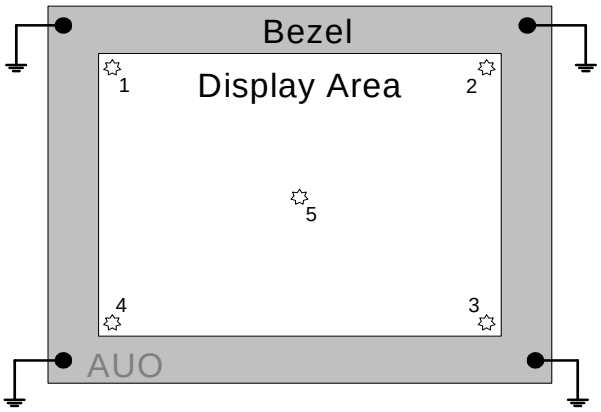
E. Reliability Test Items

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 80℃ 240Hrs	
2	Low Temperature Storage	Ta= -40℃ 240Hrs	
3	High Ttemperature Operation	Tp= 70℃ 240Hrs	
4	Low Temperature Operation	Tp=- 20 ℃ 240Hrs	
5	High Temperature & High Humidity	Tp= 60℃. 90% RH 240Hrs	Operation
6	Heat Shock	-30℃~80℃, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note 2,3
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1. Ta: Ambient temperature.
Note 2. ESD Testing Flow as the below,

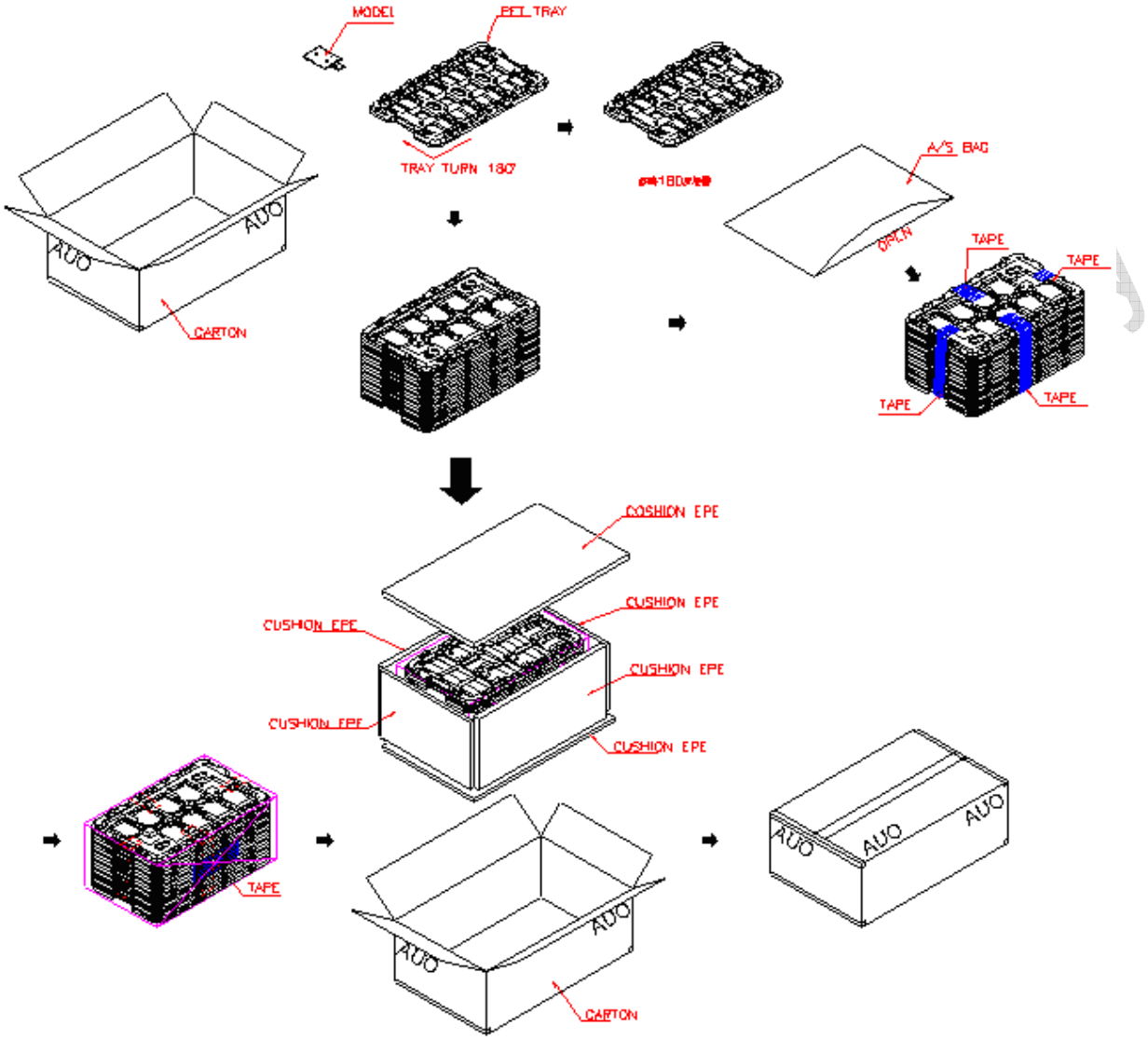


Note 3. ESD testing method.
1. Ambient: 24~26℃, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Operation System: “CX40FL-B” and adapter “A035QN04 V0T0”
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
   a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
   b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:



7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

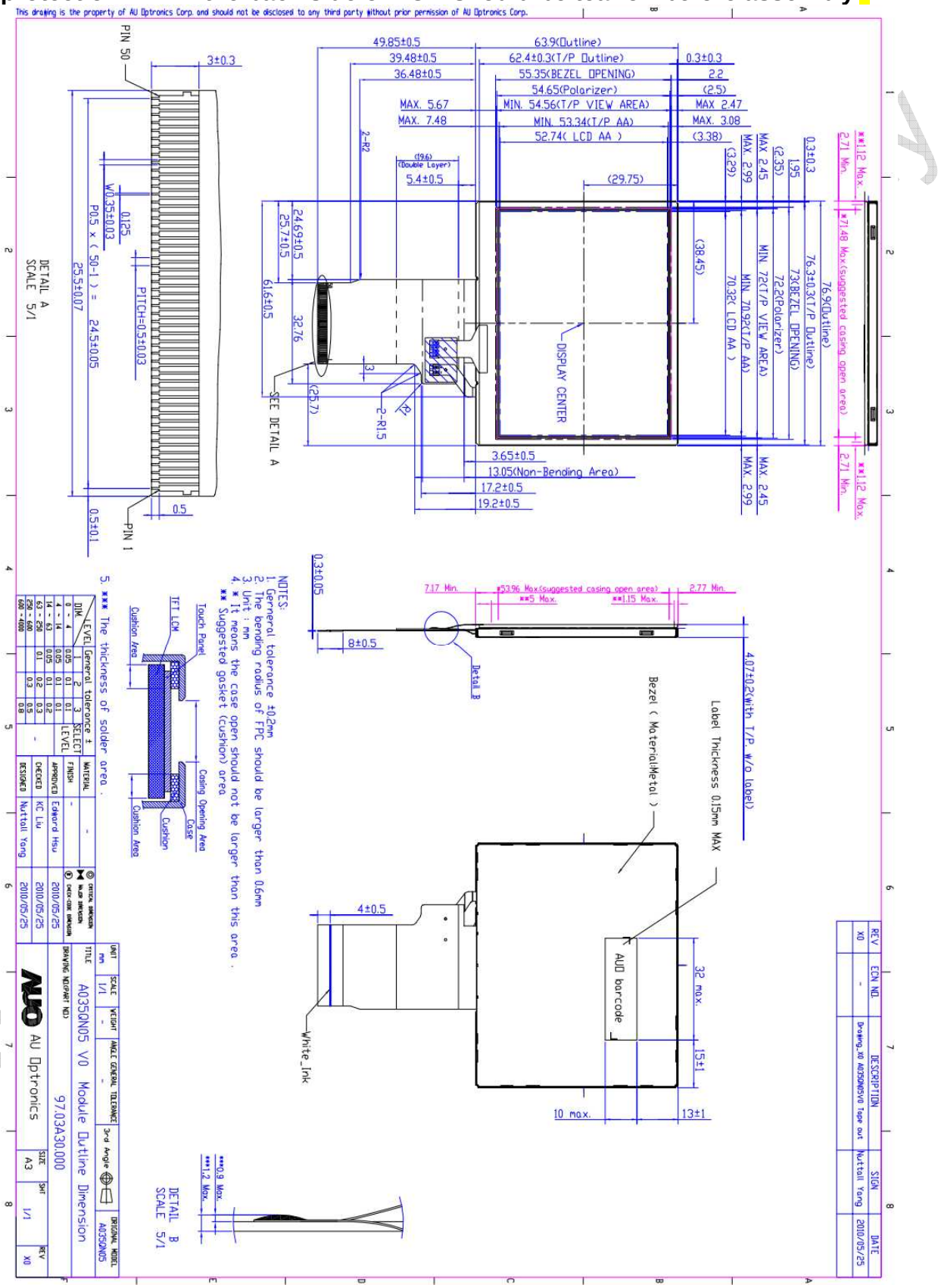
F. Packing Form



G. Outline dimension

Any stress or attachment on the back of the LCD module is forbidden.

The protection film in the back side of LCM should be tear off before assembly.



H. Application note

1.Recommended Register Settings

a. 8-bit Serial Interface HV Sync. Mode without Dummy

Power On

No.	Command		NOTE
	High byte	Low byte	
1	00h	31h	NOTE1
Whait 50 us			
2	00h	39h	
Whait 100 us			
3	10h	38h	NOTE2
4	21h	46h	
5	30h	15h	
6	43h	CBh	
7	50h	08h	
8	60h	40h	
9	70h	0Bh	
10	80h	B5h	
11	90h	35h	
12	A0h	66h	
13	B1h	F3h	
14	C1h	77h	
15	D0h	2Dh	
16	E0h	1Ah	
17	00h	3Dh	

Power Off

No.	Command		NOTE
	High byte	Low byte	
1	00h	39h	NOTE3

NOTE 1. Please add these commands if you don't use the HW Reset.
NOTE 2.Please refer to the POWER ON sequence section for register setting timing as power-on.
NOTE 3.Please refer to the POWER OFF sequence section for register setting timing as power-off.

b. 8-bit Serial Interface HV Sync. Mode with Dummy

Power On

No.	Command		NOTE
	High byte	Low byte	
1	00h	31h	NOTE1
Whait 50 us			
2	00h	39h	
Whait 100 us			
3	10h	39h	NOTE2
4	21h	F1h	
5	30h	15h	
6	43h	CBh	
7	50h	08h	
8	60h	40h	
9	70h	0Bh	
10	80h	B5h	
11	90h	35h	
12	A0h	66h	
13	B1h	F3h	
14	C1h	77h	
15	D0h	2Dh	
16	E0h	1Ah	
17	00h	3Dh	

Power Off

No.	Command		NOTE
	High byte	Low byte	
1	00h	39h	NOTE3

NOTE 1. Please add these commands if you don't use the HW Reset.
NOTE 2.Please refer to the POWER ON sequence section for register setting timing as power-on.
NOTE 3.Please refer to the POWER OFF sequence section for register setting timing as power-off.

c. YUV640 Mode

Power On

No.	Command		NOTE
	High byte	Low byte	
1	00h	31h	NOTE1
Whait 50 us			
2	00h	39h	
Whait 100 us			
3	10h	3Ch	NOTE2
4	21h	F0h	
5	30h	15h	
6	43h	CBh	
7	50h	08h	
8	60h	40h	
9	70h	0Bh	
10	80h	B5h	
11	90h	35h	
12	A0h	66h	
13	B1h	F3h	
14	C1h	77h	
15	D0h	2Dh	
16	E0h	1Ah	
17	00h	3Dh	

Power Off

No.	Command		NOTE
	High byte	Low byte	
1	00h	39h	NOTE3

NOTE 1. Please add these commands if you don't use the HW Reset.
NOTE 2.Please refer to the POWER ON sequence section for register setting timing as power-on.
NOTE 3.Please refer to the POWER OFF sequence section for register setting timing as power-off.

d. YUV720 Mode

Power On

No.	Command		NOTE
	High byte	Low byte	
1	00h	31h	NOTE1
Whait 50 us			
2	00h	39h	
Whait 100 us			
3	10h	3Dh	NOTE2
4	21h	F0h	
5	30h	15h	
6	43h	CBh	
7	50h	08h	
8	60h	40h	
9	70h	0Bh	
10	80h	B5h	
11	90h	35h	
12	A0h	66h	
13	B1h	F3h	
14	C1h	77h	
15	D0h	2Dh	
16	E0h	1Ah	
17	00h	3Dh	

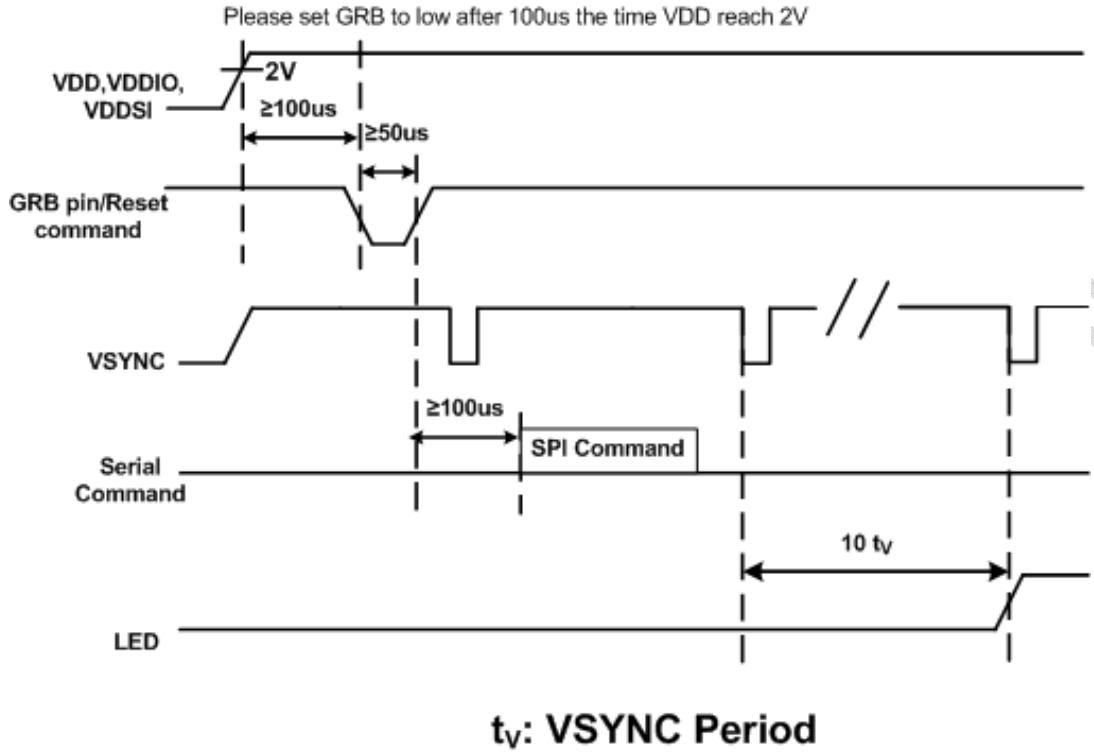
Power Off

No.	Command		NOTE
	High byte	Low byte	
1	00h	39h	NOTE3

NOTE 1. Please add these commands if you don't use the HW Reset.
NOTE 2.Please refer to the POWER ON sequence section for register setting timing as power-on.
NOTE 3.Please refer to the POWER OFF sequence section for register setting timing as power-off.

2. Power on/off sequence

e. Power on (Standby Disabling)

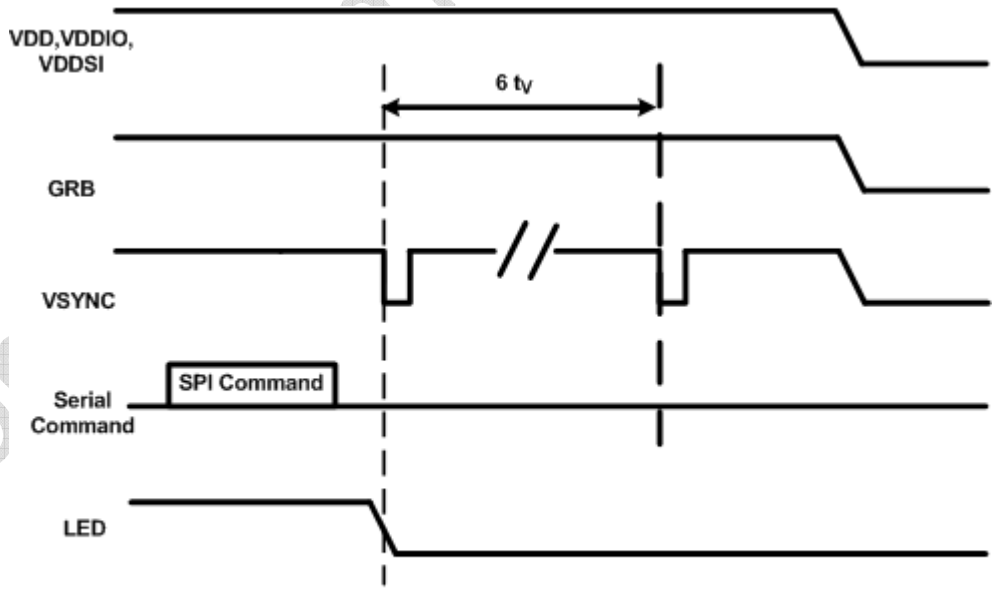


t_V: VSYNC Period

Note

1: After Setting Recommended Register, the driver enters intro the normal operating mode.
2: RESET signal is necessary for power on, Please refer to the POWER ON sequence.
You can use HW GRB PIN or SW Reset command to do this.
3: After the driver enters intro the normal operating mode, The minimum cycle time of LED ON is 10 frames.

f. Power off (Standby Enabling)



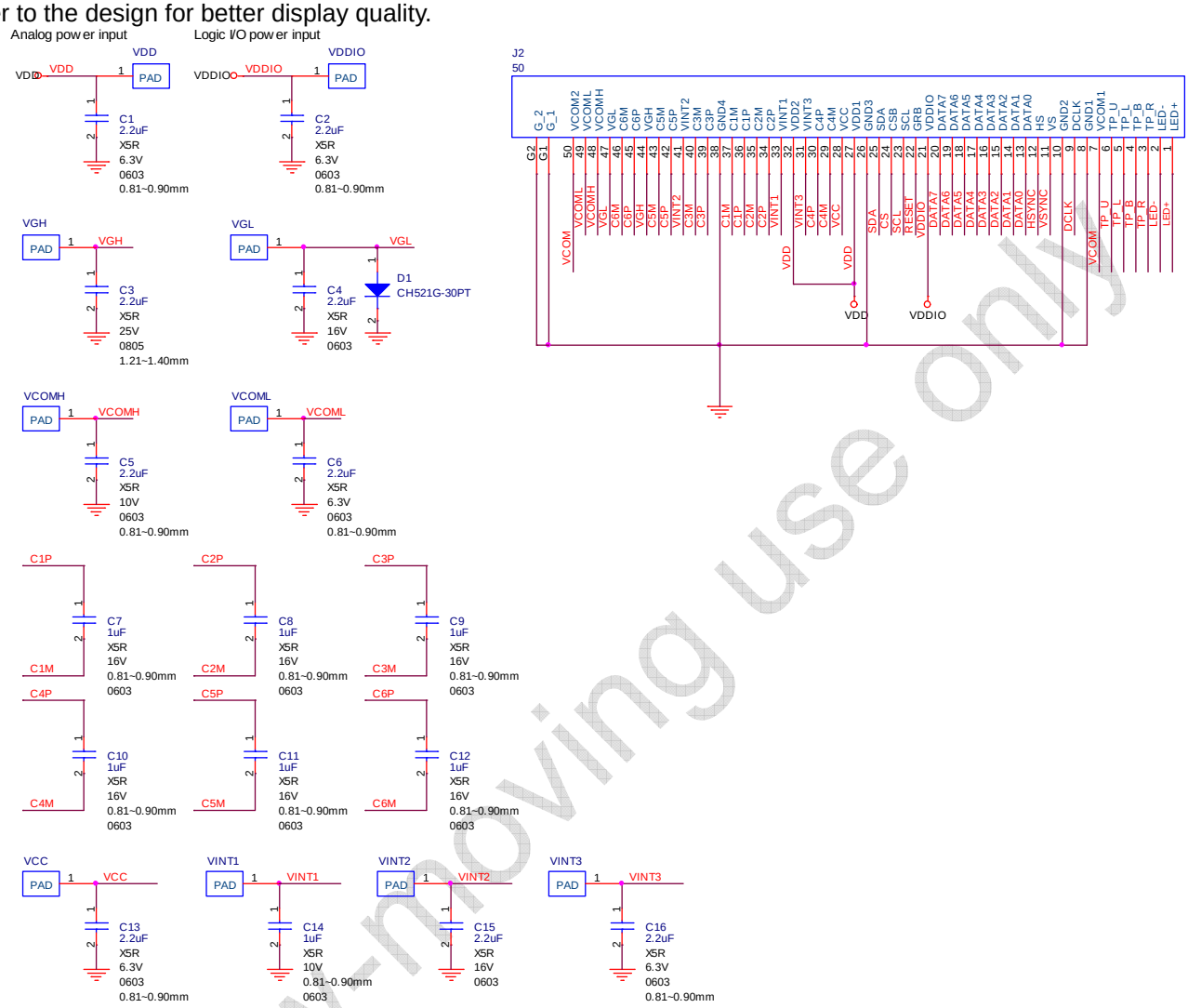
t_V: VSYNC Period

Note

1: After Setting Recommended Register, the driver enters intro standby mode.
2: Please Let LED OFF after the driver enters intro thestandby mode,
3: When enters intro standby mode, The minimum cycle time of VDD OFF is 6 frames.

3. Suggested Circuit

The suggested circuit and recommended capacitor sepcification are both showed as follows. Please refer to the design for better display quality.



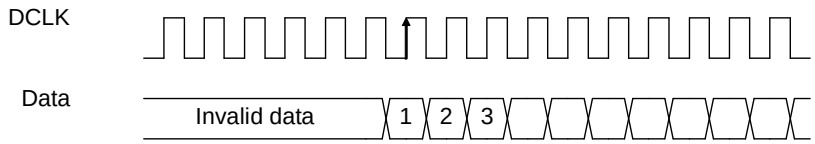
4. Input Data Timing

When SEL = “000” HV mode without dummy is selected, the input data RGB sequence should match the setting of SHL in R1.

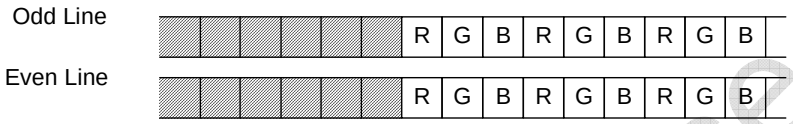
When SHL = ’1’, the RGB sequence of input data is “R data” -> “G data” -> “B data”.

When SHL = ’0’, the RGB sequence of input data is “B data” -> “G data” -> “R data”.

The illustration is shown as below:



❖ SHL = ‘1’, H shift direction = left to right.



❖ SHL = ‘0’, H shift direction = right to left.