SAT ELECTRONIC CO.LTD

SPECIFICATION

Customer: _____

Model Name: SAT035CM54D06R4-30638T058KN-G

SPEC NO.: _____

Date: _____

Version: _____

■Preliminary Specification

□Final Specification

Approved by	Comment

Prepared by	Reviewed by	Approved by

Record of Revision

Version	Revise Date	Page	Content
Pre-spec.A	2015/07/20		Initial Release

Contents

1. General Specifications

No.	Item	Specification	Remark
1	LCD size	3.5 inch(Diagonal)	
2	Driver element	a-Si TFT active matrix	
3	Resolution	320 × 3(RGB) ×240	
4	Display mode	Normally White, Transmissive	
5	Pixel pitch	0.073(H) X 0.219(V) mm	
6	Active area	70.08(H) X 52.56(V) mm	
7	Outline dimensions	76.9(H) X 63.9(V) X 3.0(D) mm	
8	Surface treatment	Anti-Glare	
9	Color arrangement	RGB-stripe	
10	Interface	RGB/CCIR656/CCIR601	
11	Backlight Power consumption	TBD	
12	Panel Power consumption	TBD	
13	Weight	TBD	

2. Pin Assignment

FPC Connector is used for the module electronics interface. The recommended model is FH12A-54S-0.5SH manufactured by Hirose

Pin	Symbol	I/O	Function	Remark
1	VBL-	I	Backlight LED Ground	
2	VBL-	I	Backlight LED Ground	
3	VBL+	I	Backlight LED Power	
4	VBL+	I	Backlight LED Power	
5	Y1	I	Top electrode ,	
6	X1	I	Right electrode	
7	NC		Not Use	
8	/RESET	-	Hardware Reset	
9	SPENA	I	SPI Interface Data Enable Signal	Note 3
10	SPCLK	I	SPI Interface Data Clock	Note 3
11	SPDAT	I	SPI Interface Data	Note 3
12	B0	I	Blue Data Bit 0	
13	B1	I	Blue Data Bit 1	
14	B2	I	Blue Data Bit 2	
15	B3	I	Blue Data Bit 3	
16	B4	I	Blue Data Bit 4	
17	B5	I	Blue Data Bit 5	
18	B6	I	Blue Data Bit 6	
19	B7	I	Blue Data Bit 7	
20	G0	I	Green Data Bit0	
21	G1	I	Green Data Bit1	
22	G2	I	Green Data Bit2	
23	G3	I	Green Data Bit3	
24	G4	I	Green Data Bit4	
25	G5	I	Green Data Bit5	
26	G6	I	Green Data Bit6	
27	G7	I	Green Data Bit7	
28	R0	I	Red Data Bit0 /DX0	Note 4
29	R1	I	Red Data Bit1 /DX1	Note 4
30	R2	I	Red Data Bit2 /DX2	Note 4
31	R3	I	Red Data Bit3 /DX3	Note 4
32	R4	I	Red Data Bit4 /DX4	Note 4
33	R5	I	Red Data Bit5 /DX5	Note 4
34	R6	I	Red Data Bit6 /DX6	Note 4

35	R7	I	Red Data Bit7 /DX7	Note 4
36	HSYNC	I	Horizontal Sync Input	
37	VSYNC	I	Vertical Sync Input	
38	DCLK	I	Dot Data Clock	
39	NC		Not Use	
40	NC		Not Use	
41	Vcc	I	Digital Power	
42	Vcc	I	Digital Power	
43	Y2	I	Bottom electrode	
44	X2	I	Left electrode	
45	NC		Not Use	
46	NC	-	Not Use	
47	NC		Not Use	
48	IF2	I	Control the input data format /floating	Note 1
49	IF1	I	Control the input data format	Note 1,5
50	IF0	I	Control the input data format	Note 1,5
51	NC		Not Use	
52	DE	I	Data Enable Input	Note 2
53	GND	I	Ground	
54	GND	I	Ground	

Note:

1. The mode control (IF2) not use ,it can't control CCIR601 interface , If not use CCIR601 ,it can floating.
2. For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported. If DE signal is fixed low, SYNC mode is used. Otherwise, DE+SYNC mode is used.Suggest used SYNC mode!!
3. usually pull high.
4. IF select serial RGB or CCIR601/656 input mode is selected,only DX0-DX7 used,and the other short to GND, Only selected serial RGB、CCIR601/656 interface,DX BUS will enable,Digital input mode DX0 is LSB and DX7 is MSB.
5. Control the input data format

IF2-0: Define the input interface mode.

IF2	IF1	IF0	Format	Operating Frequency
0	0	0	Parallel-RGB data format (only support stripe type color filter)	6.5MHz
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Mode	D[23:16]	D[15:8]	D[7:0]	IHS	IVS	DEN
ITU-R BT 656	D[23:16]	GND	GND	NC	NC	NC
ITU-R BT 601	D[23:16]	GND	GND	IHS	IVS	NC
8 bit RGB	D[23:16]	GND	GND	IHS	IVS	NC for HV Mode DEN for DEN Mode
24 bit RGB	R[7:0]	G[7:0]	B[7:0]	IHS	IVS	NC for HV Mode DEN for DEN Mode

3. Operation Specifications

3.1. Absolute Maximum Ratings

(Note 1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Supply voltage	VCIP	-0.3	5.0	V	
Supply voltage	V1–V6	-0.3	VDDA+0.3	V	
Logic Supply voltage	VCI	-0.5	5.0	V	
Analog Supply voltage	VDDA	-0.5	7.5	V	
	V_{GH}-V_{GL}	-0.3	25	V	
Operation Temperature	T_{OP}	-20	70	℃	
Storage Temperature	T_{ST}	-30	80	℃	

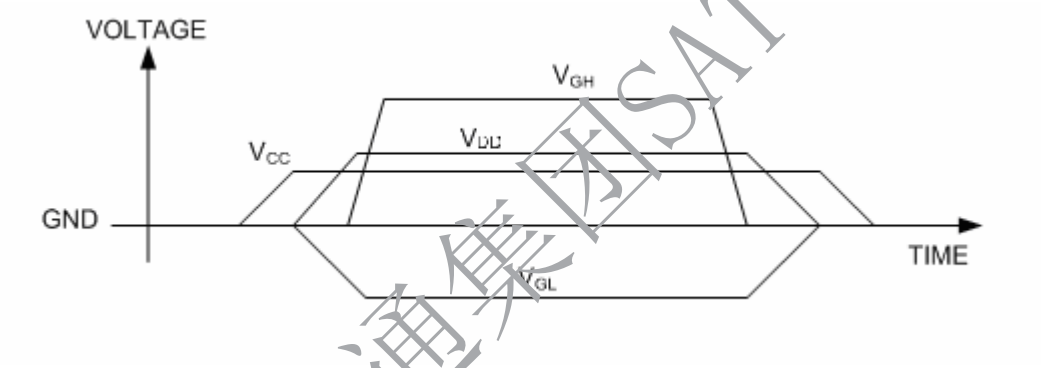
Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

3.1.1. Typical Operation Conditions

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power Voltage	VCC	3.0	3.3	3.6	V	
Digital Operation Current	Icc		8.6		mA	
Gate On Power	VGH	14	15	18	V	
Gate Off Power	VGL	-11	-10	-8	V	
Vcom High Voltage	VcomH		3.7		V	Note1
Vcom low Voltage	VcomL		-1.6		V	Note1
Vcom level max	VcomA			6	V	

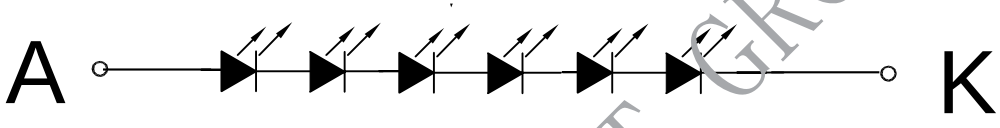
Note1. VcomH& VcomL：Adjust the color with gamma data. Vp-p should be higher then 4V.(Option 5V)

Note: Please power on following the sequence VCC → VDD



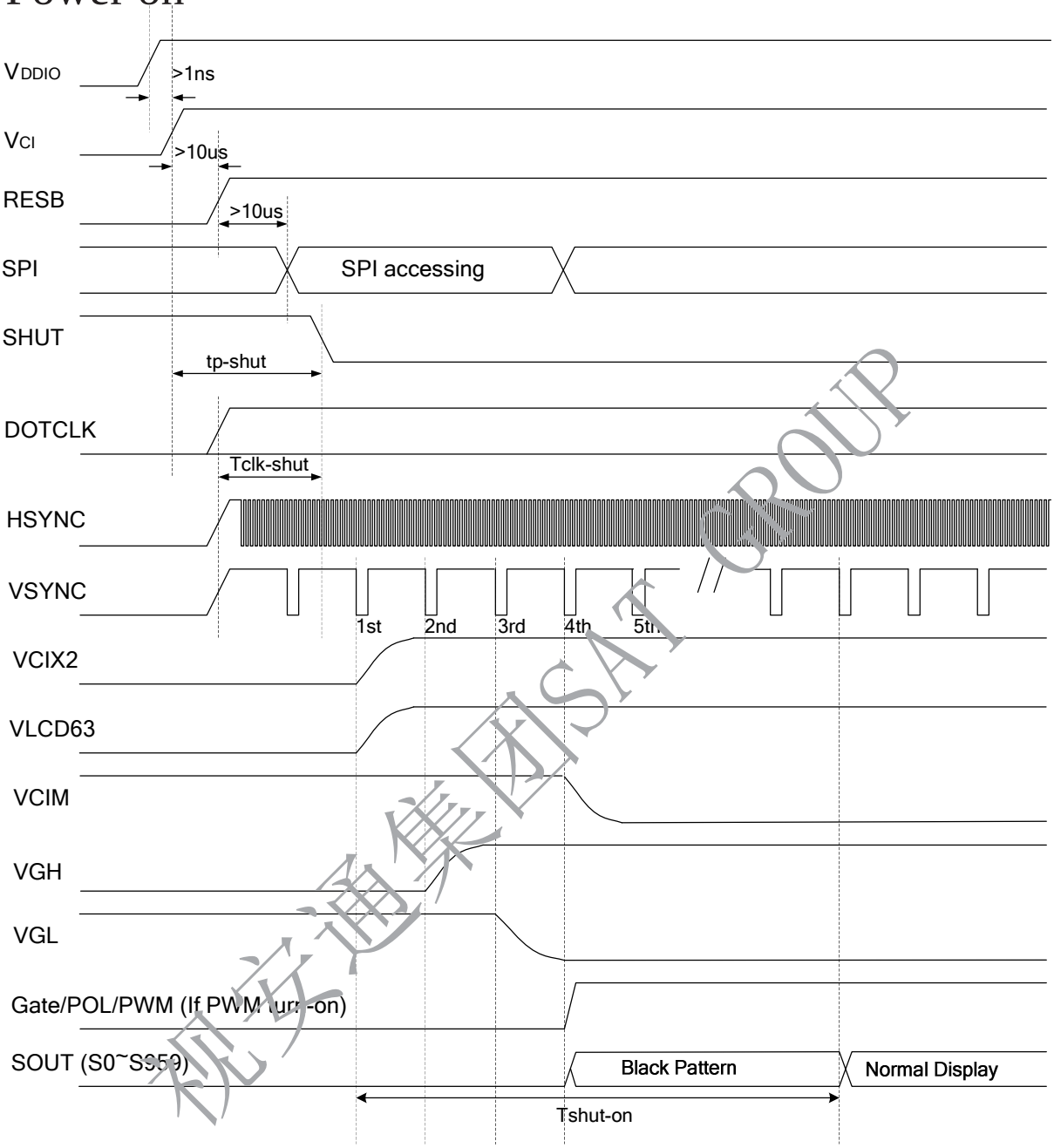
3.1.2. Backlight Driving Conditions (6 White Chips)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage of white LED backlight	VL	17.4	19.8	21	V	Note 1
Current for LED backlight	IL	15	20	25	mA	
Luminance (on the module surface,BM-7)		360	410	-	cd/m^2	
LED life time	-	20,000	-	50,000	Hr	Note 2



3.2. Power Sequence

Power on



Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
VDDD / VDDIO on to falling edge of SHUT	tp-shut	1	-	-	μs
DOTCLK	tclk-shut	1	-	-	clk
Falling edge of SHUT to display start - 1 line: 408 clk - 1 frame: 262 line -DOTCLK = 6.5MHz	tshut-on	-	-	14	frame
		-	166	232.4	ms

Note: It is necessary to input DOTCLK before the falling edge of SHUT.
Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

PowerUpSequence

Power off

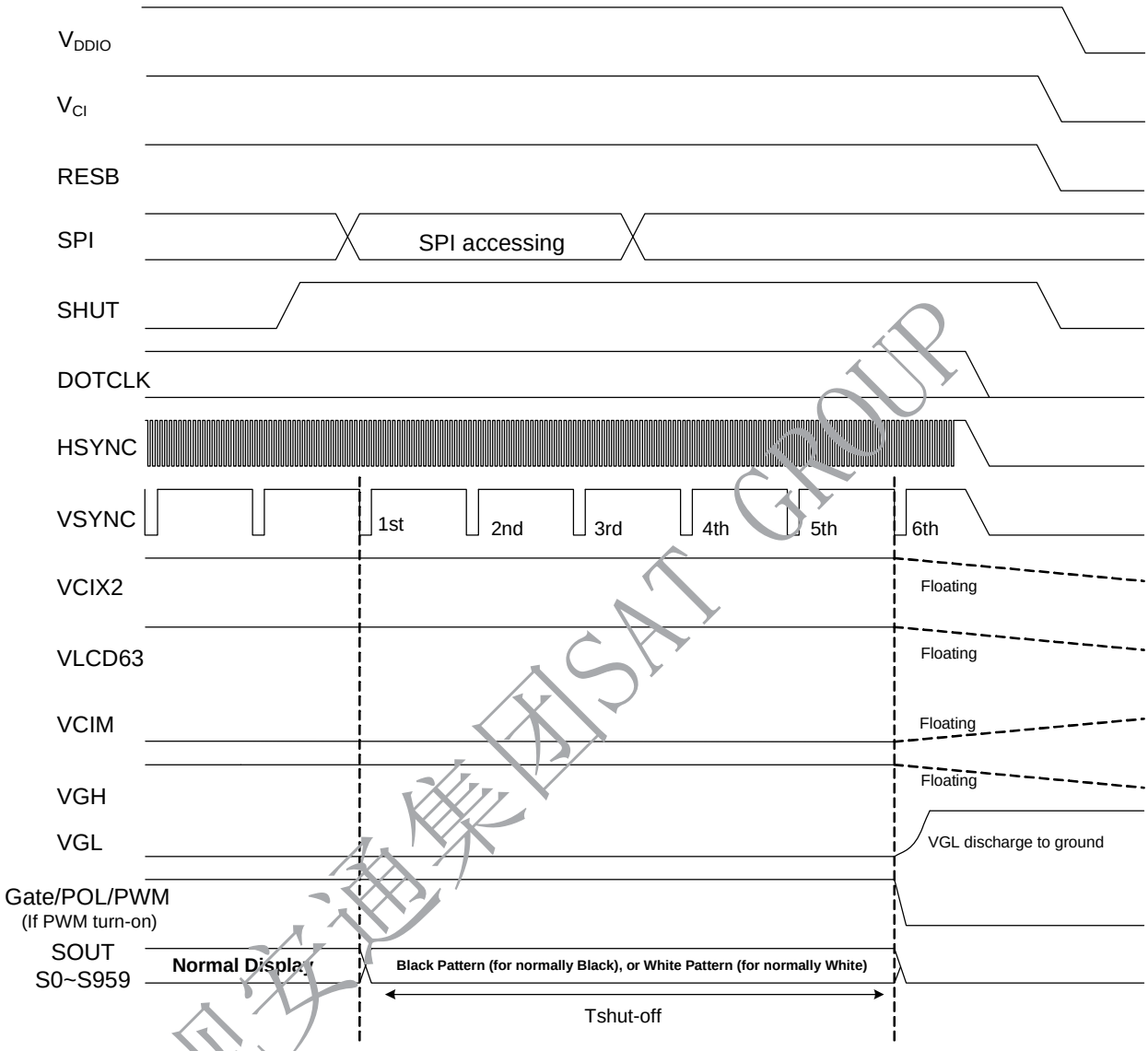


Figure 12. 11 Power Down Sequence

Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Rising edge of SHUT to display off - 1 line: 408 clk - 1 frame: 262 line - DOTCLK = 6.5MHz	tshut-off	2	-	-	frame
		33.4	-	-	ms

Note: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.
Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.
If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

Table 12. 4 Power Down Sequence

3.3. Timing Characteristics

AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 2.2V, T_A = 25℃)

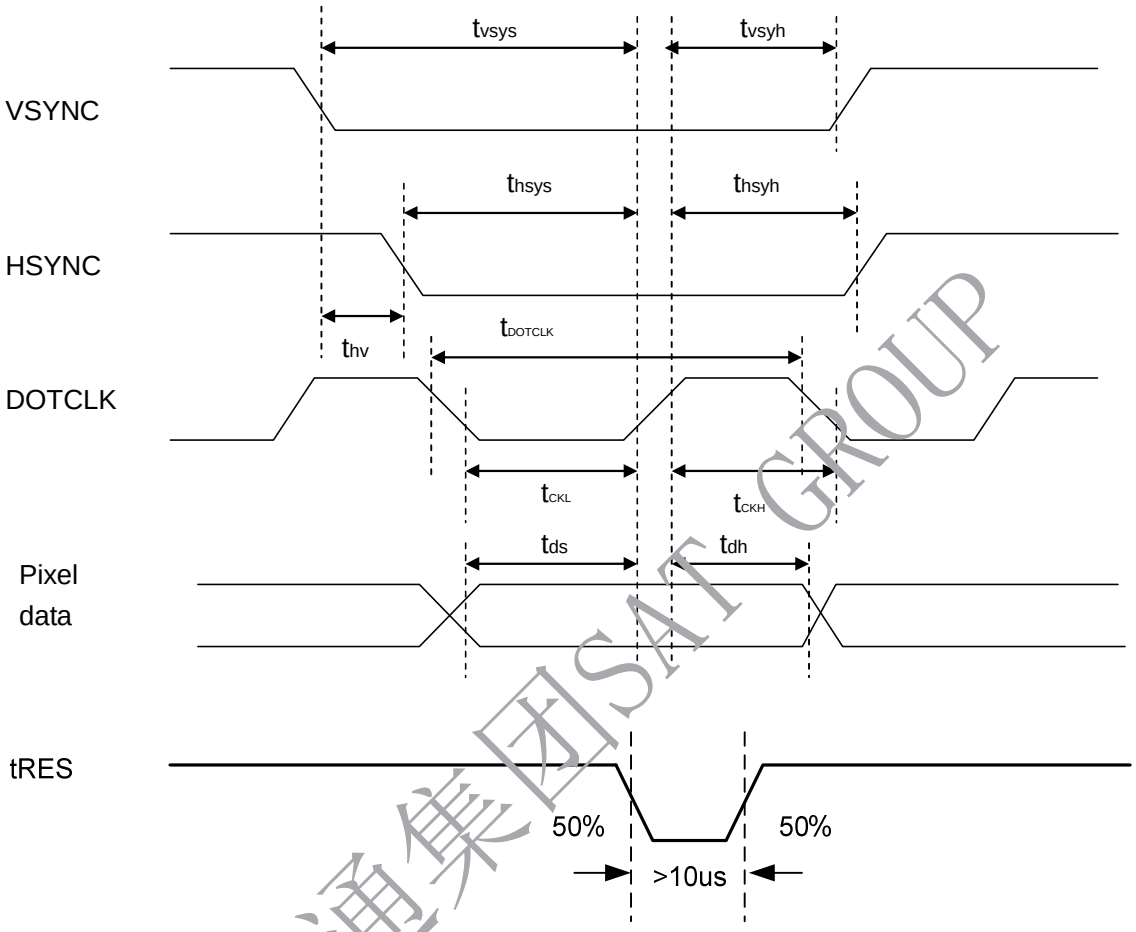


Figure 12. 1 Pixel Timing

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Vertical Sync Setup Time	tvsys	20	10	-	-	-	-	ns
Vertical Sync Hold Time	tvsyh	20	10	-	-	-	-	ns
Horizontal Sync Setup Time	thsys	20	10	-	-	-	-	ns
Horizontal Sync Hold Time	thsyh	20	10	-	-	-	-	ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-	-	-	-	ns
DOTCLK High Period	tCKH	50	15	-	-	-	-	ns
Data Setup Time	tds	12	10	-	-	-	-	ns
Data hold Time	tdh	12	10	-	-	-	-	ns
Reset pulse width	tRES	10		-		-		μs

Note: External clock source must be provided to DOTCLK pin of HX8238-D. The driver will not operate if absent of the clocking signal.

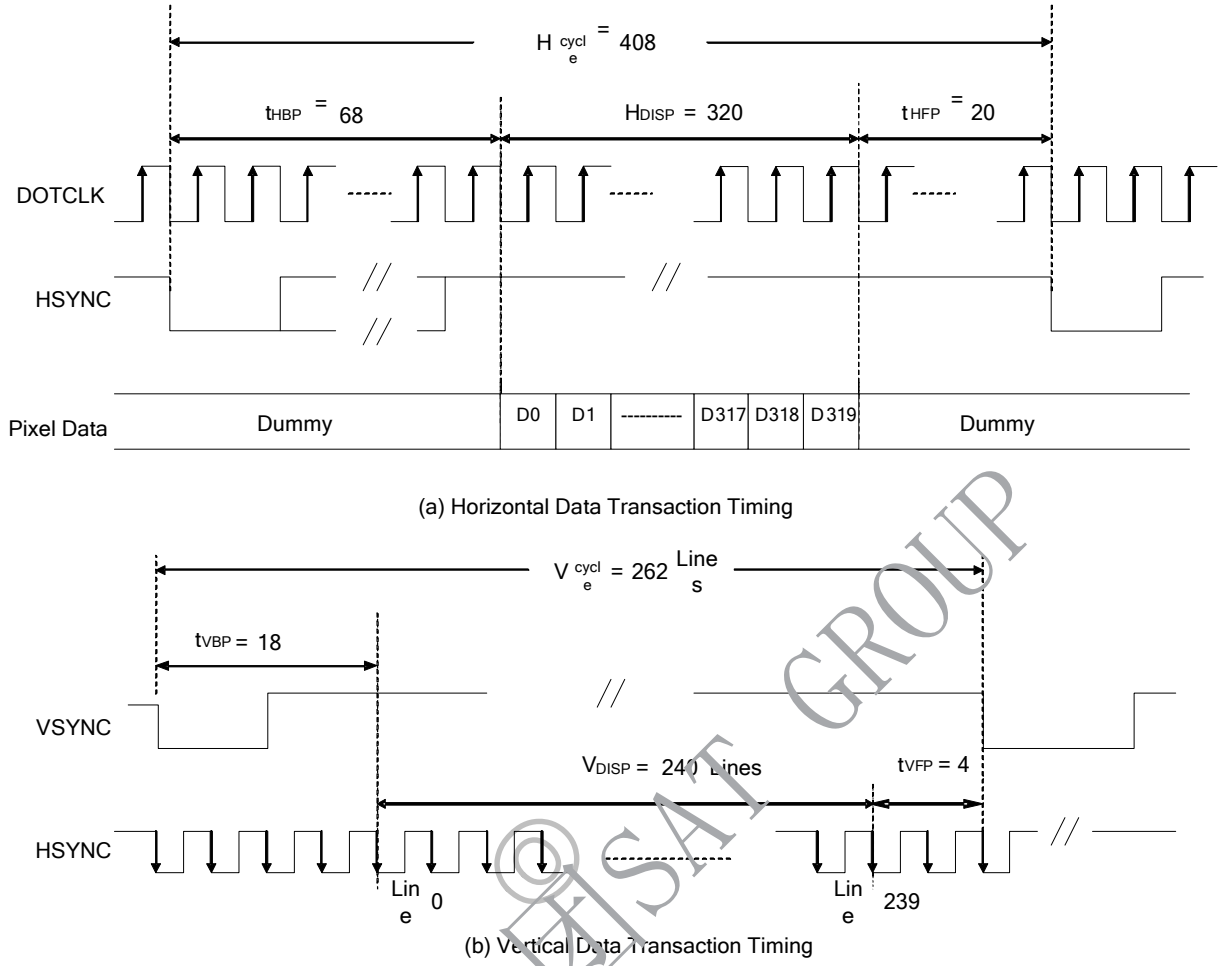


Figure 12. 2 Data Transaction Timing in Parallel RGB (24 bit) Interface (SYNC Mode)

Characteristics		Symbol	Min.		Typ.		Max.		Unit
			24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency		fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period		tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)		fH	-		14.9		22.35		KHz
Vertical Frequency (Refresh)		fV	-		60		90		Hz
Horizontal Back Porch		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Front Porch		tHFP	-	-	20	60	-	-	tDOTCLK
Horizontal Data Start Point		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Blanking Period		tHBP + tHFP	-	-	88	264	-	-	tDOTCLK
Horizontal Display Area		HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle		Hcycle	-	-	408	1224	450	1350	tDOTCLK
Vertical Back Porch		tVBP	-		18		-		Lines
Vertical Front Porch		tVFP	-		4		-		Lines
Vertical Data Start Point		tVBP	-		18		-		Lines
Vertical Blanking Period		tVBP + tVFP	-		22		-		Lines
Vertical Display Area	NTSC	VDISP	-		240		-		Lines
	PAL				280(PALM=0)				
	PAL				288(PALM=1)				
Vertical Cycle	NTSC	Vcycle	-		262		350		Lines
	PAL				313				

Table 12. 2 Data Transaction Timing in Normal Operating Mode

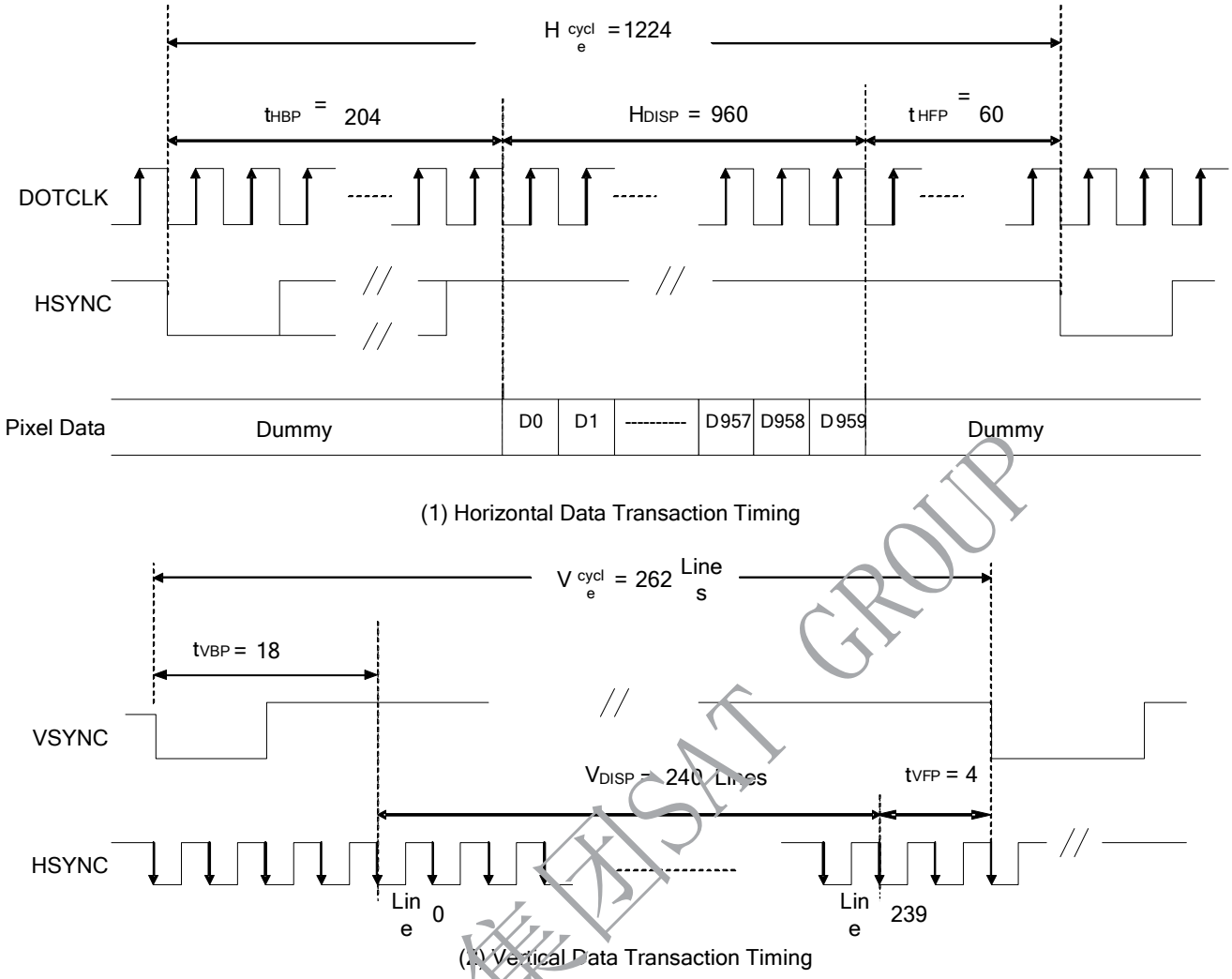


Figure 12. 3 Data Transaction Timing in Serial RGB (8 bit) Interface (SYNC Mode)

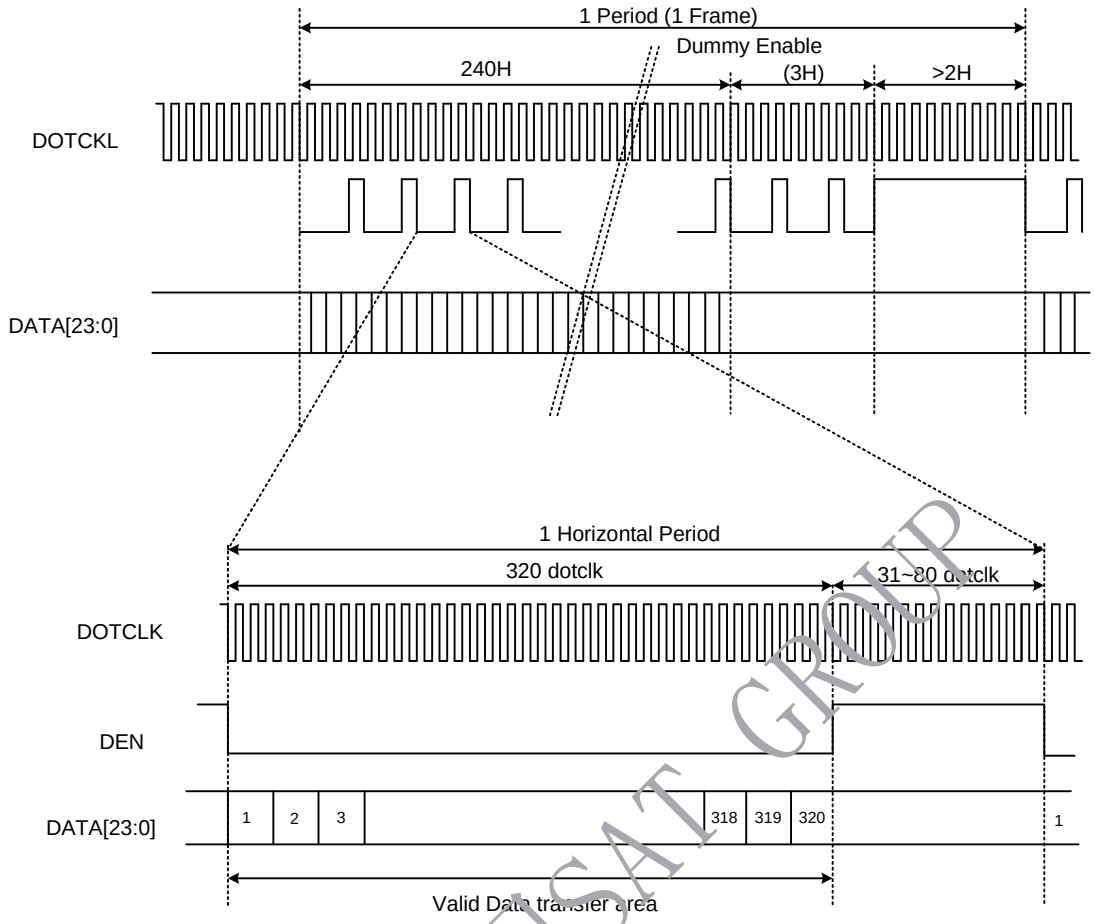
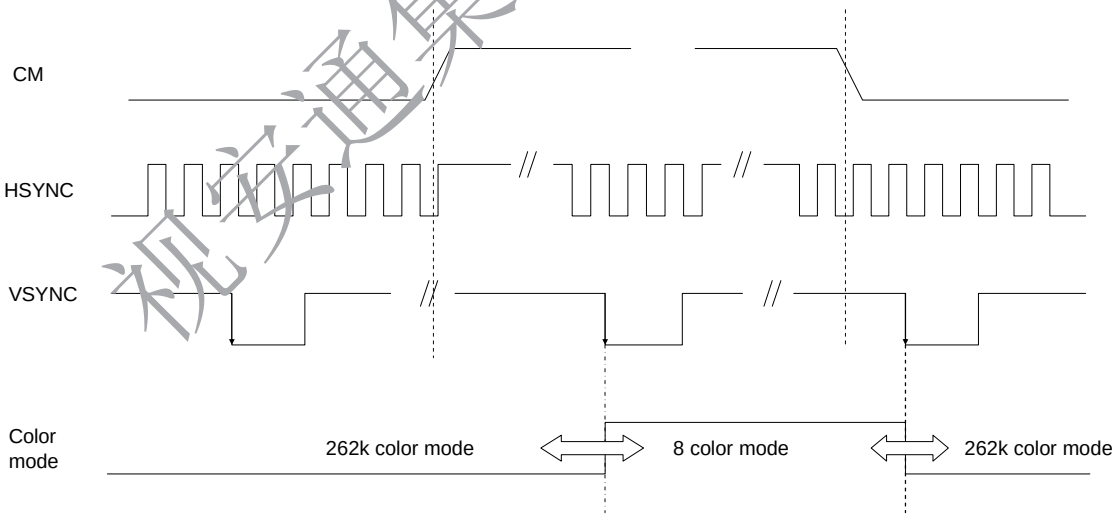


Figure 12. 4 Signal Timing in DE Mode



Note: The color mode conversion starts at the first falling edge of VSYNC after stage change of CM.

Figure 12. 5 Color Mode Conversion Timing

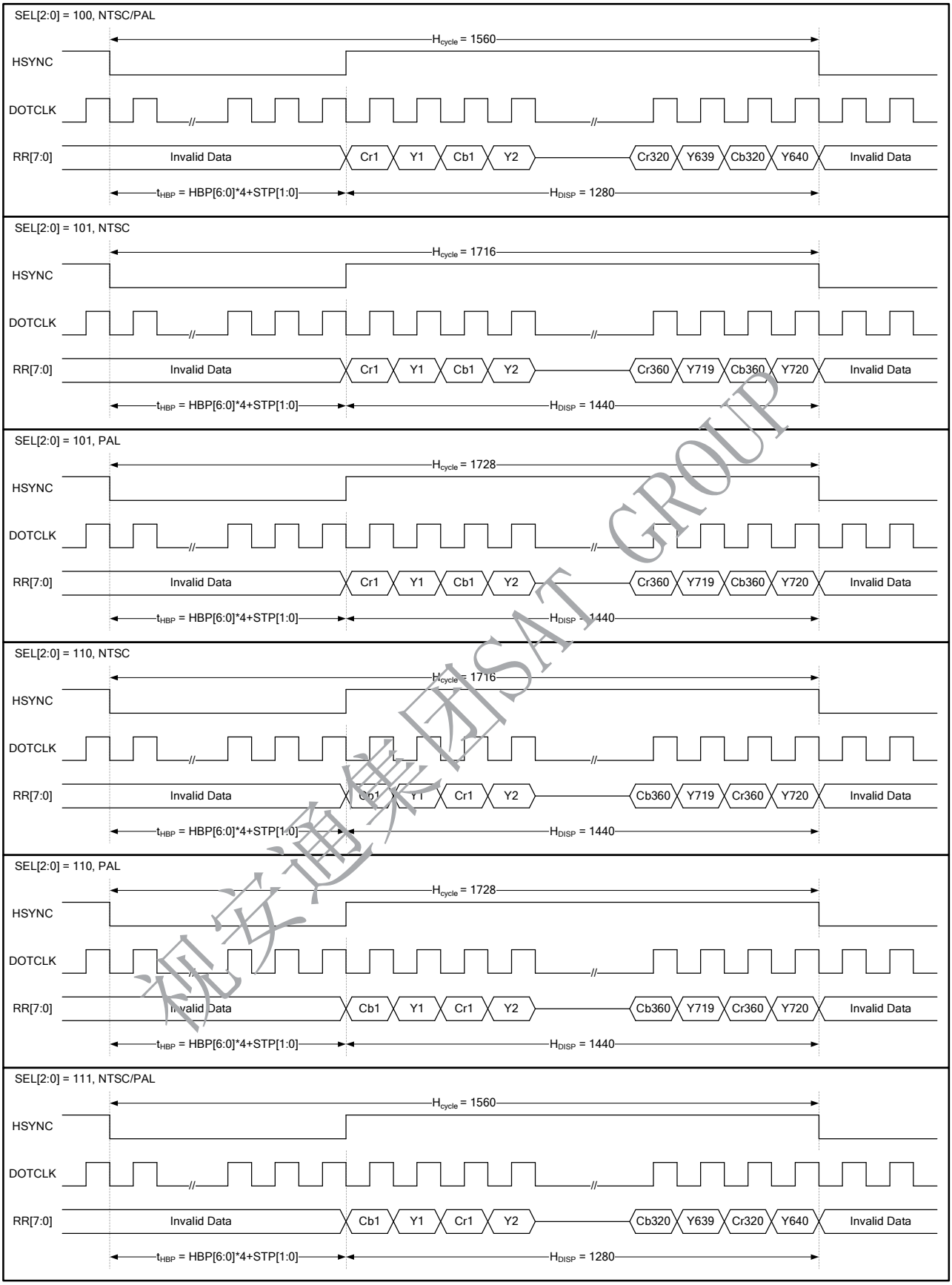


Figure 12. 6 CCIR601 Horizontal Timing

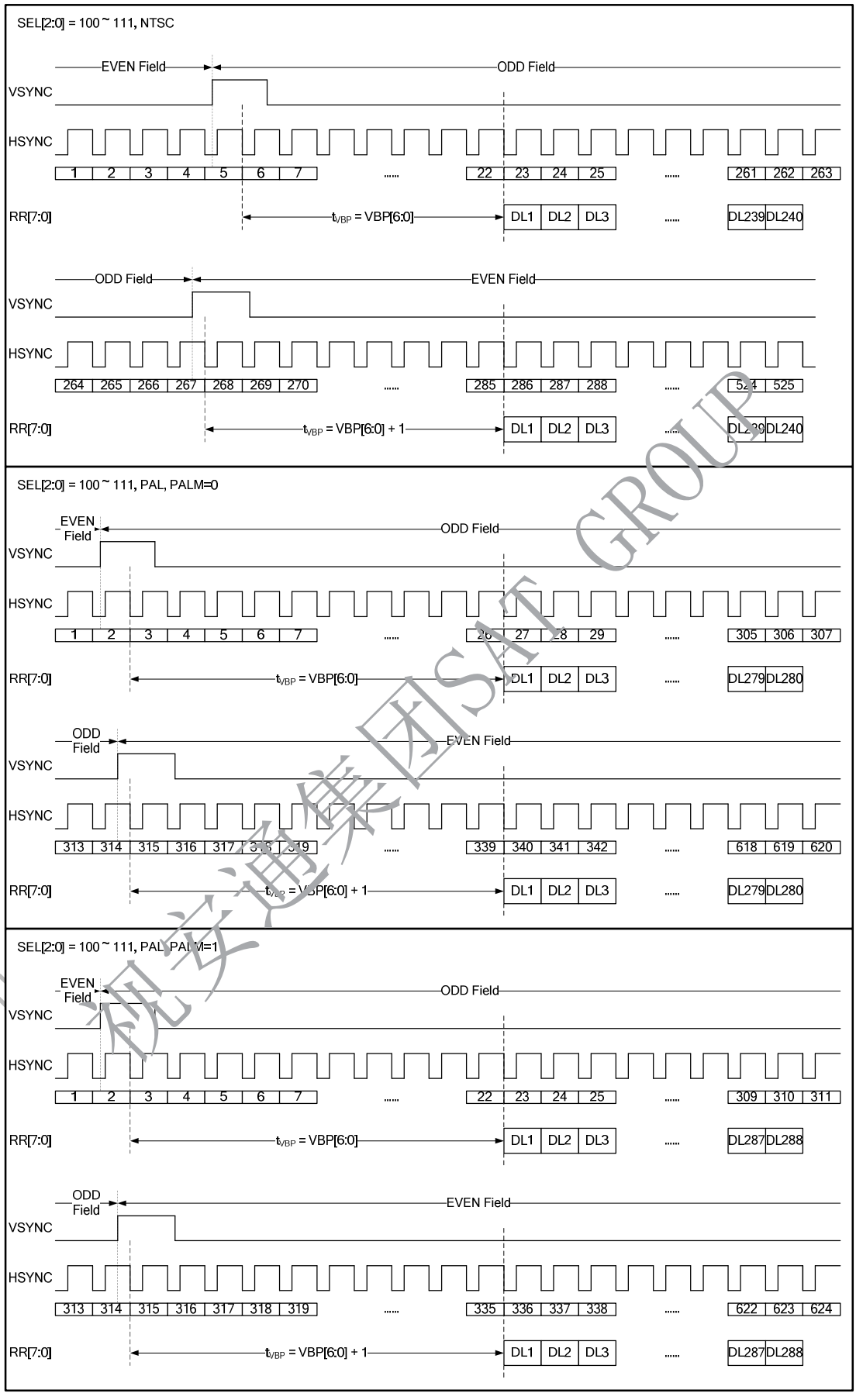


Figure 12. 7 CCIR601 Vertical Timing

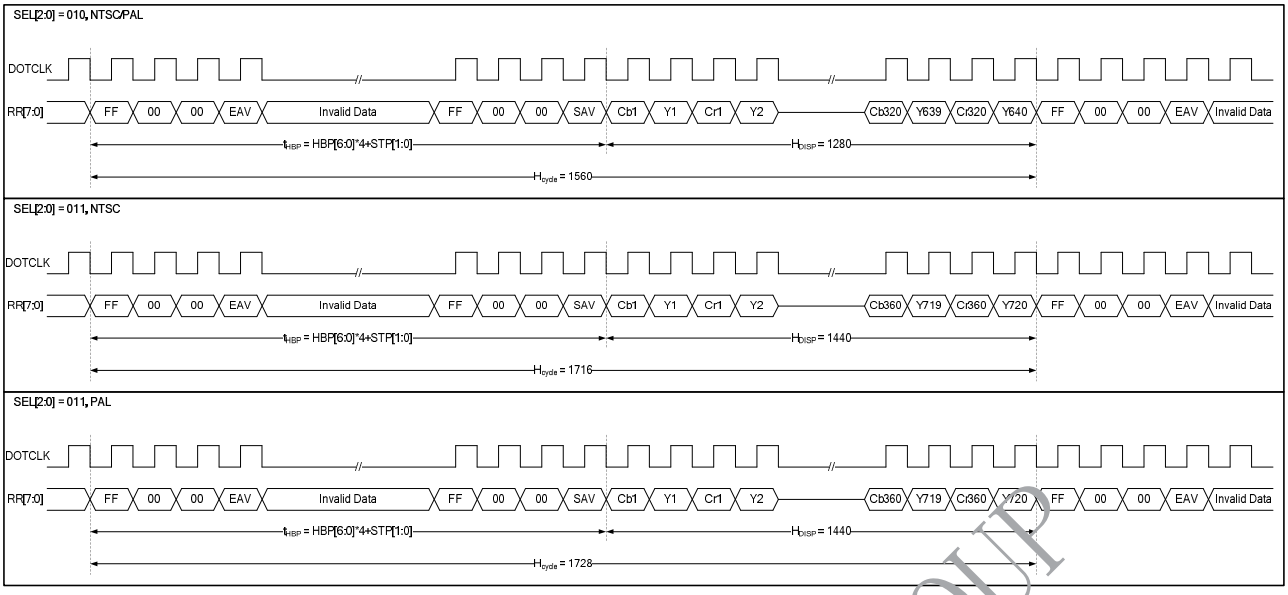


Figure 12. 8 CCIR656 Horizontal Timing

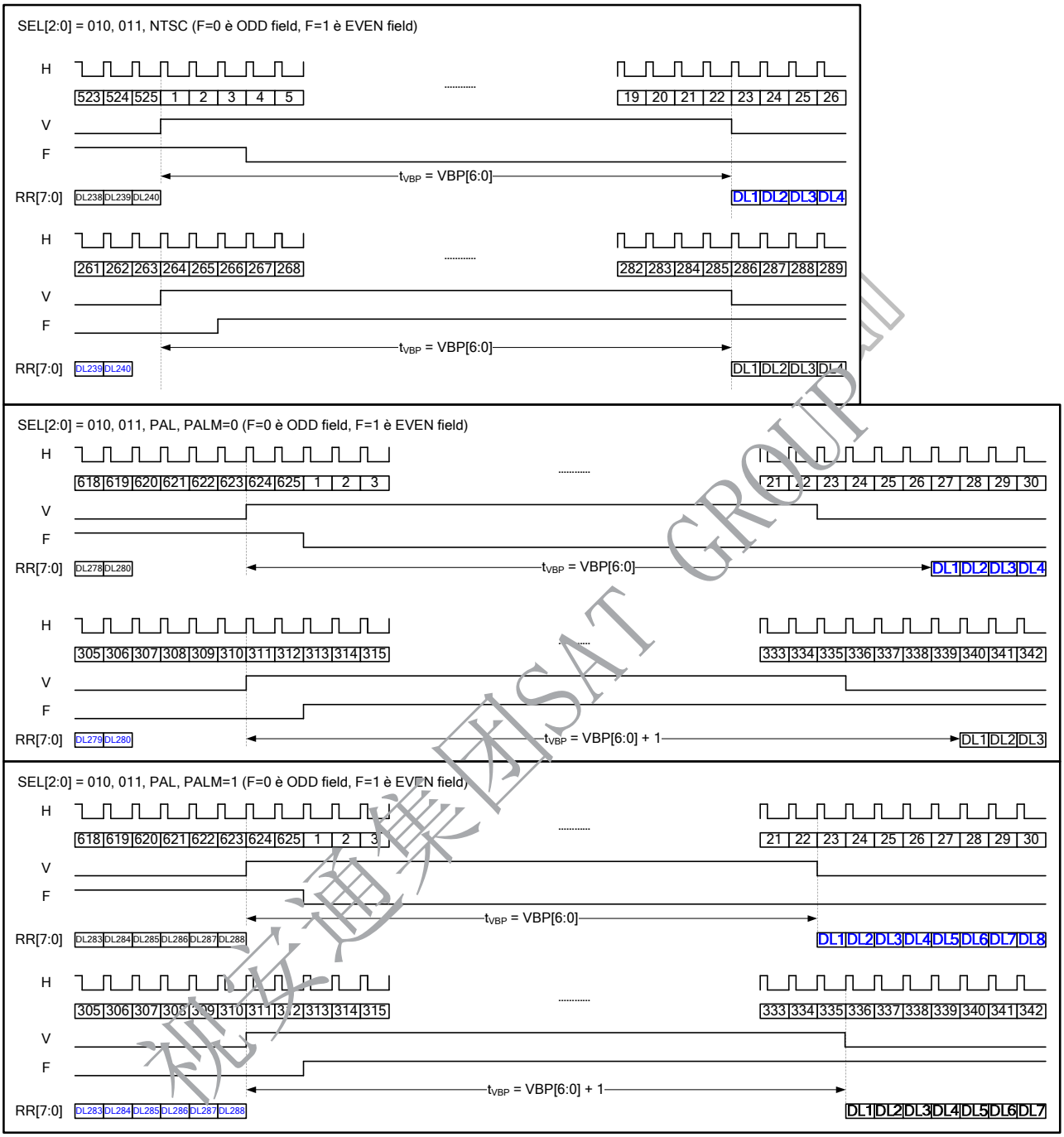
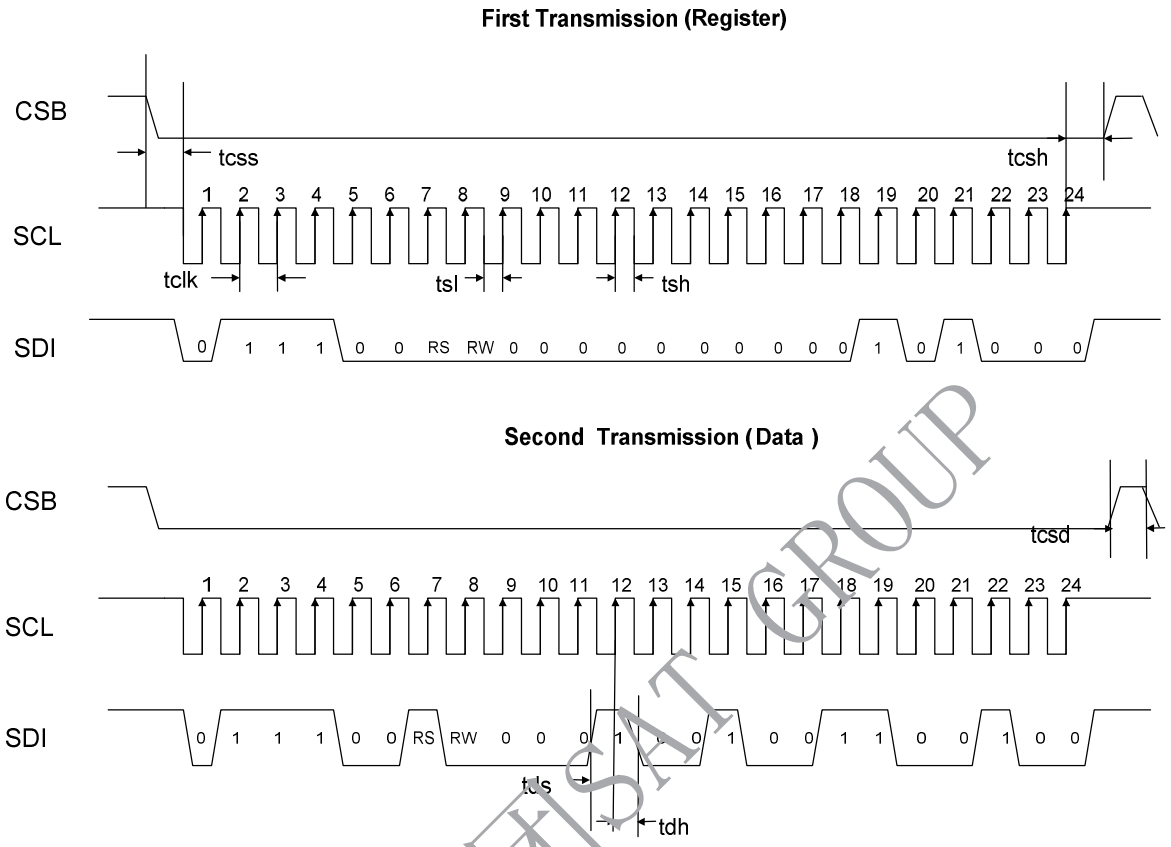


Figure 12. 9 CCIR656 Vertical Timing

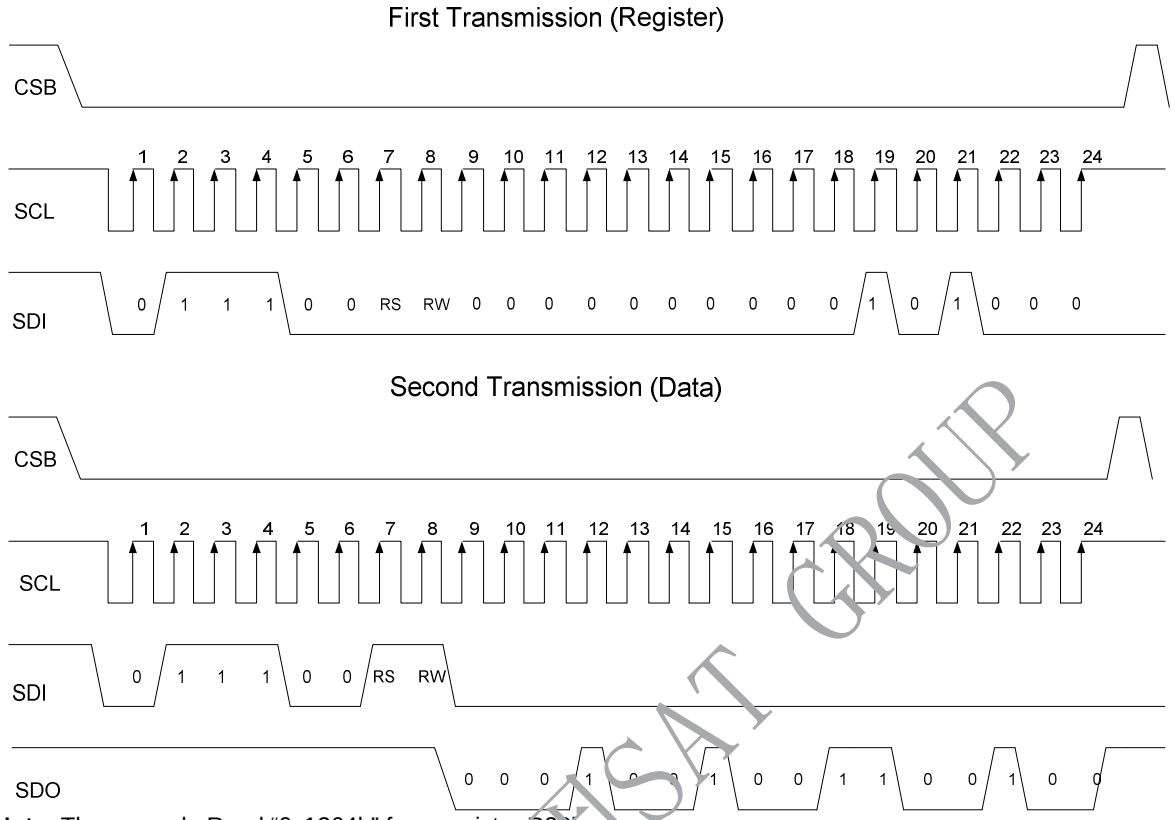
- Write SPI



Note: The example writes “0x1264h” to register R23h.
SPID connected to VSS.

Figure 12. 12 (a) SPI Interface Timing Diagram & Write SPI Example

- Read SPI



Note: The example Read "0x1264h" from register R28h.

Figure 12. 13 (b) SPI interface Timing Diagram & Read SPI Example

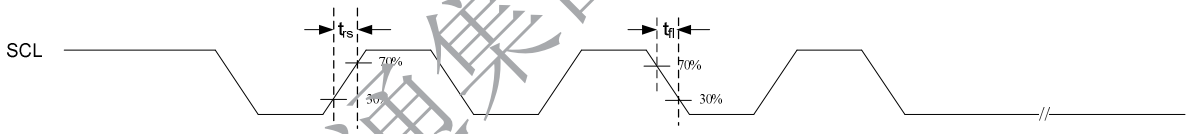


Figure 12. 14 Rising/Falling Time

Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Clock Rising Time	trs	-	-	30	ns
Clock Falling Time	tfl	-	-	30	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

Table 12. 5 SPI Timing

4. Optical Specifications

Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing angle (CR≥ 10)		θ_L	Φ=180°(9 o'clock)	50	60	-	degree	Note 1
		θ_R	Φ=0°(3 o'clock)	50	60	-		
		θ_T	Φ=90°(12 o'clock)	40	50	-		
		θ_B	Φ=270°(6 o'clock)	45	55	-		
Response time		T_{ON}	Normal θ=Φ=0°	-	10	-	msec	Note 3
		T_{OFF}		-	15	-		
Contrast ratio		CR		300	400	-	-	Note 4
Color Chromaticity	White	W_X		0.269	0.279	0.299	-	Note 2 Note 5 Note 6
		W_Y		0.292	0.302	0.322	-	
	Red	R_X		0.609	0.639	0.669	-	
		R_Y		0.314	0.344	0.374	-	
	Green	G_X		0.264	0.294	0.324	-	
		G_Y		0.557	0.587	0.617	-	
	Blue	B_X		0.102	0.132	0.162	-	
		B_Y		0.106	0.136	0.166	-	
Luminance		L		360	410	--	cd/m^2	Note 6
Luminance uniformity		Y_U		75	80	--	%	Note 7

Test Conditions:

1. DV_{DD}=3.3V, I_L =20mA(Backlight current),the amblent temperature is 25℃.
2. The test systems refer to Note 2.

5. Mechanical Drawing