SPECIFICATION

Customer: _____

Model Name: SAT050AT40D12B2-30076T051ZD

SPEC NO.: _____

Date: _____

Version: _____

■ **Preliminary Specification**

□ **Final Specification**

Approved by	Comment

Prepared by	Reviewed by	Approved by

Record of Revision

Version	Revise Date	Page	Content
Pre-spec.A	2014/08/22		Initial Release

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1. General Specifications

No.	Item	Specification	Remark
1	LCD Size	5.0 inch(Diagonal)	
2	Driver element	a-Si TFT active matrix	
3	Resolution	480 × 3(RGB) ×272	
4	Display mode	Normally White, Transmissive	
5	Dot pitch	0.066(W) X 0.198(H) mm	
6	Active area	110.880(W) X 3(RGB) X 62.832(H) mm	
7	Outline dimensions	120.7(H) X 75.8(V) X 3.0(D) mm	
8	Surface treatment	Anti-Glare	
9	Color arrangement	RGB-stripe	
10	Interface	TTL RGB-24bit parallel interface	
11	Backlight Power consumption	TBD	
12	Panel Power consumption	TBD	
13	Weight	TBD	

2. Pin Assignment

FPC connector is used for electronics interface. The recommended model is FH19SC-40S-0.5SH (05) manufactured by HIROSE.

No.	Symbol	I/O	Function
1	VLED-	P	Power for LED backlight cathode
2	VLED+	P	Power for LED backlight anode
3	GND	P	Power ground
4	VDD	P	Power voltage
5	R0	I	Red data (LSB)
6	R1	I	Red data
7	R2	I	Red data
8	R3	I	Red data
9	R4	I	Red data
10	R5	I	Red data
11	R6	I	Red data
12	R7	I	Red data (MSB)
13	G0	I	Green data (LSB)
14	G1	I	Green data
15	G2	I	Green data
16	G3	I	Green data
17	G4	I	Green data
18	G5	I	Green data
19	G6	I	Green data
20	G7	I	Green data (MSB)
21	B0	I	Blue data (LSB)
22	B1	I	Blue data
23	B2	I	Blue data
24	B3	I	Blue data
25	B4	I	Blue data
26	B5	I	Blue data
27	B6	I	Blue data
28	B7	I	Blue data (MSB)
29	GND	P	Power ground
30	DCLK	I	Pixel clock
31	DISP	I	Display on/ off
32	HSYNC	I	Horizontal sync signal
33	VSYNC	I	Vertical sync signal
34	DE	I	Data enable
35	NC	-	No connect
36	GND	P	Power ground
37	X_R	I/O	Right electrode - differential analog

38	Y_B	I/O	Bottom electrode - differential analog
39	X_L	I/O	Left electrode - differential analog
40	Y_T	I/O	Top electrode - differential analog

I/O: I: input, O: output, P: power

3. Operation Specifications

3.1. Absolute Maximum Ratings

(Note 1)

Item	Symbol	Values		Unit	Remark
		Min.	Max.		
Supply voltage	V_{DD}	-0.3	4.5	V	
Operation Temperature	T_{OP}	-20	70	℃	
Storage Temperature	T_{ST}	-30	80	℃	

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

3.1.1. Typical Operation Conditions

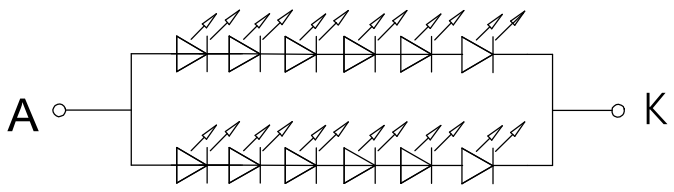
Item	Symbol	Values			Unit	Remark
		Min.	Typ	Max.		
Power voltage	V_{DD}	3.0	3.3	3.6	V	Note 2
Current for Driver	IV_{DD}	-	17	25	mA	
Input logic high voltage	V_{IH}	0.8 V_{DD}	-	V_{DD}	V	Note 3
Input logic low voltage	V_{IL}	0	-	0.2 V_{DD}	V	

3.1.2. Backlight Driving Conditions (12 White Chips)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage of white LED backlight	VL	17.4	19.8	21	V	Note 1
Current for LED backlight	IL	30	40	50	mA	
Luminance (on the module surface,BM-7)		300	350	-	cd/m^2	
LED life time	-	50,000	-	-	Hr	Note 2

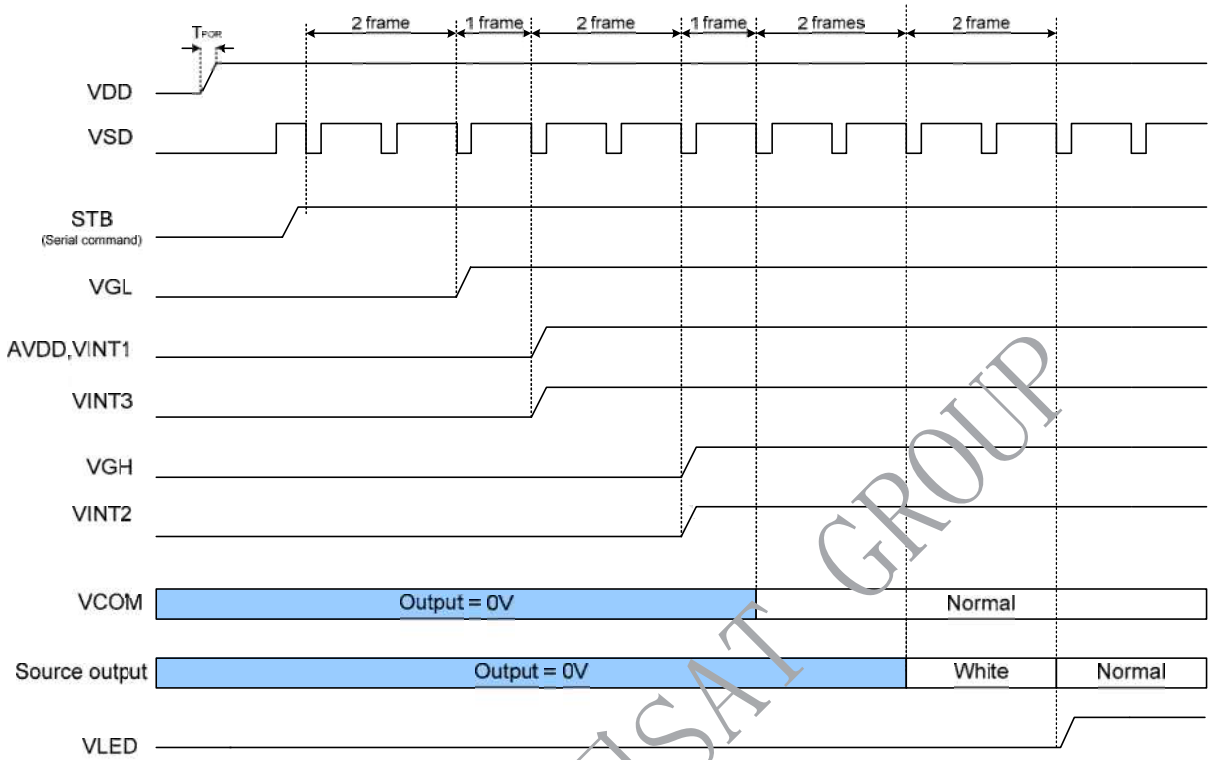
Note 1: The LED Supply Voltage is defined by the number of LED at Ta=25℃ and I_L=40mA.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and I_L=40mA. The LED lifetime could be decreased if operating I_L is lager than 40mA.

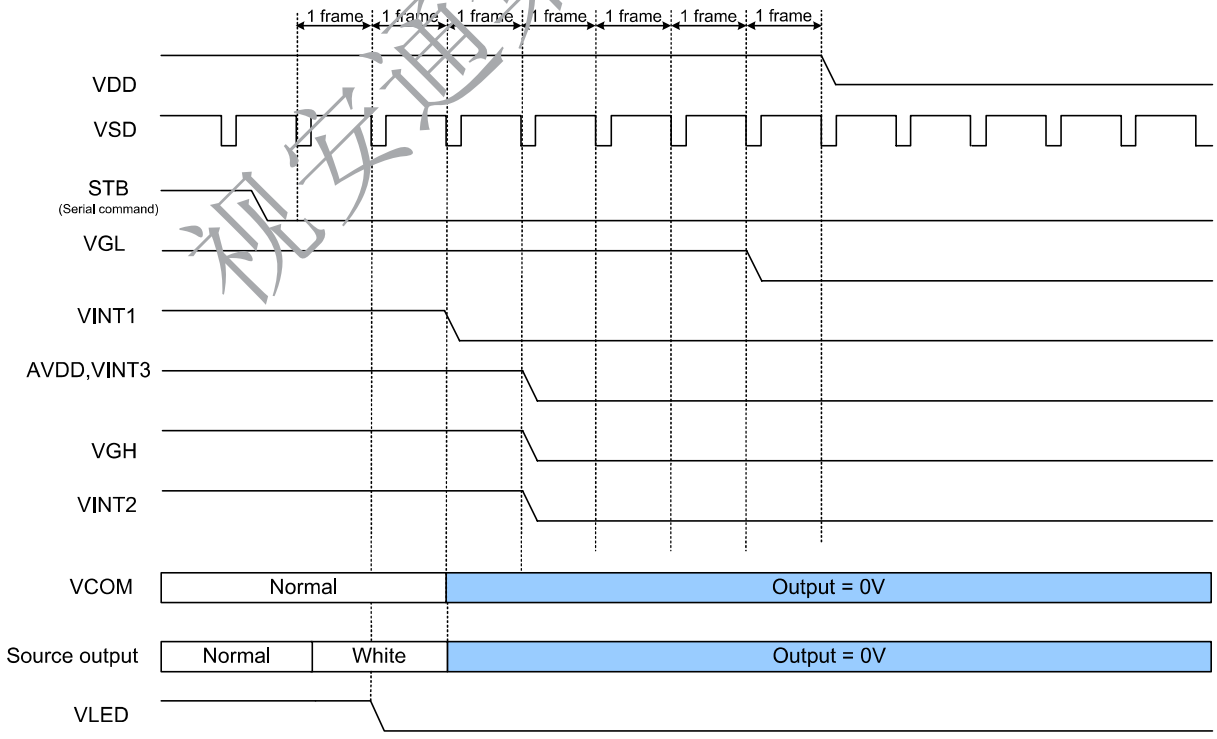


3.2. Power Sequence

Power On Sequence



Power Off Sequence



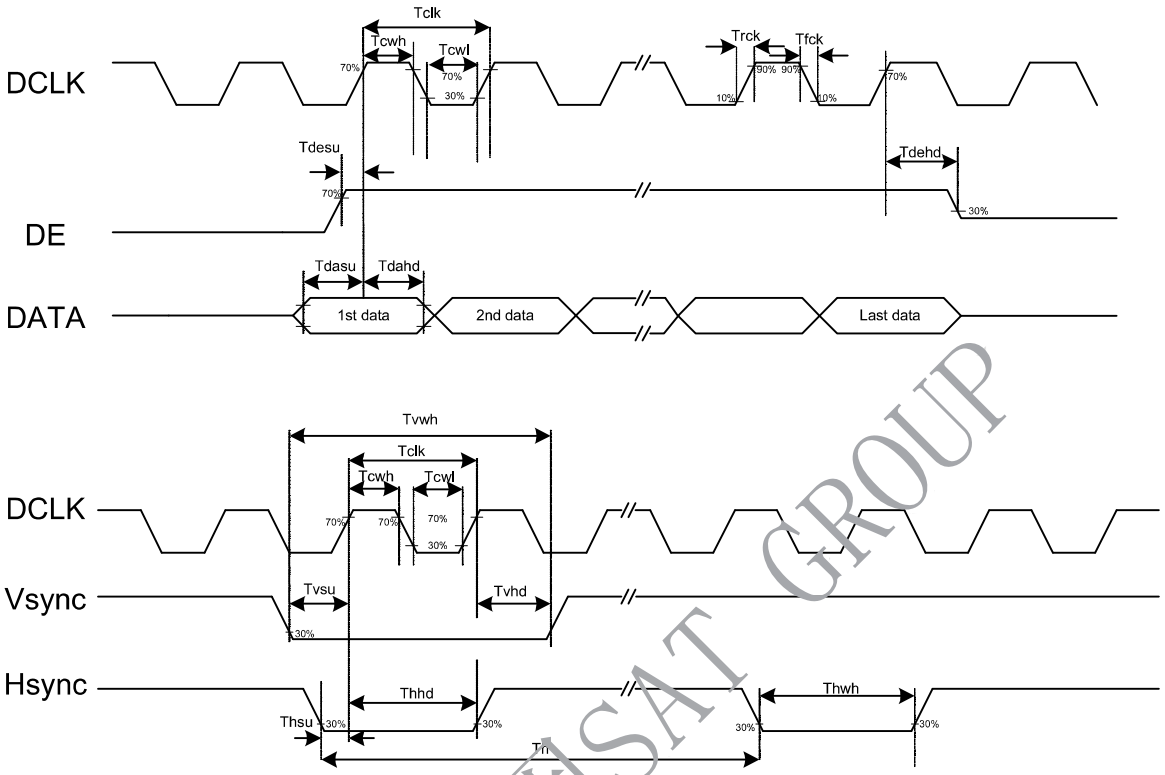
3.3. Timing Characteristics

3.3.1. AC Electrical Characteristics

AC Electrical Characteristics (VDDIO=VDD=3.0 to 3.6v, GND=0V, TA=-20 to +85 ℃)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
System operation timing						
VDD power source slew time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB pulse width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
Input Output timing						
DCLK clock time	Tclk	33.3	-	-	ns	DCLK=30MHz
DCLK clock low period	Tcwl	40	-	60	%	
DCLK clock high period	Tcwh	40	-	60	%	
Clock rising time	Trck	9	-	-	ns	
Clock falling time	Tfck	9	-	-	ns	
HSD width	Thwh	1	-	-	DCLK	
HSD period time	Th	55	60	65	us	
HSD setup time	Thsu	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
VSD width	Tvwh	1	-	-	Th	
VSD setup time	Tvsu	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
Data setup time	Tdasu	12	-	-	ns	
Data hold time	Tdahd	12	-	-	ns	
DE setup time	Tdesu	12	-	-	ns	
DE hold time	Tdehd	12	-	-	ns	
Source output setting time	Tsst	-	-	TBD	us	10% to 90% CL=60pF, RL=2Kohm
Gate output setting time	Tgst	-	-	TBD	ns	10% to 90%, CL=60pF
VCOM output setting time	Tcst	-	-	TBD	us	10% to 90%, CL=40nF, RL=50ohm
Time from VSD to 1st line data input	Tvs	3	8	31	Th	HV mode By HDL[4:0] setting
3-wire serial communication AC timing						
Serial clock	Tsck	200	-	-	ns	For SCL pin
SCL pulse low period	Tckl	40	-	60	%	
SCL pulse low period	Tckh	40	-	60	%	
Serial data setup time	Tisu	50	-	-	ns	
Serial data hold time	Tihd	50	-	-	ns	
Serial clock high/low	Tssw	50	-	-	ns	
CSB to VSD	Tcv	1			us	
CSB distinguish time	Tcd	400	-	-	ns	
CSB input setup time	Tcsu	50	-	-	ns	
CSB input hold time	Tchd	50	-	-	ns	

3.3.2. Input Clock and Data Timing Diagram



3.3.3. Timing

Vertical input timing

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
DCLK frequency	Fclk	24	27	30	MHz	
DCLK cycle time	Tclk	83	110	200	ns	
DCLK pulse duty	Tcwh	40	50	60	%	
Time from HSD to source output	Thso	-	13	-	DCLK	
Time from HSD to gate output	Thgo	-	27	-	DCLK	
Time from HSD to gate output off	Thgz	-	3	-	DCLK	
Time from HSD to VCOM	Thvc	-	12	-	DCLK	

Parallel RGB input timign table

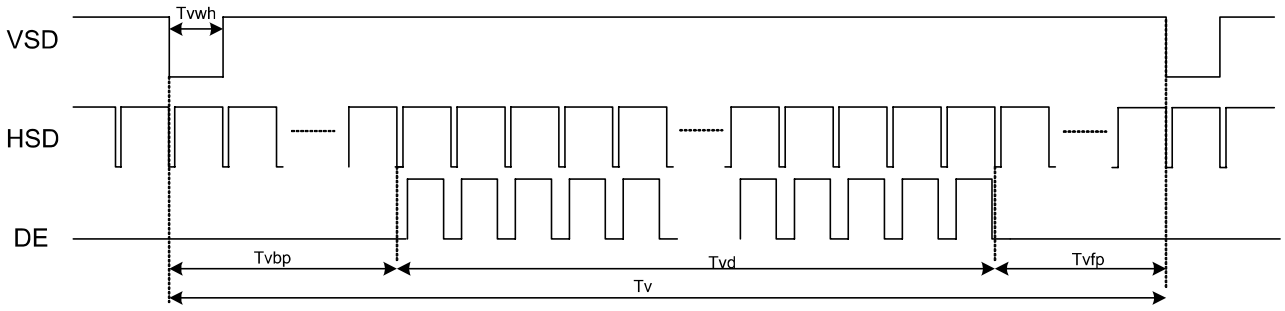
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	5	9	12	MHz
VSD period time	Tv	277	288	400	H
VSD display area	Tvd		272		H
VSD back porch	Tvb	3	8	31	H
VSD front porch	Tvfp	2	8	93	H
HSD period time	Th	520	525	800	DCLK
HSD display area	Thd		480		DCLK
HSD back porch	Thbp	36	40	255	DCLK
HSD front porch	Thfp	4	5	65	DCLK

Serial RGB input timign table

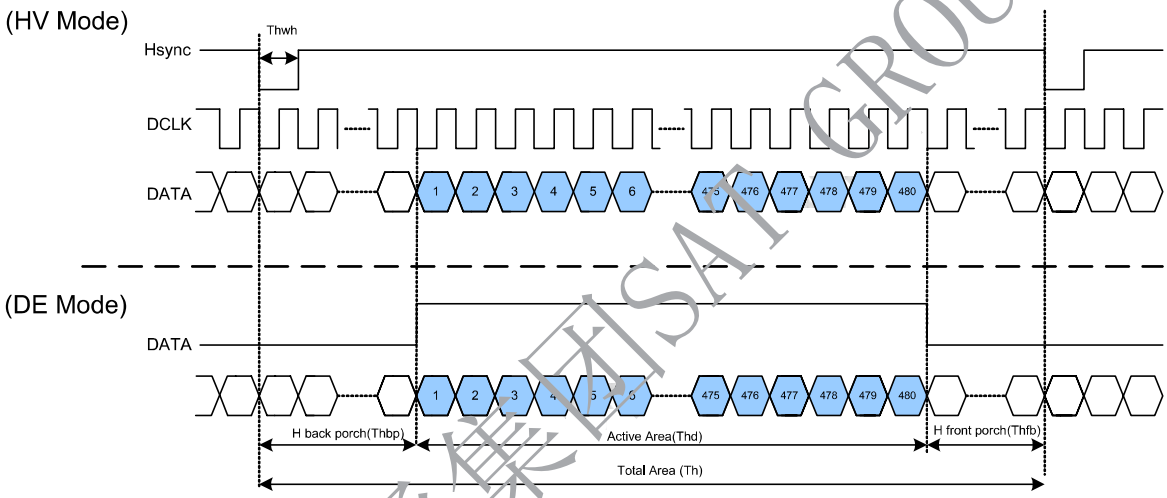
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	-	27	-	MHz
VSD period time	Tv	277	288	400	H
VSD display area	Tvd		272		H
VSD back porch	Tvb	3	8	31	H
VSD front porch	Tvfp	2	8	93	H
HSD period time	Th	-	1575	-	DCLK
HSD display area	Thd		1440		DCLK
HSD back porch	Thbp	-	120	-	DCLK
HSD front porch	Thfp	-	15	-	DCLK

3.3.4. Data Input Format

Vertical input timing

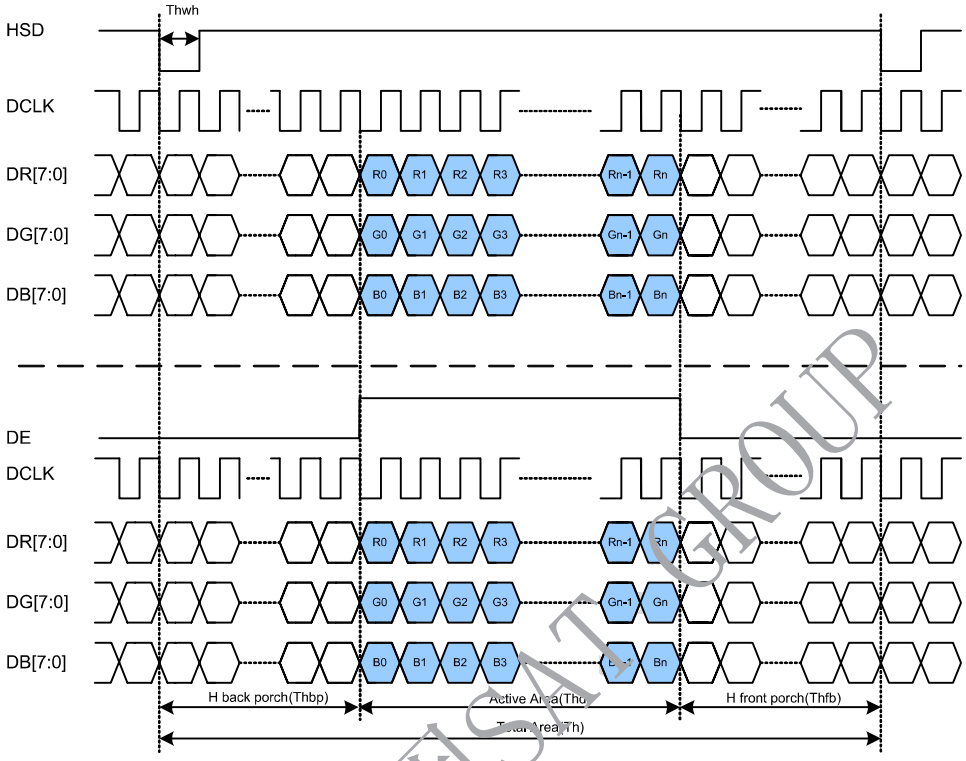


Serial 8-bit RGB Mode Data format



Parallel RGB Mode Data format

(HV Mode)



(DE Mode)

4. Optical Specifications

Ta=25 ℃

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	30	40	--	Degree	Note1
		θB		40	50	--		
		θL		40	50	--		
		θR		40	50	--		
Contrast Ratio		CR	θ=0°	350	500	--		Note4
Response Time		T_{ON}	25℃	–	25	40	ms	Note3
		T_{OFF}						
Chromaticity	White	x	Backlight is on	0.278	0.288	0.308		Note2 Note5 Note6
		y		0.309	0.329	0.349		
	Red	x		0.585	0.605	0.625		
		y		0.311	0.331	0.351		
	Green	x		0.269	0.289	0.309		
		y		0.526	0.546	0.566		
	Blue	x		0.121	0.141	0.161		
		y		0.109	0.129	0.149		
Uniformity		U		75	80	--	%	Note7
NTSC				–	50	--	%	
Luminance		L		300	350	--	cd/m^2	Note6

Test Conditions:

1. DV_{DD}=3.3V, I_L=40mA(Backlight current),the amblent temperature is25 ℃.
2. The test systems refer to Note 2.

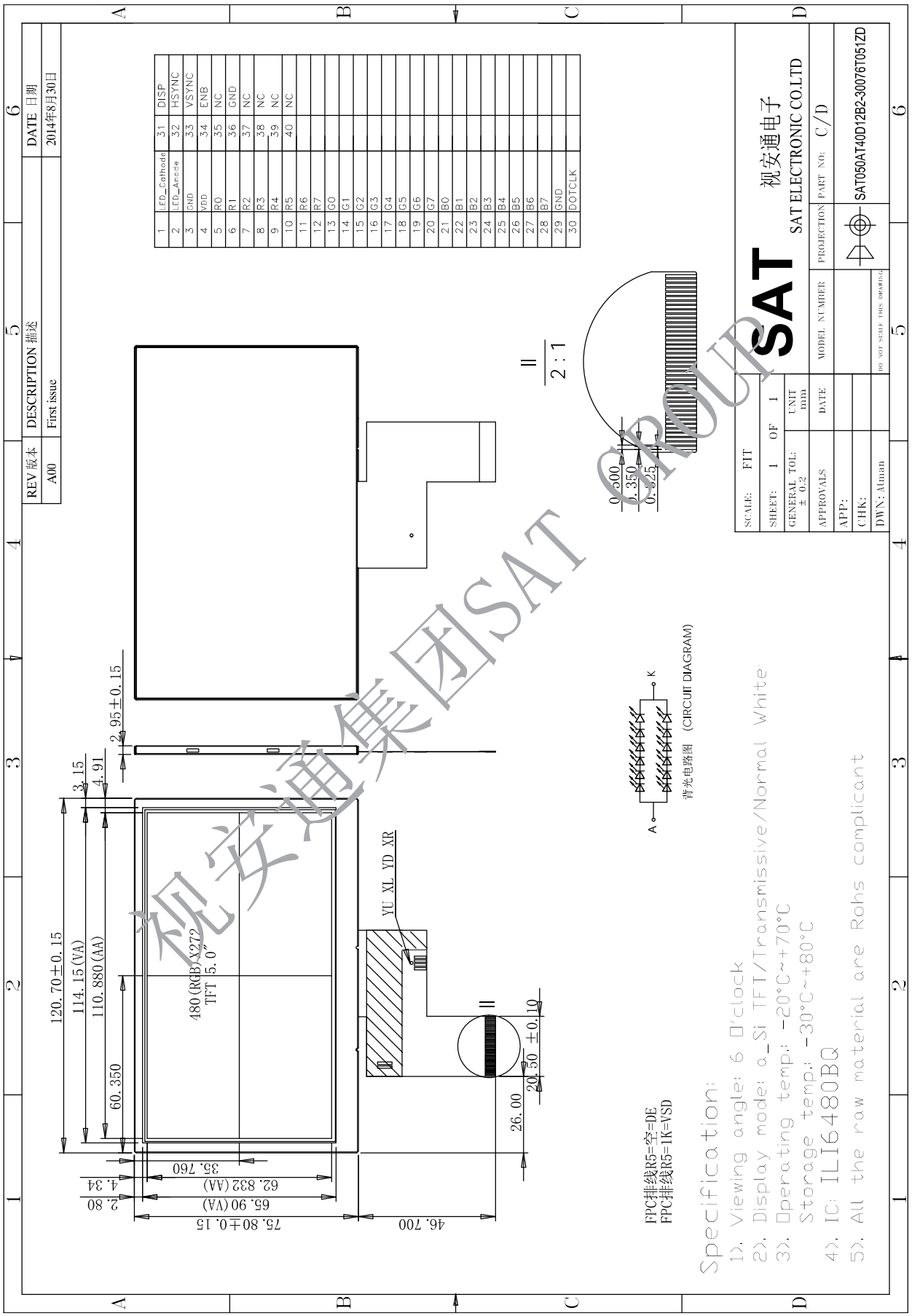
5. Reliability Test Items

(Note3)

Item	Test Conditions	Remark
High Temperature Storage	Ta = 80℃ 240hrs	Note 1，Note 4
Low Temperature Storage	Ta = -30℃ 240hrs	Note 1，Note 4
High Temperature Operation	Ts = 70℃ 240hrs	Note 2，Note 4
Low Temperature Operation	Ta = -20℃ 240hrs	Note 1，Note 4
Operate at High Temperature and Humidity	+60℃, 90%RH 240hrs	Note 4
Thermal Shock	-30℃/30 min ~ +80℃/30 min for a total 100 cycles, Start with cold temperature and end with high temperature.	Note 4
Vibration Test	Frequency range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total)	
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	
Package Vibration Test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	
Package Drop Test	Height:60 cm 1 corner, 3 edges, 6 surfaces	
Electro Static Discharge	Contact:±6KV,Air:±8KV 150pF，330Ω，	Note 5

Note 1: Ta is the ambient temperature of samples.
Note 2: Ts is the temperature of panel's surface.
Note 3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.
Note 4: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.
Note 5: LCD glass and metal bezel .

6. Mechanical Drawing



1	LED_Cathode	31 DISP
2	LED_Anode	32 HSYNC
3	GND	33 VSYNC
4	VDD	34 ENB
5	R0	35 NC
6	R1	36 GND
7	R2	37 NC
8	R3	38 NC
9	R4	39 NC
10	R5	40 NC
11	R6	
12	R7	
13	G0	
14	G1	
15	G2	
16	G3	
17	G4	
18	G5	
19	G6	
20	G7	
21	B0	
22	B1	
23	B2	
24	B3	
25	B4	
26	B5	
27	B6	
28	B7	
29	GND	
30	DOTCLK	

7. Package Drawing