

SPECIFICATION

Customer: _____
Model Name: SAT043CP40D08Y0-30671T051KN
SPEC NO.: _____
Date: _____
Version: _____

- Preliminary Specification
 Final Specification

| Approved by | Comment |
|-------------|---------|
| | |

| RePrepared by | Reviewed by | Approved by |
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Record of Revision

| Version | Revise Date | Page | Content |
|------------|-------------|------|-----------------|
| Pre-spec.A | 2016/12/06 | | Initial Release |

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1. General Specifications

| No. | Item | Specification | Remark |
|-----|-----------------------------|----------------------------------|--------|
| 1 | LCD Size | 4.3 inch(Diagonal) | |
| 2 | Driver element | a-Si TFT active matrix | |
| 3 | Resolution | 480 × 3(RGB) × 272 | |
| 4 | Display mode | Normally White, Transmissive | |
| 5 | Dot pitch | 0.066(W) X 0.198(H) mm | |
| 6 | Active area | 95.04(W) X 3(RGB) X 53.856(H) mm | |
| 7 | Outline dimensions | 105.5(H) X 67.1(V) X 3.0(D) mm | |
| 8 | Surface treatment | Anti-Glare | |
| 9 | Color arrangement | RGB-stripe | |
| 10 | Interface | TTL RGB-24bit parallel interface | |
| 11 | Backlight Power consumption | TBD | |
| 12 | Panel Power consumption | TBD | |
| 13 | Weight | TBD | |

2. Pin Assignment

FPC connector is used for electronics interface. The recommended model is FH19SC-40S-0.5SH (05) manufactured by HIROSE.

| No. | Symbol | I/O | Function |
|-----|--------|-----|---------------------------------------|
| 1 | VLED- | P | Power for LED backlight cathode |
| 2 | VLED+ | P | Power for LED backlight anode |
| 3 | GND | P | Power ground |
| 4 | VDD | P | Power voltage |
| 5 | R0 | I | Red data (LSB) |
| 6 | R1 | I | Red data |
| 7 | R2 | I | Red data |
| 8 | R3 | I | Red data |
| 9 | R4 | I | Red data |
| 10 | R5 | I | Red data |
| 11 | R6 | I | Red data |
| 12 | R7 | I | Red data (MSB) |
| 13 | G0 | I | Green data (LSB) |
| 14 | G1 | I | Green data |
| 15 | G2 | I | Green data |
| 16 | G3 | I | Green data |
| 17 | G4 | I | Green data |
| 18 | G5 | I | Green data |
| 19 | G6 | I | Green data |
| 20 | G7 | I | Green data (MSB) |
| 21 | B0 | I | Blue data (LSB) |
| 22 | B1 | I | Blue data |
| 23 | B2 | I | Blue data |
| 24 | B3 | I | Blue data |
| 25 | B4 | I | Blue data |
| 26 | B5 | I | Blue data |
| 27 | B6 | I | Blue data |
| 28 | B7 | I | Blue data (MSB) |
| 29 | GND | P | Power ground |
| 30 | DCLK | I | Pixel clock |
| 31 | DISP | I | Display on/ off |
| 32 | HSYNC | I | Horizontal sync signal |
| 33 | VSYNC | I | Vertical sync signal |
| 34 | DE | I | Data enable |
| 35 | NC | - | No connect |
| 36 | GND | P | Power ground |
| 37 | X_R | I/O | Right electrode - differential analog |

| | | | |
|----|-----|-----|--|
| 38 | Y_B | I/O | Bottom electrode - differential analog |
| 39 | X_L | I/O | Left electrode - differential analog |
| 40 | Y_T | I/O | Top electrode - differential analog |

I/O: I: input, O: output, P: power

3. Operation Specifications

3.1. Absolute Maximum Ratings

(Note 1)

| Item | Symbol | Rating | Unit |
|-----------------------------|--------|-------------------|------|
| Power Supply Voltage | VDD | - 0.3 ~ +4.6 | V |
| IO Supply Voltage | VDDI | - 0.3 ~ +4.6 | V |
| Charge Pump Supply Voltage | PVDD | - 0.3 ~ +4.6 | V |
| Logic Input Voltage Range | VIN | -0.3 ~ VDDI + 0.3 | V |
| Logic Output Voltage Range | VO | -0.3 ~ VDDI + 0.3 | V |
| Operating Temperature Range | TOPR | -20 ~ + 70 | °C |
| Storage Temperature Range | TSTG | -30 ~ +80 | °C |

Note 1: The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.

3.1.1. Typical Operation Conditions

| Parameter | Symbol | Value | Unit | Remarks |
|------------------------------|----------|---------|------|---------|
| POWER SUPPLY | VDD/PVDD | 3.3 | V | |
| TFT Gate ON Voltage | VGH | 15 | V | |
| TFT Gate OFF Voltage | VGL | -7~ -10 | V | |
| TFT Common Electrode Voltage | VCOMH | / | V | |
| | VCOML | / | V | |

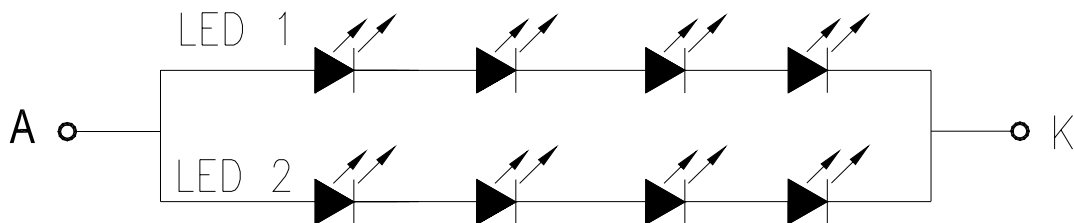
Notes :

1. VGH is TFT Gate operating voltage.
2. VGL is TFT Gate operating voltage. The low voltage level of VGL signal must be fluctuates with same phase as Vcom.
3. Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc..

different D-IC.

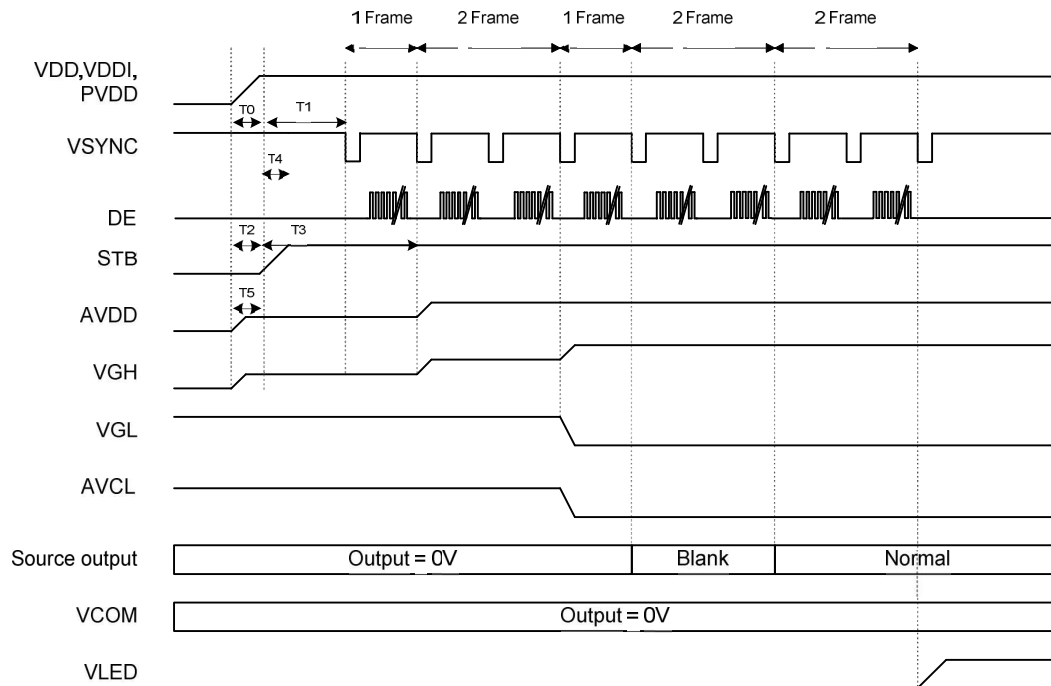
3.1.2. Backlight Driving Conditions (8 White Chips)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|--|--------|--------|------|------|-------------------|--------|
| Supply voltage of white LED backlight | VL | 12 | 13.2 | 14 | V | Note 1 |
| Current for LED backlight | IL | 30 | 40 | 50 | mA | |
| Luminance (on the module surface, BM-7) | | 330 | 380 | - | cd/m ² | |
| LED life time | - | 50,000 | - | - | Hr | Note 2 |



3.2. Power Sequence

Power On Sequence



| | Description | Min. Time |
|----|--|------------------|
| T0 | Determined by the external power | |
| T1 | Time from stable VDD, VDDI, PVDD set-up to the first VSYNC | T1=0 |
| T2 | Time from AVDD=0V to AVDD=3.3V | T2=T0 |
| T3 | Time from AVDD=3.3V to AVDD=6.0V | T3=T1+ (1*Frame) |
| T4 | Time from stable VDD, VDDI, PVDD set-up to DISP asserted | T4=0 |
| T5 | Time from VGH=0V to VGH=3.3V | T5=T0 |

3.3. Timing Characteristics

3.3.1 RGB Timing Table

Parallel 24-bit RGB Timing Table

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remark |
|----------------|----------------|--------|------|------|------|------|-----------------------|
| DCLK Frequency | | Fclk | 8 | 9 | 12 | MHz | |
| DCLK Period | | Tclk | 83 | 111 | 125 | Ns | |
| HSYNC | Period Time | Th | 485 | 531 | | DCLK | |
| | Display Period | Thdisp | | 480 | | DCLK | |
| | Back Porch | Thbp | 3 | 43 | | DCLK | By H_Blanking setting |
| | Front Porch | Thfp | 2 | 8 | | DCLK | |
| | Pulse Width | Thw | 2 | 4 | | DCLK | |
| VSYNC | Period Time | Tv | 276 | 292 | | H | |
| | Display Period | Tvdisp | | 272 | | H | |
| | Back Porch | Tvbp | 2 | 12 | | H | By V_Blanking setting |
| | Front Porch | Tvfp | 2 | 8 | | H | |
| | Pulse Width | Tvw | 2 | 4 | | H | |

Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

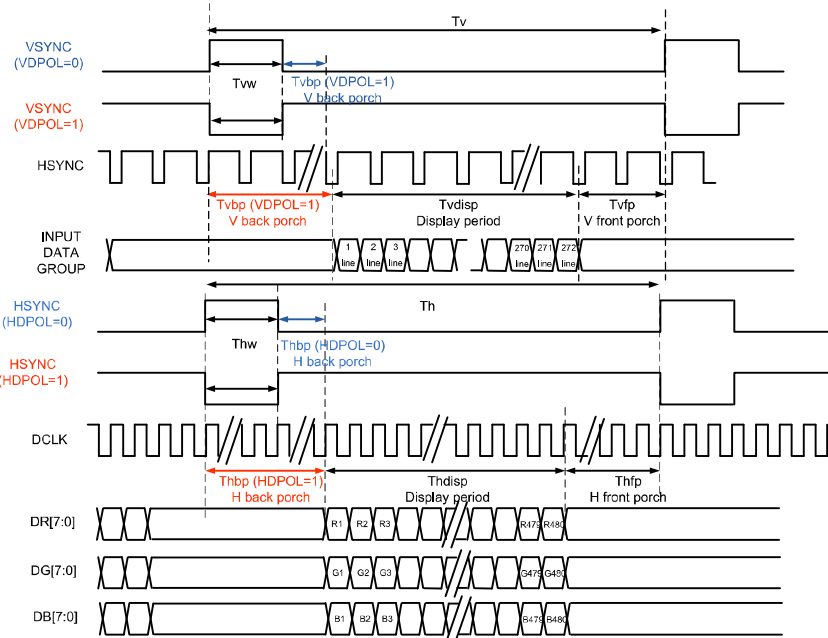
Serial 8-bit RGB Timing Table

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remark |
|----------------|----------------|--------|------|------|------|------|-----------------------|
| DCLK Frequency | | Fclk | 24 | 27 | 30 | MHz | |
| DCLK Period | | Tclk | 33 | 37 | 42 | Ns | |
| HSYNC | Period Time | Th | 1445 | 1491 | | DCLK | |
| | Display Period | Thdisp | | 1440 | | DCLK | |
| | Back Porch | Thbp | 3 | 43 | | DCLK | By H_Blanking setting |
| | Front Porch | Thfp | 2 | 8 | | DCLK | |
| | Pulse Width | Thw | 2 | 4 | | DCLK | |
| VSYNC | Period Time | Tv | 276 | 292 | | H | |
| | Display Period | Tvdisp | | 272 | | H | |
| | Back Porch | Tvbp | 2 | 12 | | H | By V_Blanking setting |
| | Front Porch | Tvfp | 2 | 8 | | H | |
| | Pulse Width | Tvw | 2 | 4 | | H | |

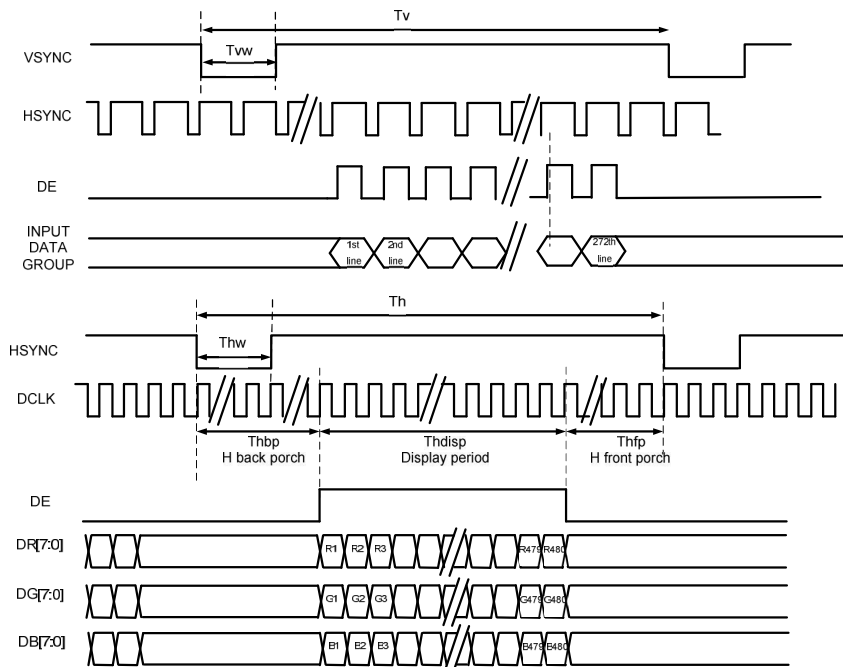
Note: It is necessary to keep Tvbp =12 and Thbp =43 in sync mode. DE mode is unnecessary to keep it.

3.3.2 Timing Diagram

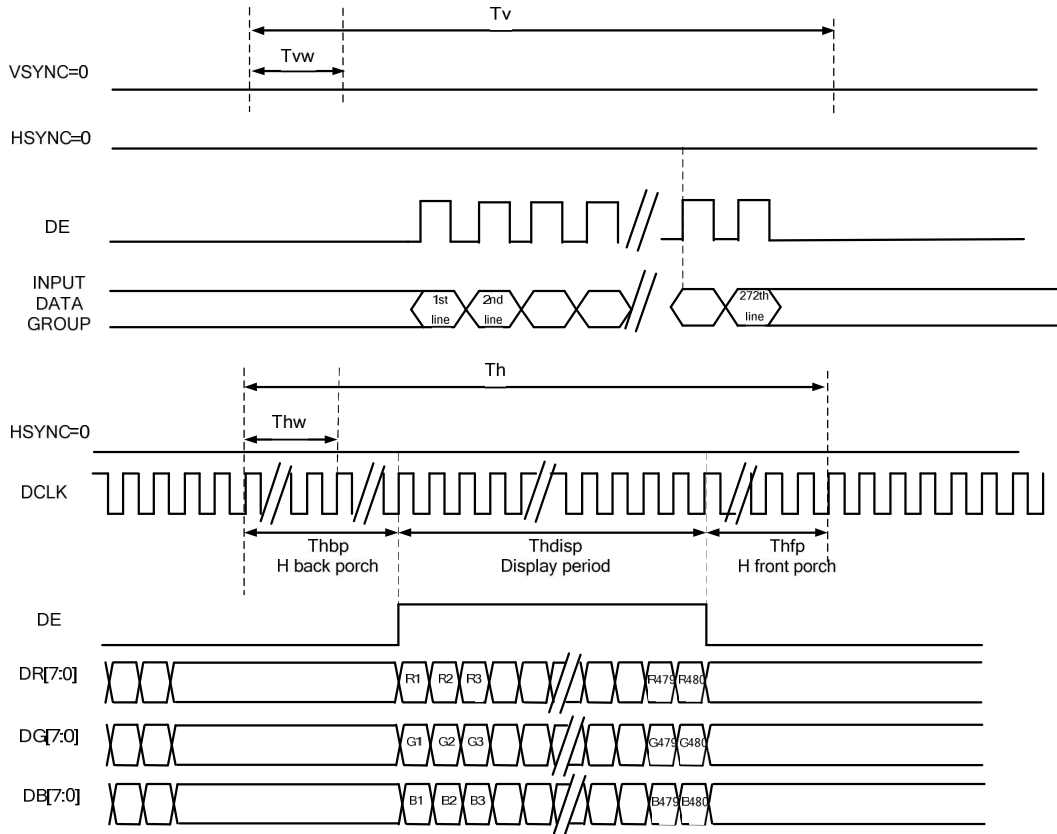
SYNC Mode Timing Diagram



SYNC-DE Mode Timing Diagram



DE Mode Timing Diagram



4. Optical Specifications

Ta=25 °C

| ITEM | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT | REMARK |
|--|------------|---|---------------------------|-------|-------|-------|--------|
| Transmittance | T | | 6.0 | 6.4 | | % | Note 2 |
| Contrast Ratio | CR | *1) | 250 | 350 | -- | -- | Note 3 |
| Response Time | Tr+ Tf | *3) | - | 30 | 45 | ms | Note 4 |
| Viewing Angle | Vertical | $\theta^{*2)}$ $\psi^{*2)}$ $CR \geq 10$ | 90 | 110 | -- | | Note 5 |
| | | | | | -- | | |
| | Horizontal | | 110 | 130 | -- | | |
| | | | | | -- | | |
| Color Filter Chromacicity with C light | White | x y | $\theta = \phi = 0^\circ$ | 0.263 | 0.278 | 0.293 | Note 6 |
| | | | | 0.290 | 0.305 | 0.320 | |
| | Red | x y | $\theta = \phi = 0^\circ$ | 0.589 | 0.609 | 0.629 | |
| | | | | 0.297 | 0.317 | 0.337 | |
| | Green | x y | $\theta = \phi = 0^\circ$ | 0.297 | 0.317 | 0.337 | |
| | | | | 0.523 | 0.543 | 0.563 | |
| | Blue | x y | $\theta = \phi = 0^\circ$ | 0.117 | 0.137 | 0.157 | |
| 0.141 | | | | 0.161 | 0.181 | | |
| NTSC | | | - | 48.1% | - | | |
| Electro Static Discharge | | Contact:±4KV,Air:±8KV 150pF, 330Ω, 200pF,0Ω +/-200V contact test | | | | | |

Test Conditions:

1. $DV_{DD}=3.3V$, $I_L=40mA$ (Backlight current),the ambient temperature is 25°C.
2. The test systems refer to Note 2.

5. Mechanical Drawing

