ADS42LBx9 14- and 16-Bit, 250-MSPS, Analog-to-Digital Converters

1 Features

- Dual Channel
- 14- and 16-Bit Resolution
- Maximum Clock Rate: 250 MSPS
- Analog Input Buffer with High Impedance Input
- Flexible Input Clock Buffer with Divide-by-1, -2, and -4
- 2-V_{PP} and 2.5-V_{PP} Differential Full-Scale Input (SPI-Programmable)
- DDR or QDR LVDS Interface
- 64-Pin VQFN Package (9-mm × 9-mm)
- Power Dissipation: 820 mW/ch
- Aperture Jitter: 85 f_S
- Internal Dither
- Channel Isolation: 100 dB
- Performance at f_{IN} = 170 MHz at 2 V_{PP}, –1 dBFS
  - SNR: 73.2 dBFS
  - SFDR:
    - 87 dBc (HD2 and HD3)
    - 100 dBc (Non HD2 and HD3)
- Performance at f_{IN} = 170 MHz: 2.5 V_{PP}, –1 dBFS
  - SNR: 74.9 dBFS
  - SFDR:
    - 85 dBc (HD2 and HD3)
    - 97 dBc (Non HD2 and HD3)

2 Applications

- Communication and Cable Infrastructure
- Multi-Carrier, Multimode Cellular Receivers
- Radar and Smart Antenna Arrays
- Broadband Wireless
- Test and Measurement Systems
- Software-Defined and Diversity Radios
- Microwave and Dual-Channel I/Q Receivers
- Repeaters
- Power Amplifier Linearization

3 Description

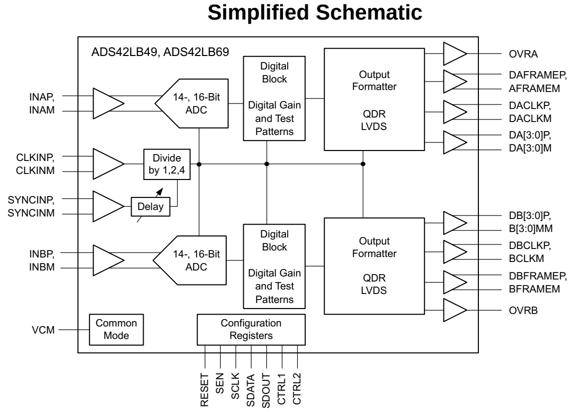
The ADS42LB49 and ADS42LB69 are a family of high-linearity, dual-channel, 14- and 16-bit, 250-MSPS, analog-to-digital converters (ADCs) supporting DDR and QDR LVDS output interfaces. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. A sampling clock divider allows more flexibility for system clock architecture design. The ADS42LBx9 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with low-power consumption.

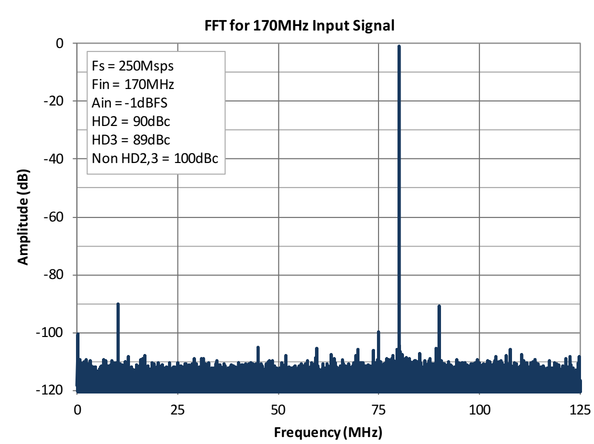
Device Information(1)

PART NUMBER	PACKAGE	INTERFACE OPTION
ADS42LB49	VQFN (64)	14-bit DDR or QDR LVDS
		14-bit JESD204B
ADS42LB69	VQFN (64)	16-bit DDR or QDR LVDS
		16-bit JESD204B

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic





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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (December 2014) to Revision F — **Page**

- Added *Using the ADS42LBx9 In Time-Domain, Low-Frequency Pulse Applications* section ... 63
- Added *Community Resources* section ... 70

Changes from Revision D (September 2013) to Revision E — **Page**

- Added *ESD Ratings* table and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted *Ordering Information* section ... 4
- Merged all Pin Functions tables into one table ... 7
- Changed INAP, INAM pin numbers for ADS42LB69 and ADS42LB49 DDR LVDS in pin assignments table ... 7
- Added footnote to Table 1 ... 15
- Added footnote to Table 2 ... 16
- Changed pin 34 to pin 37 in Figure 79 ... 36

Changes from Revision C (September 2013) to Revision D — **Page**

- Changed device status to Production Data ... 1
- Added pre-RTM changes throughout document ... 1

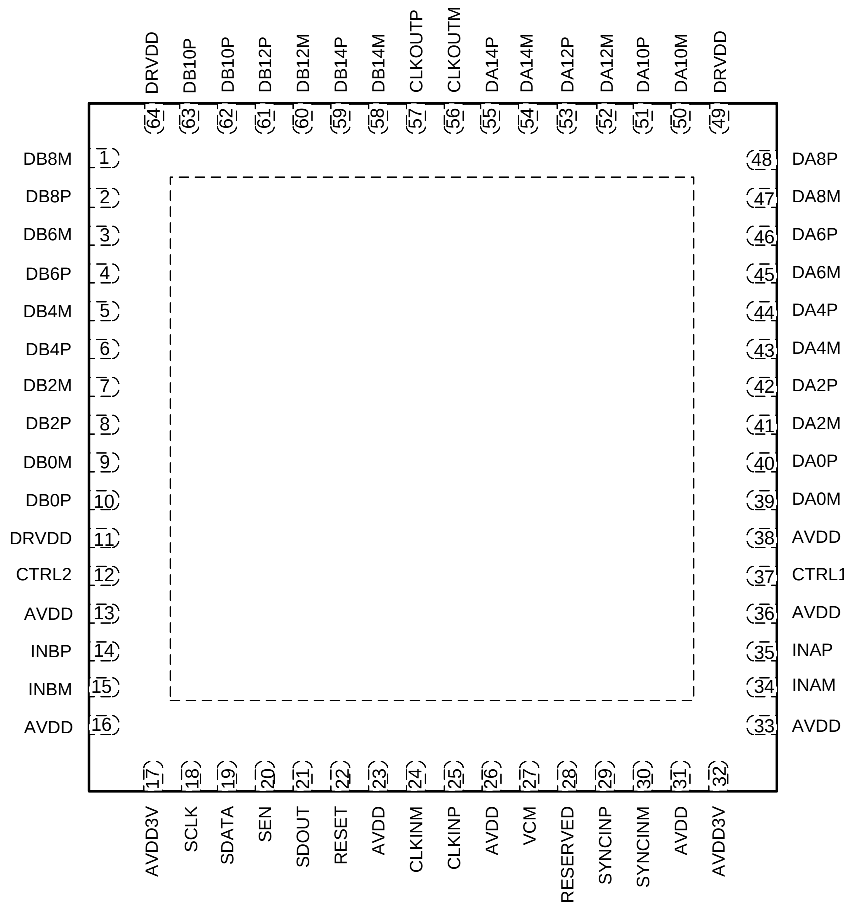
Changes from Revision B (March 2013) to Revision C	Page
• Added pre-RTM changes throughout document	1

Changes from Revision A (November 2012) to Revision B	Page
• Added pre-RTM changes throughout document	1

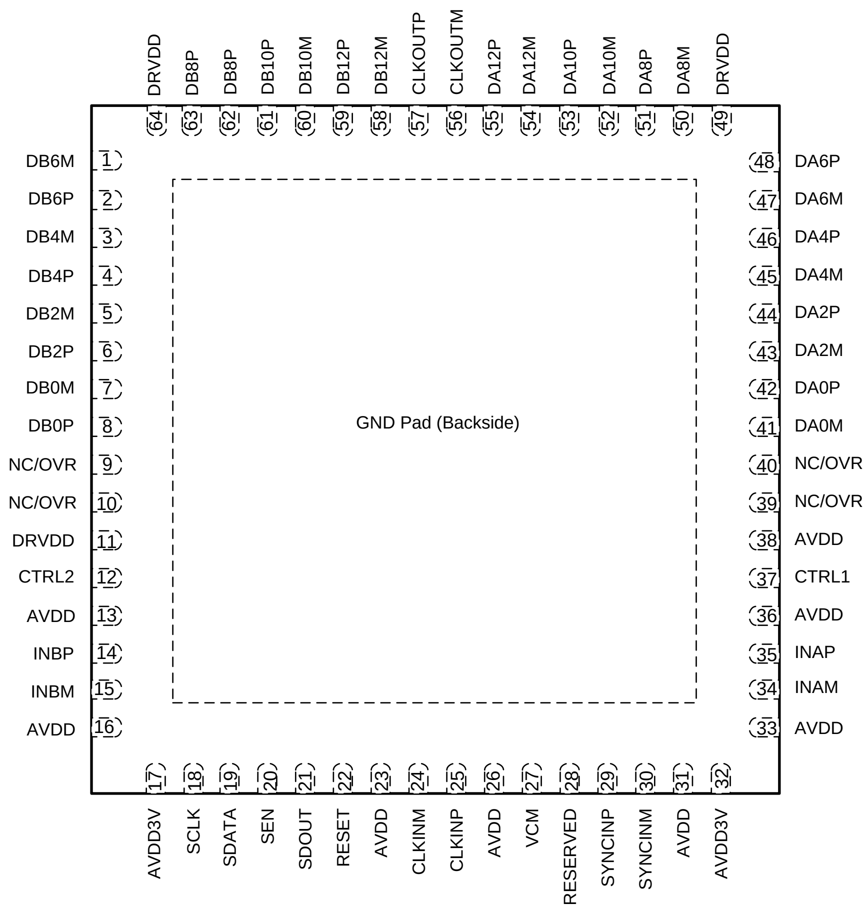
Changes from Original (October 2012) to Revision A	Page
• Added pre-RTM changes throughout document	1

5 Pin Configuration and Functions

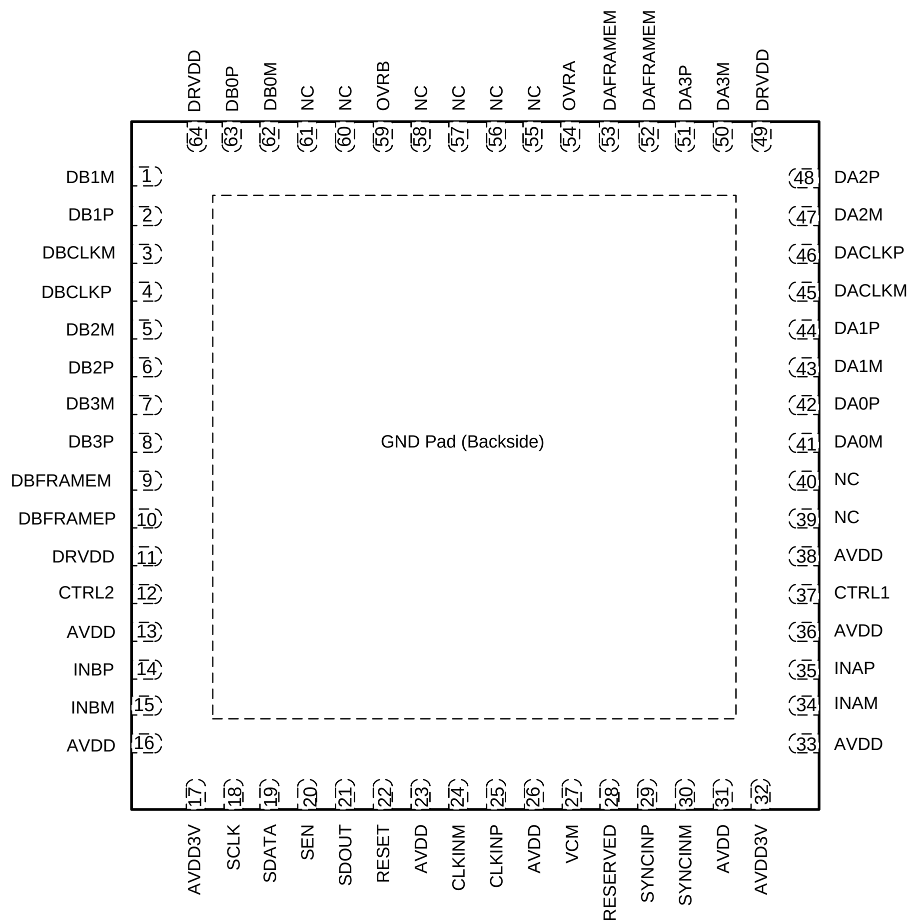
ADS42LB69 DDR LVDS: RGC Package
64-Pin VQFN
Top View



ADS42LB49 DDR LVDS: RGC Package
64-Pin VQFN
Top View



ADS42LB69, ADS42LB49 QDR LVDS: RGC Package
64-Pin VQFN
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	ADS42LB69 DDR LVDS	ADS42LB49 DDR LVDS	QDR LVDS		
INPUT AND REFERENCE					
INAP, INAM	35, 34	35, 34	34, 35	I	Differential analog input for channel A
INBP, INBM	14, 15	14, 15	14, 15	I	Differential analog input for channel B
VCM	27	27	27	O	Common-mode voltage for analog inputs, 1.9 V
CLOCK AND SYNC					
CLKINP, CLKINM	25, 24	25, 24	24, 25	I	Differential clock input for ADC
SYNCINP, SYNCINM	29, 30	29, 30	29, 30	I	External sync input. If not used, connect SYNCINP to GND and SYNCINM to AVDD.
CONTROL AND SERIAL					
CTRL1	37	37	37	I/O	Can be configured as power-down input pin or as OVR output pin for channel A, depending on the register bit PDN/OVR FOR CTRL PINS.
CTRL2	12	12	12	I/O	Can be configured as power-down input pin or as OVR output pin for channel B, depending on the register bit PDN/OVR FOR CTRL PINS
NC	—	—	39, 40, 55-58, 60, 61	—	Do not connect
NC/OVR	—	9, 10, 39, 40	—	—	If the OVR ON LSB bit is set, these pins can be used because they carry overrange information. Otherwise, do not connect these pins.
Reserved	28	28	28	—	Do not connect
RESET	22	22	22	I	Hardware reset. Active high.
SCLK	18	18	18	I	Serial interface clock input
SDATA	19	19	19	I	Serial interface data input
SDOUT	21	21	21	O	Serial interface data output
SEN	20	20	20	I	Serial interface enable
DATA INTERFACE					
CLKOUTP, CLKOUTM	57, 56	57, 56	—	O	Differential LVDS output clock
DA[3:0]P, DA[3:0]M	—	—	41-44, 47, 48, 50, 51	O	4-bit QDR LVDS output interface for channel A
DA[14:0]P, DA[14:0]M	39-48, 50-55	41-48, 50-55	—	O	DDR LVDS output interface for channel A
DACLKP, DACLKM	—	—	45, 46	O	Differential output clock for channel A
DAFRAMEP, DAFRAMEM	—	—	52, 53	—	Differential frame clock output for channel A
DB[3:0]P, DB[3:0]M	—	—	1, 2, 5-8, 62, 63	—	4-bit QDR LVDS output interface for channel B
DB[14:0]P, DB[14:0]M	1-10, 58-63	1-8, 58-63	—	O	DDR LVDS output interface for channel B
DBCLKP, DBCLKM	—	—	3, 4	—	Differential output clock for channel A
DBFRAMEP, DBFRAMEM	—	—	9, 10	—	Differential frame clock output for channel A

Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	ADS42LB69 DDR LVDS	ADS42LB49 DDR LVDS	QDR LVDS		
OVRA	—	—	54	O	Overrange indication channel A
OVRB	—	—	59	O	Overrange indication channel A
POWER SUPPLY					
AVDD	13, 16, 23, 26, 31, 33, 36, 38	13, 16, 23, 26, 31, 33, 36, 38	13, 16, 23, 26, 31, 33, 36, 38	I	Analog 1.8-V power supply
AVDD3V	17, 32	17, 32	17, 32	I	Analog 3.3 V power supply for analog buffer
DRVDD	11, 49, 64	11, 49, 64	11, 49, 64	I	Digital 1.8-V power supply
GND	Ground pad	Ground pad	Ground pad	I	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply voltage	AVDD3V	–0.3	3.6	V
	AVDD	–0.3	2.1	
	DRVDD	–0.3	2.1	
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INA, INBP, INA, INBM	–0.3	3	V
	CLKINP, CLKINM	–0.3	AVDD + 0.3	
	SYNCINP, SYNCINM	–0.3	AVDD + 0.3	
	SCLK, SEN, SDATA, RESET, CTRL1, CTRL2	–0.3	3.9	
Temperature	Operating free-air, T_A	–40	+85	°C
	Operating junction, T_J		+125	
	Storage, T_{stg}	–65	+150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
AVDD3V	Analog buffer supply voltage		3.15	3.3	3.45	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default after reset		2		V_{PP}
		Register programmable(2)		2.5		V_{PP}
V_{ICR}	Input common-mode voltage			VCM ± 0.025		V
	Maximum analog input frequency with 2.5-V_{PP} input amplitude			250		MHz
	Maximum analog input frequency with 2-V_{PP} input amplitude			400		MHz
CLOCK INPUT						
	Input clock sample rate	QDR interface	30		250	MSPS
		DDR interface	10		250	MSPS
	Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.3(3)	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		1.5		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			3.3		pF
R_{LOAD}	Single-ended load resistance			+50		Ω
T_A	Operating free-air temperature		–40		+85	°C

(1) After power-up, to reset the device for the first time, *only use the RESET pin*. Refer to the *Register Initialization* section.
(2) For details, refer to the *Digital Gain* section.
(3) Refer to the *Performance vs Clock Amplitude* curves, Figure 27 and Figure 28.

6.4 Thermal Information

THERMAL METRIC(1)		ADS42LBx9 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	2.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: ADS42LB69 (16-Bit)

Typical values are at T_A = +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	2-V_{PP} FULL-SCALE			2.5-V_{PP} FULL-SCALE			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73.9			75.8		dBFS
		f_{IN} = 70 MHz		73.7			75.5		
		f_{IN} = 170 MHz	70.8	73.2			74.7		
		f_{IN} = 230 MHz		72.8			74.1		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.7			75.1		dBFS
		f_{IN} = 70 MHz		73.6			75.3		
		f_{IN} = 170 MHz	69.6	73.1			74.2		
		f_{IN} = 230 MHz		72.5			73.4		
SFDR	Spurious-free dynamic range (including second and third harmonic distortion)	f_{IN} = 10 MHz		87			83		dBc
		f_{IN} = 70 MHz		90			88		
		f_{IN} = 170 MHz	81	87			85		
		f_{IN} = 230 MHz		86			83		
THD	Total harmonic distortion	f_{IN} = 10 MHz		86			82		dBc
		f_{IN} = 70 MHz		89			87		
		f_{IN} = 170 MHz	78	85			82		
		f_{IN} = 230 MHz		83			81		
HD2	2nd-order harmonic distortion	f_{IN} = 10 MHz		97			95		dBc
		f_{IN} = 70 MHz		90			88		
		f_{IN} = 170 MHz	81	87			85		
		f_{IN} = 230 MHz		86			84		
HD3	3rd-order harmonic distortion	f_{IN} = 10 MHz		87			83		dBc
		f_{IN} = 70 MHz		96			94		
		f_{IN} = 170 MHz	81	91			85		
		f_{IN} = 230 MHz		87			83		
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		102			103		dBc
		f_{IN} = 70 MHz		101			103		
		f_{IN} = 170 MHz	87	101			101		
		f_{IN} = 230 MHz		100			100		
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		97			94		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		94			90		
	Crosstalk	20-MHz, full-scale signal on channel under observation; 170-MHz, full-scale signal on other channel		100			100		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For 50-mV_{PP} signal on AVDD supply, up to 10 MHz		> 40			> 40		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.85			12.03		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		±0.6			±0.6		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±3	±8		±3.5		LSBs

6.6 Electrical Characteristics: ADS42LB49 (14-Bit)

Typical values are at T_A = +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	2-V_{PP} FULL-SCALE			2.5-V_{PP} FULL-SCALE			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73.3			74.9		dBFS
		f_{IN} = 70 MHz		73.1			74.7		
		f_{IN} = 170 MHz	69.5	72.7			74.1		
		f_{IN} = 230 MHz		72.3			73.5		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.1			74.1		dBFS
		f_{IN} = 70 MHz		73.1			74.4		
		f_{IN} = 170 MHz	68.5	72.6			73.6		
		f_{IN} = 230 MHz		72			72.9		
SFDR	Spurious-free dynamic range (including second and third harmonic distortion)	f_{IN} = 10 MHz		87			82		dBc
		f_{IN} = 70 MHz		90			88		
		f_{IN} = 170 MHz	79	87			85		
		f_{IN} = 230 MHz		86			83		
THD	Total harmonic distortion	f_{IN} = 10 MHz		86			81		dBc
		f_{IN} = 70 MHz		89			87		
		f_{IN} = 170 MHz	76	85			82		
		f_{IN} = 230 MHz		83			81		
HD2	2nd-order harmonic distortion	f_{IN} = 10 MHz		97			95		dBc
		f_{IN} = 70 MHz		90			88		
		f_{IN} = 170 MHz	79	87			85		
		f_{IN} = 230 MHz		86			84		
HD3	3rd-order harmonic distortion	f_{IN} = 10 MHz		87			82		dBc
		f_{IN} = 70 MHz		96			94		
		f_{IN} = 170 MHz	79	91			85		
		f_{IN} = 230 MHz		87			83		
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		104			103		dBc
		f_{IN} = 70 MHz		101			103		
		f_{IN} = 170 MHz	87	100			101		
		f_{IN} = 230 MHz		99			100		
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		99			95		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		93			93		
	Crosstalk	20-MHz, full-scale signal on channel under observation; 170-MHz, full-scale signal on other channel		100			90		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For a 50-mV_{PP} signal on AVDD supply, up to 10 MHz		> 40			> 40		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.76			11.93		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		±0.15			±0.15		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±0.75	±3		±0.9		LSBs

6.7 Electrical Characteristics: General

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default (after reset)		2		V_{PP}
		Register programmed(1)		2.5		
		Differential input resistance (at 170 MHz)		1.2		kΩ
		Differential input capacitance (at 170 MHz)		4		pF
	Analog input bandwidth	With 50-Ω source impedance, and 50-Ω termination		900		MHz
VCM	Common-mode output voltage			1.9		V
	VCM output current capability			10		mA
DC ACCURACY						
	Offset error		–20		20	mV
E_{GREF}	Gain error as a result of internal reference inaccuracy alone			±2		%FS
E_{GCHAN}	Gain error of channel alone			–5		%FS
	Temperature coefficient of E_{GCHAN}			0.01		Δ%/°C
POWER SUPPLY						
IAVDD	Analog supply current			141	182	mA
IAVDD3V	Analog buffer supply current			302	340	mA
IDRVDD	Digital and output buffer supply current	External 100-Ω differential termination on LVDS outputs		219	245	mA
	Analog power			253		mW
	Analog buffer power			996		mW
	Power consumption (includes digital blocks and output buffers)	External 100-Ω differential termination on LVDS outputs		393		mW
	Total power			1.64	1.85	W
	Global power-down (both channels)				160	mW

(1) Refer to the *Serial Interface* section.

6.8 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2)(1)							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current	RESET, SDATA, SCLK, CTRL1, CTRL2(2)	V_{HIGH} = 1.8 V		10		µA
		SEN(3)	V_{HIGH} = 1.8 V		0		
I_{IL}	Low-level input current	RESET, SDATA, SCLK, CTRL1, CTRL2	V_{LOW} = 0 V		0		µA
		SEN	V_{LOW} = 0 V		10		
DIGITAL OUTPUTS, CMOS INTERFACE (OVRA, OVRB, SDOUT)							
V_{OH}	High-level output voltage			DRVDD – 0.1	DRVDD		V
V_{OL}	Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS, LVDS INTERFACE							
V_{ODH}	High-level output differential voltage		With an external 100-Ω termination	250	350	500	mV
V_{ODL}	Low-level output differential voltage		With an external 100-Ω termination	–500	–350	–250	mV
V_{OCM}	Output common-mode voltage				1.05		V

(1) SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.
(2) SDATA and SCLK have an internal 150-kΩ pull-down resistor.
(3) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up resistor is weak, SEN can also be driven by 1.8-V or 3.3-V CMOS buffers.

6.9 Timing Requirements: General

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 3.3 pF, and R_{LOAD} = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.7 V to 1.9 V.

			MIN	TYP	MAX	UNIT
t_A	Aperture delay		0.5	0.7	1.1	ns
	Aperture delay matching between two channels of the same device			±70		ps
	Variation of aperture delay between two devices at the same temperature and supply voltage			±150		ps
t_J	Aperture jitter			85		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		50	100	µs
		Time to valid data after coming out of GLOBAL power-down mode (in this mode, both channels power-down)		250	1000	µs
	ADC latency(1)	Default latency after reset		14		Clock cycles
		Normal OVR latency		14		Clock cycles
		Fast OVR latency		9		Clock cycles
t_{SU_SYNCIN}	Setup time for SYNCIN, referenced to input clock rising edge		400			ps
t_{H_SYNCIN}	Hold time for SYNCIN, referenced to input clock rising edge		100			ps

(1) Overall latency = ADC latency + t_{PDI}.

6.10 Timing Requirements: DDR LVDS Mode(1)

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 3.3 pF, and R_{LOAD} = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, and DRVDD = 1.7 V to 1.9 V.

		MIN	TYP	MAX	UNIT
t_{SU}	Data setup time: data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)(2)	0.62	0.82		ns
t_{HO}	Data hold time: zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid(2)	0.54	0.64		ns
t_{PDI}	Clock propagation delay: input clock rising edge cross-over to output clock (CLKOUTP – CLKOUTM) rising edge cross-over	8	10.5	13	ns
	LVDS bit clock duty cycle: duty cycle of differential clock (CLKOUTP – CLKOUTM)		52%		
t_{FALL}, t_{RISE}	Data fall time, data rise time: rise time measured from –100 mV to +100 mV, *10 MSPS ≤ sampling frequency ≤ 250 MSPS*		0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time: Rise time measured from –100 mV to +100 mV, *10 MSPS ≤ sampling frequency ≤ 250 MSPS*		0.18		ns

(1) Measurements are done with a transmission line of a 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(2) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.

Table 1. DDR LVDS Timings at Lower Sampling Frequencies(1)

SAMPLING FREQUENCY (MSPS)	SETUP TIME t_{SU} MIN	SETUP TIME t_{SU} TYP	SETUP TIME t_{SU} MAX	HOLD TIME t_{HO} MIN	HOLD TIME t_{HO} TYP	HOLD TIME t_{HO} MAX	CLOCK PROPAGATION DELAY t_{PDI} MIN	CLOCK PROPAGATION DELAY t_{PDI} TYP	CLOCK PROPAGATION DELAY t_{PDI} MAX	UNIT
80	2.40	2.96		2.16	2.82		9	11.9	15	ns
120	1.57	1.92		1.40	1.84		8	11.1	14	
160	1.17	1.40		1.02	1.36		8	10.6	13	
200	0.82	1.07		0.72	1.02		8	10.5	13	
230	0.69	0.91		0.61	0.84		8	10.5	13	

(1) See Figure 73 for a timing diagram in DDR LVDS mode.

6.11 Timing Requirements: QDR LVDS Mode(1)(2)

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine-wave input clock, C_{LOAD} = 3.3 pF(3), and R_{LOAD} = 100 Ω(4), unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, and DRVDD = 1.7 V to 1.9 V.

		MIN	TYP	MAX	UNIT
t_{SU}	Data setup time(5)(6): data valid to DxCLKP, DxCLKM zero-crossing	0.23	0.31		ns
t_H	Data hold time(5)(6): DxCLKP, DxCLKM zero-crossing to data becoming invalid	0.16	0.29		ns
	LVDS bit clock duty cycle: differential bit clock duty cycle (DxCLKP, DxCLKM)		50%		
t_{PDI}	Clock propagation delay: input clock rising edge cross-over to output frame clock (DxFRAMEP-DxFRAMEM) rising edge cross-over	7	10.1	13	ns
t_{RISE}, t_{FALL}	Data rise and fall time: rise time measured from –100 mV to +100 mV		0.18		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise and fall time: rise time measured from –100 mV to +100 mV		0.2		ns

(1) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(2) Timing parameters are ensured by design and characterization and are not tested in production.
(3) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(4) R_{LOAD} is the differential load resistance between the LVDS output pair.
(5) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.
(6) The setup and hold times of a channel are measured with respect to the same channel output clock.

Table 2. QDR LVDS Timings at Lower Sampling Frequencies(1)

SAMPLING FREQUENCY (MSPS)	SETUP TIME t_{SU}			HOLD TIME t_{HO}			CLOCK PROPAGATION DELAY t_{PDI}			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
80	1.06	1.21		0.84	1.29		6	9.3	12	ns
120	0.63	0.77		0.66	0.88		7	9.5	13	
160	0.43	0.55		0.39	0.61		7	9.7	13	
200	0.31	0.42		0.28	0.47		7	9.8	13	
230	0.24	0.34		0.17	0.36		7	9.9	13	

(1) See Figure 74 for a timing diagram in QDR LVDS mode.

6.12 Typical Characteristics: ADS42LB69

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

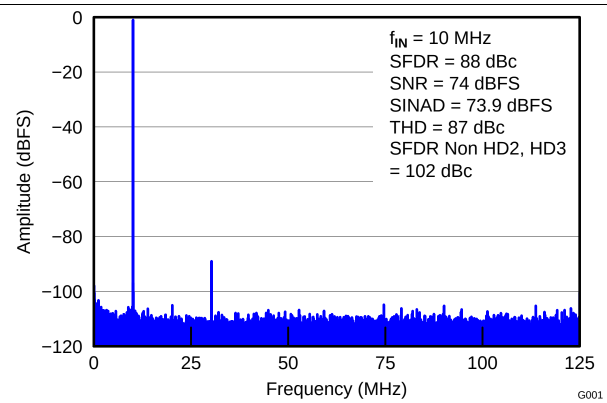


Figure 1. FFT for 10-MHz Input Signal

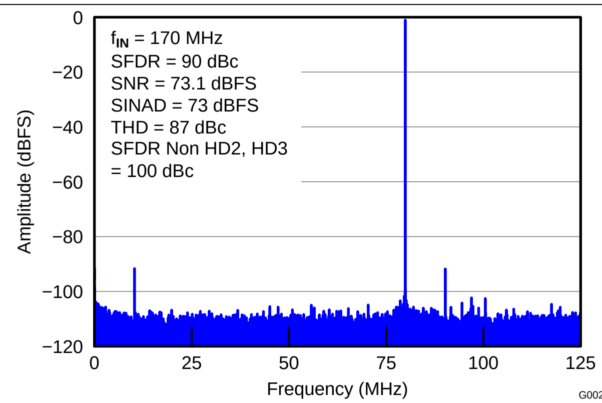


Figure 2. FFT for 170-MHz Input Signal

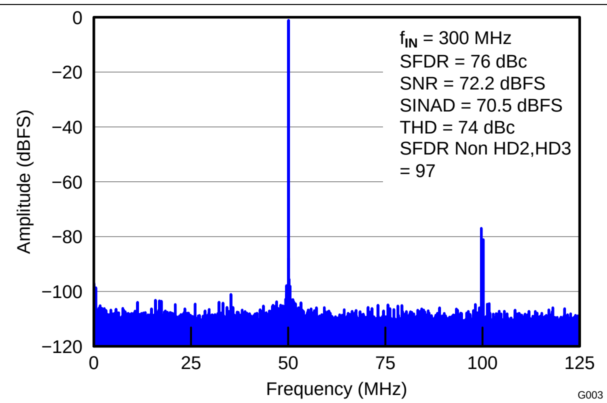


Figure 3. FFT for 300-MHz Input Signal

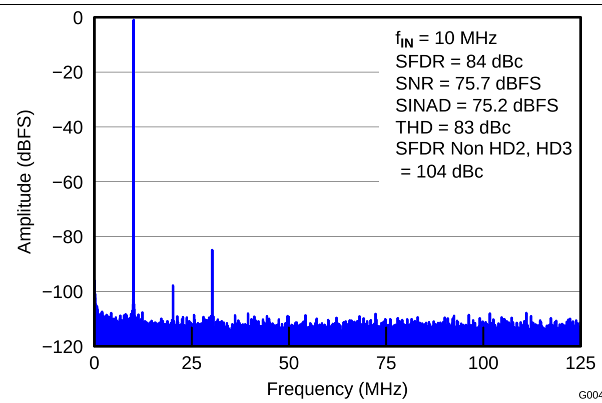


Figure 4. FFT for 10-MHz Input Signal (2.5-V_{PP} Full-Scale)

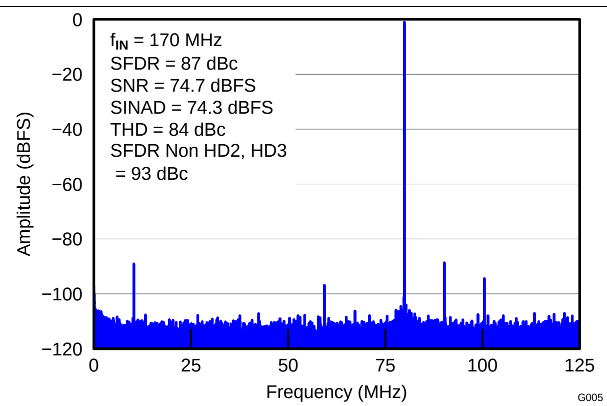


Figure 5. FFT for 170-MHz Input Signal (2.5-V_{PP} Full-Scale)

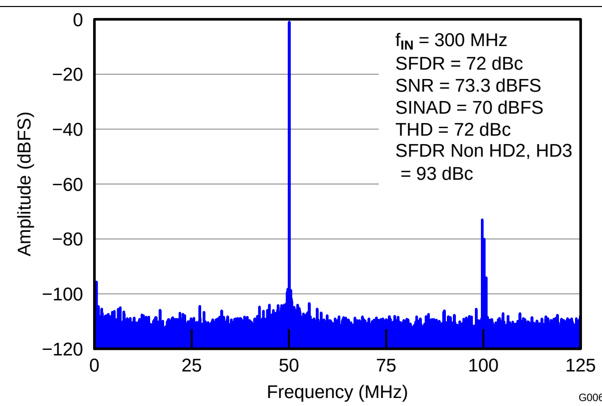


Figure 6. FFT for 300-MHz Input Signal (2.5-V_{PP} Full-Scale)

Typical Characteristics: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

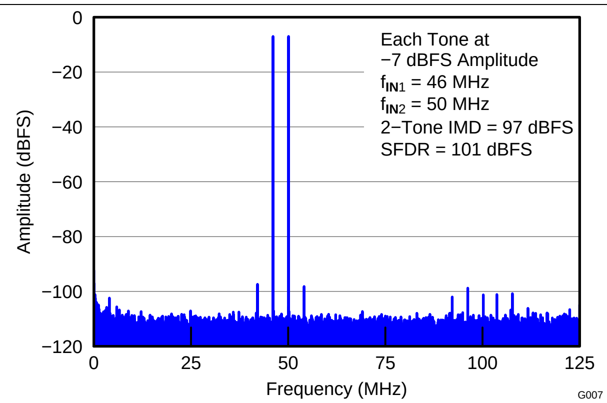


Figure 7. FFT for Two-Tone Input Signal (At –7 dBFS, 46 MHz and 50 MHz)

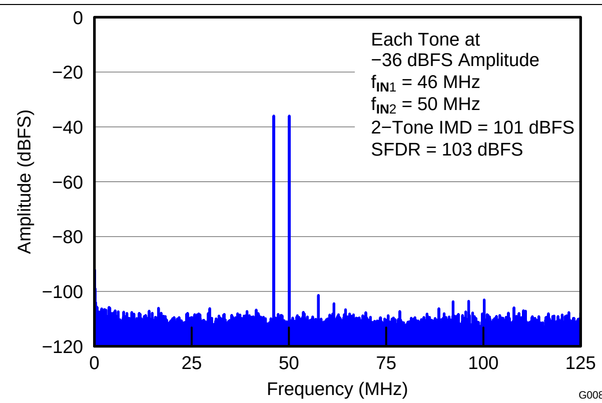


Figure 8. FFT for Two-Tone Input Signal (At –36 dBFS, 46 MHz and 50 MHz)

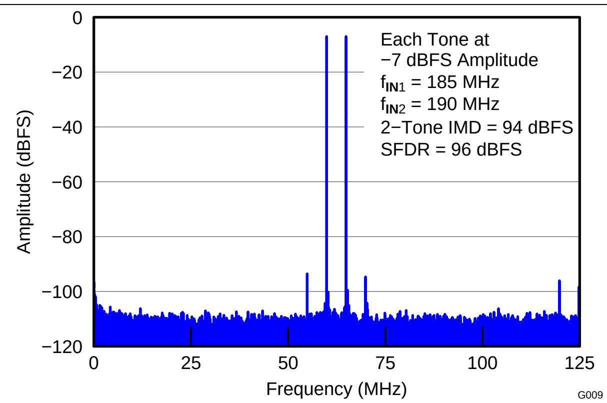


Figure 9. FFT for Two-Tone Input Signal (At –7 dBFS, 185 MHz and 190 MHz)

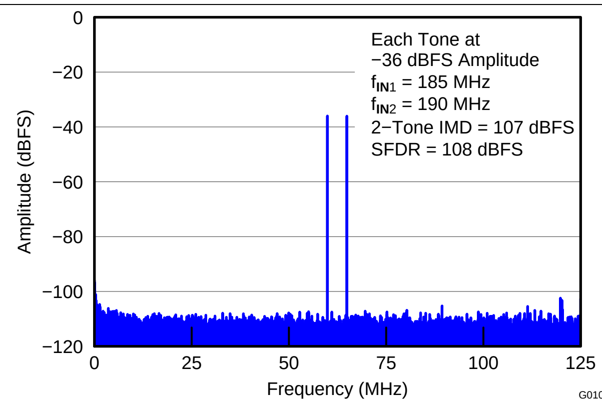


Figure 10. FFT for Two-Tone Input Signal (At –36 dBFS, 185 MHz and 190 MHz)

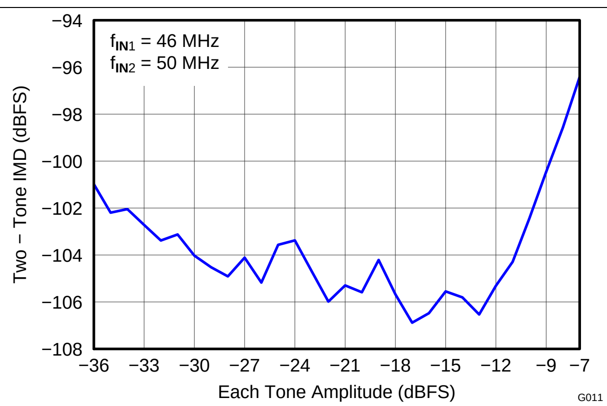


Figure 11. IMD3 vs Input Amplitude (46 MHz and 50 MHz)

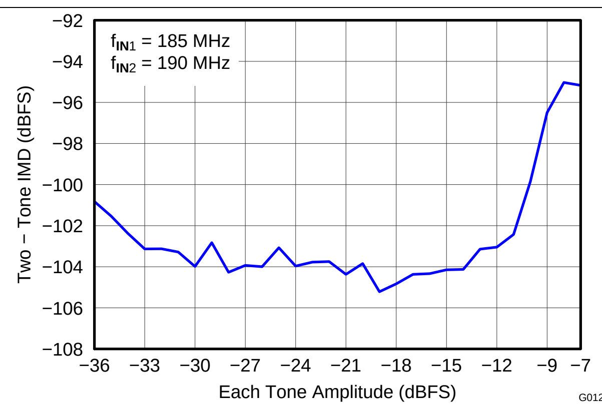


Figure 12. IMD3 vs Input Amplitude (185 MHz and 190 MHz)

Typical Characteristics: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

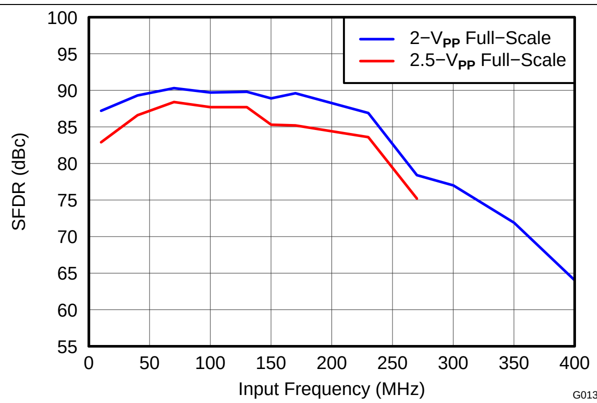


Figure 13. SFDR vs Input Frequency

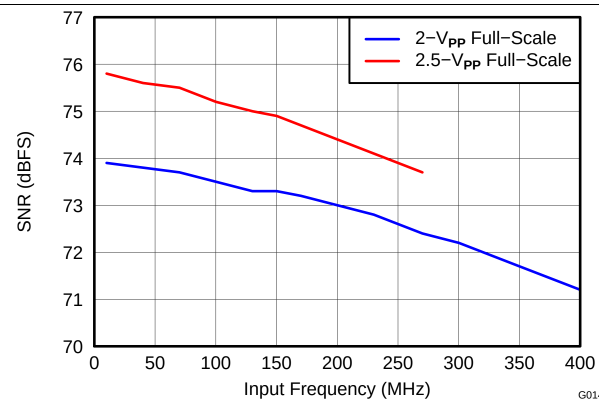


Figure 14. SNR vs Input Frequency

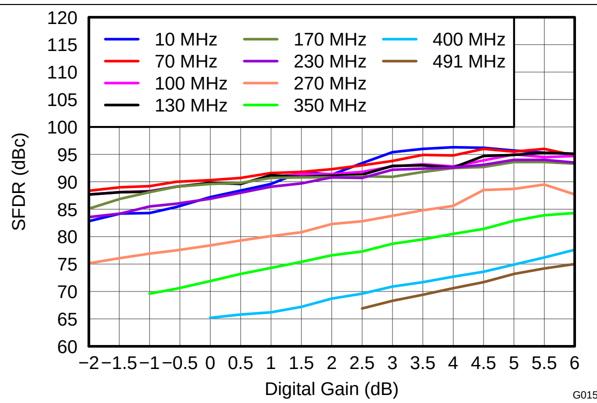


Figure 15. SFDR vs Digital Gain

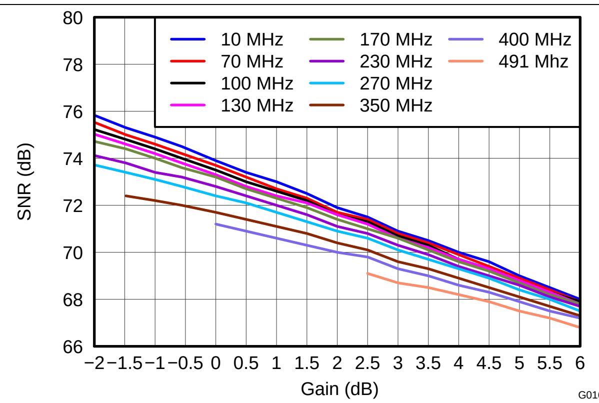


Figure 16. SNR vs Digital Gain

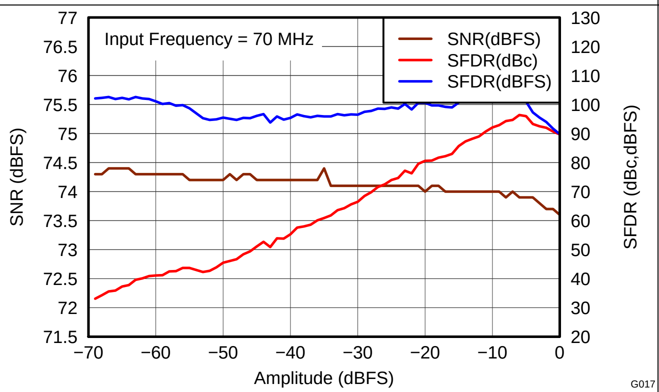


Figure 17. Performance Across Input Amplitude (70 MHz)

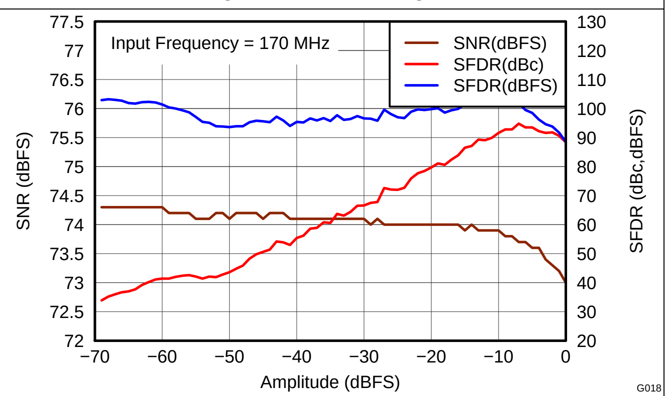


Figure 18. Performance Across Input Amplitude (170 MHz)

Typical Characteristics: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

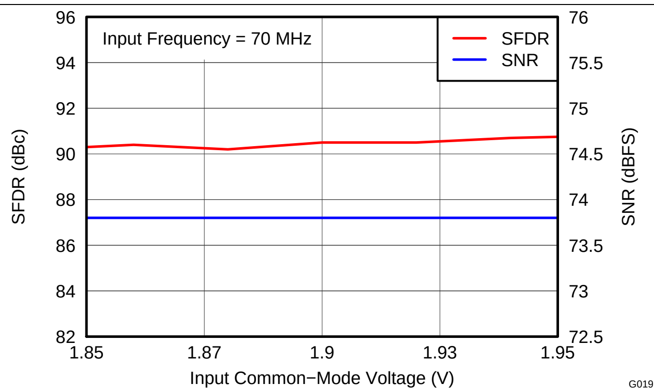


Figure 19. Performance vs Input Common-Mode Voltage (70 MHz)

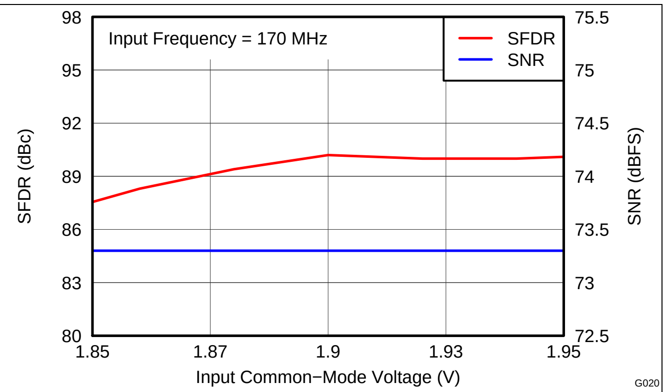


Figure 20. Performance vs Input Common-Mode Voltage (170 MHz)

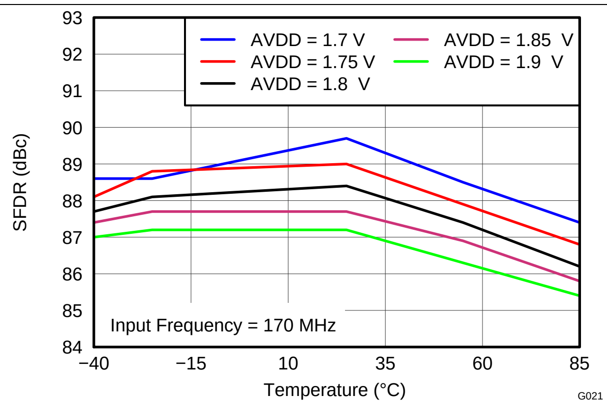


Figure 21. SFDR vs AVDD Supply and Temperature (170 MHz)

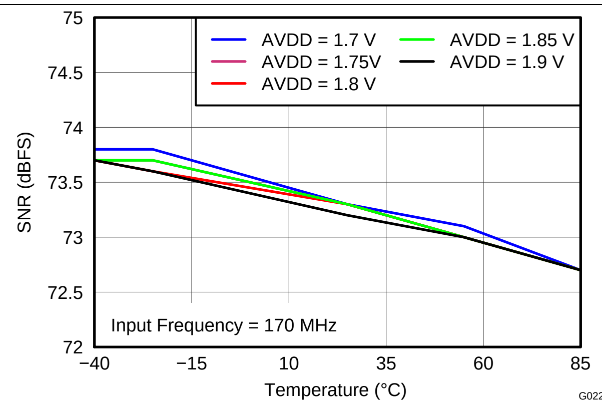


Figure 22. SNR vs AVDD Supply and Temperature (170 MHz)

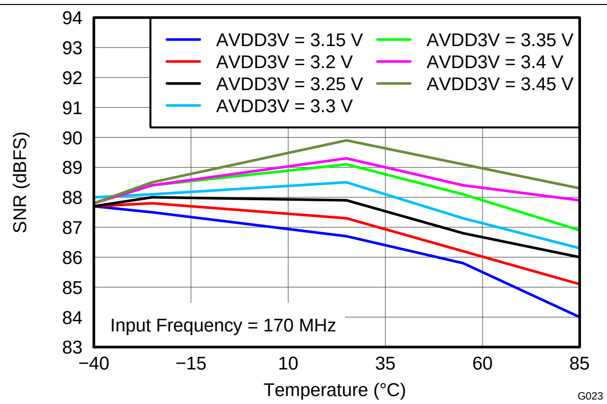


Figure 23. SFDR vs AVDD_BUF Supply and Temperature (170 MHz)

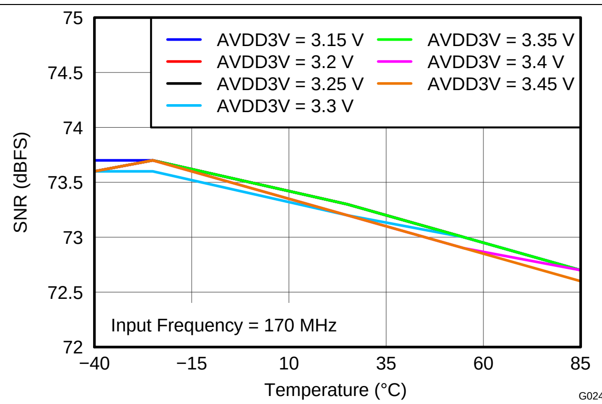


Figure 24. SNR vs AVDD_BUF Supply and Temperature (170 MHz)

Typical Characteristics: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

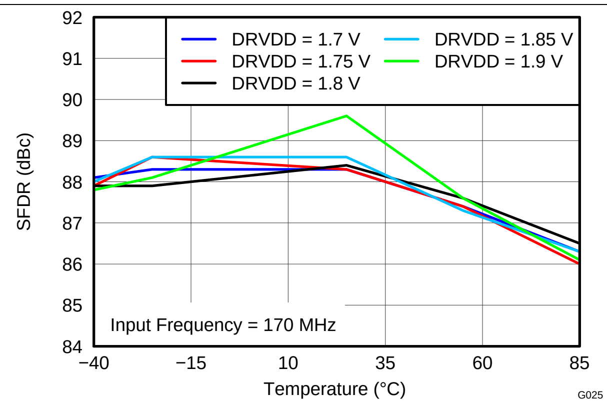


Figure 25. SFDR vs DRVDD Supply and Temperature (170 MHz)

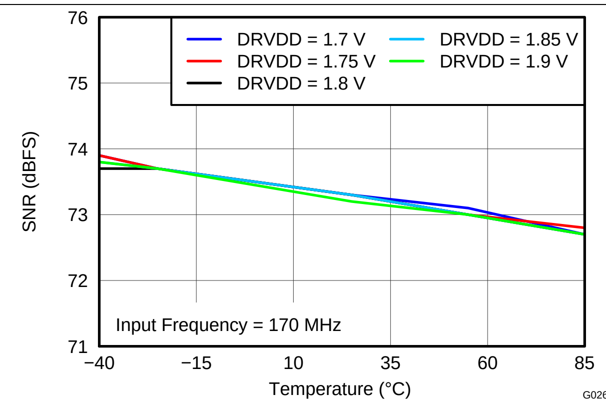


Figure 26. SNR vs DRVDD Supply and Temperature (170 MHz)

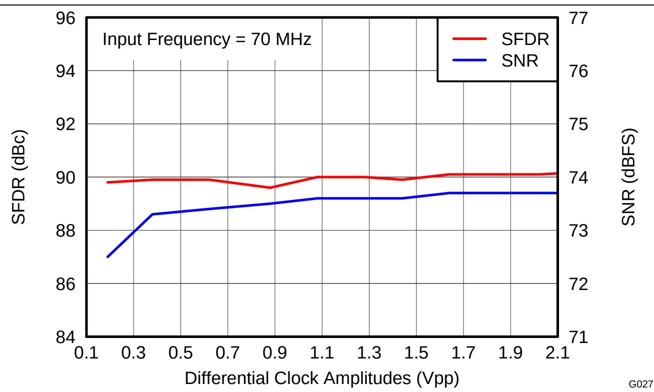


Figure 27. Performance vs Clock Amplitude (70 MHz)

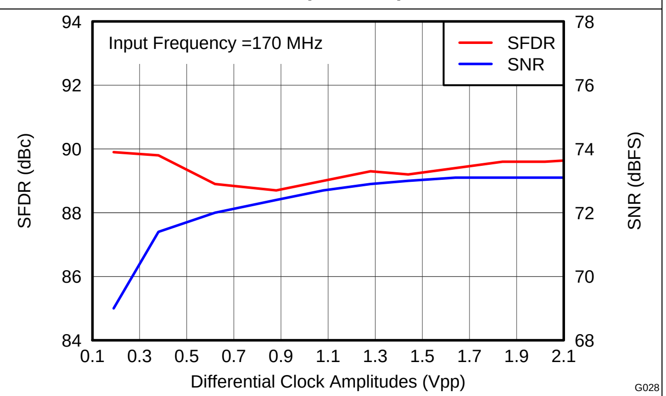


Figure 28. Performance vs Clock Amplitude (170 MHz)

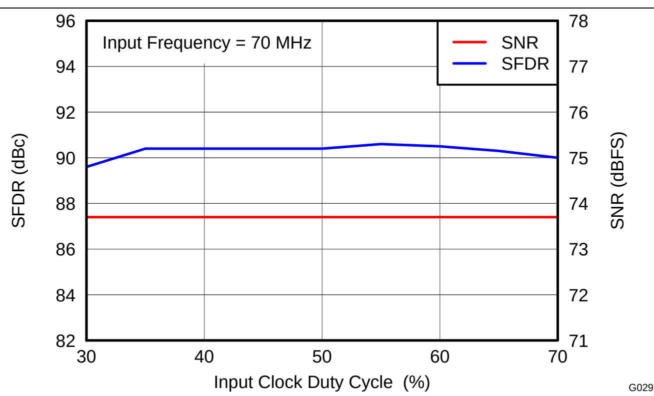


Figure 29. Performance vs Clock Duty Cycle (70 MHz)

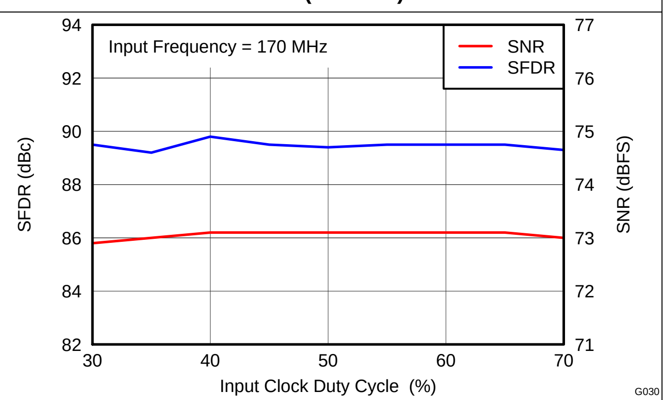


Figure 30. Performance vs Clock Duty Cycle (170 MHz)

6.13 Typical Characteristics: ADS42LB49

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

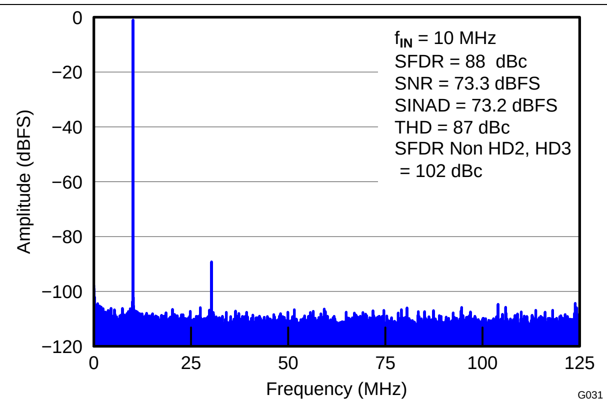


Figure 31. FFT for 10-MHz Input Signal

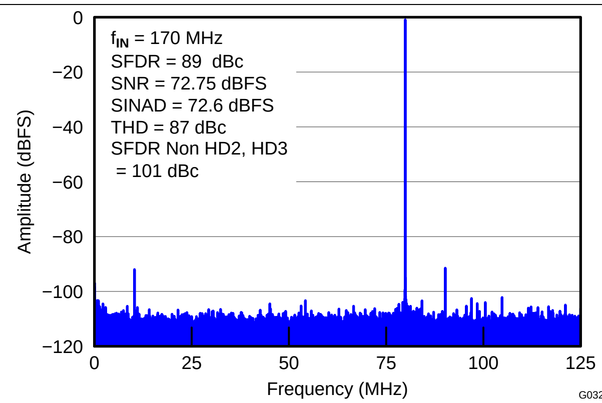


Figure 32. FFT for 170-MHz Input Signal

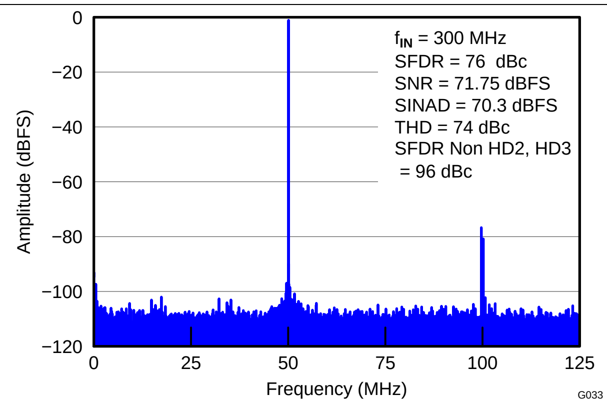


Figure 33. FFT for 300-MHz Input Signal

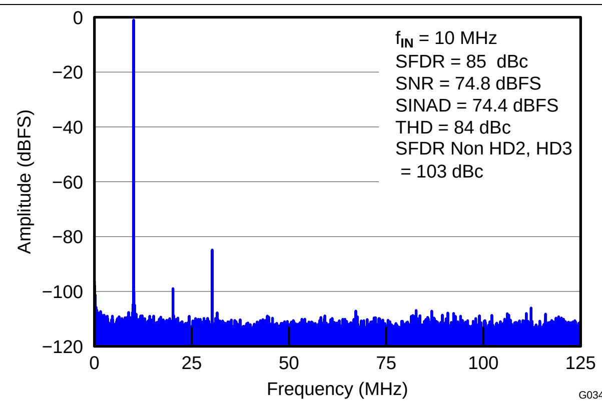


Figure 34. FFT for 10-MHz Input Signal (2.5-V_{PP} Full-Scale)

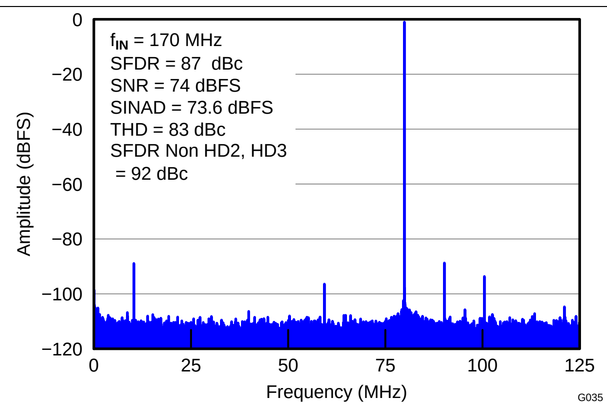


Figure 35. FFT for 170-MHz Input Signal (2.5-V_{PP} Full-Scale)

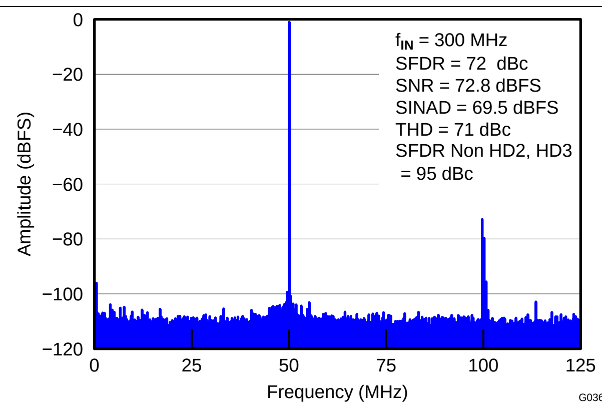


Figure 36. FFT for 300-MHz Input Signal (2.5-V_{PP} Full-Scale)

Typical Characteristics: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

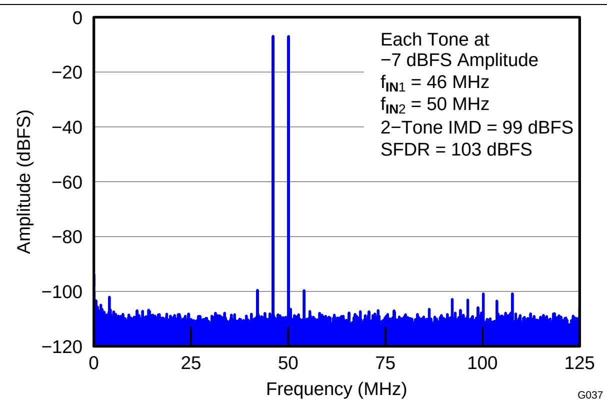


Figure 37. FFT for Two-Tone Input Signal (At –7 dBFS, 46 MHz and 50 MHz)

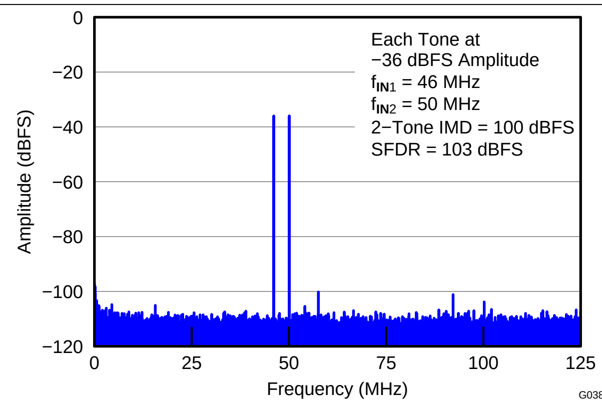


Figure 38. FFT for Two-Tone Input Signal (At –36 dBFS, 46 MHz and 50 MHz)

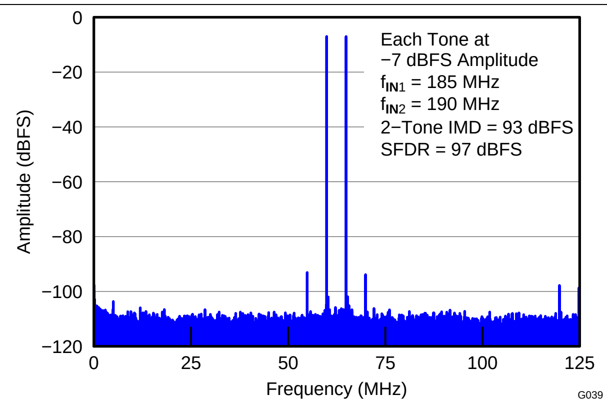


Figure 39. FFT for Two-Tone Input Signal (At –7 dBFS, 185 MHz and 190 MHz)

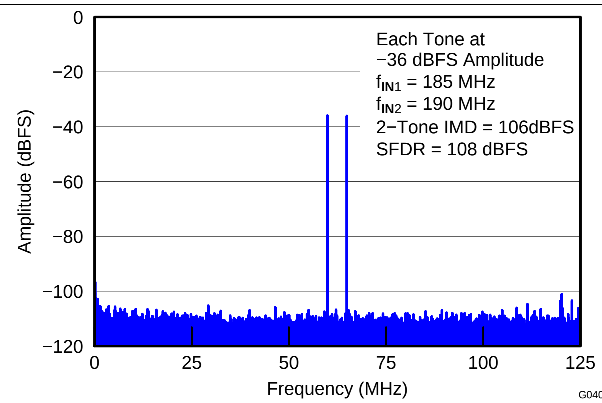


Figure 40. FFT for Two-Tone Input Signal (At –36 dBFS, 185 MHz and 190 MHz)

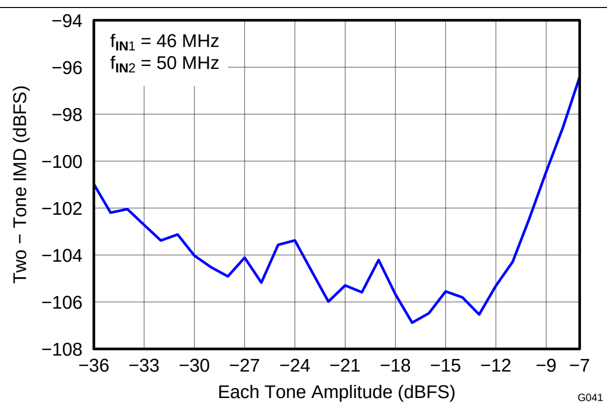


Figure 41. IMD3 vs Input Amplitude (46 MHz and 50 MHz)

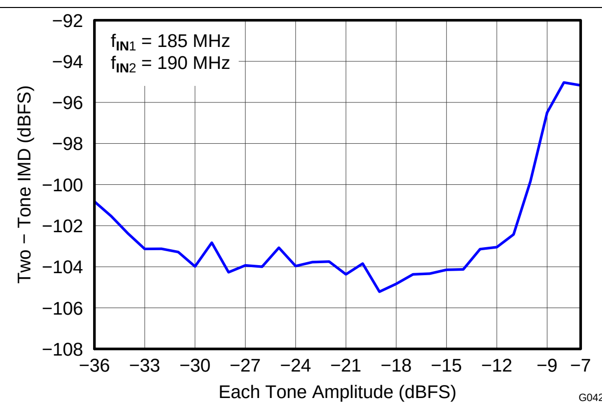


Figure 42. IMD3 vs Input Amplitude (185 MHz and 190 MHz)

Typical Characteristics: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

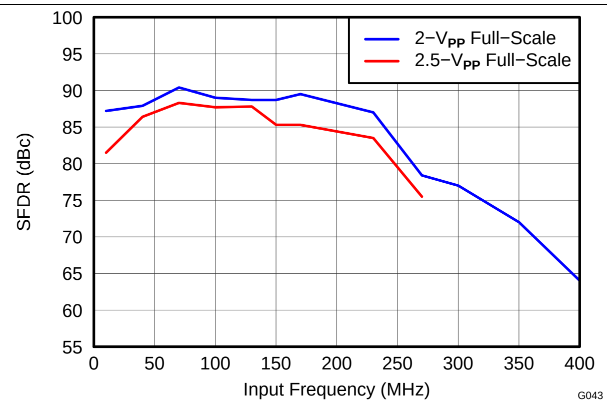


Figure 43. SFDR vs Input Frequency

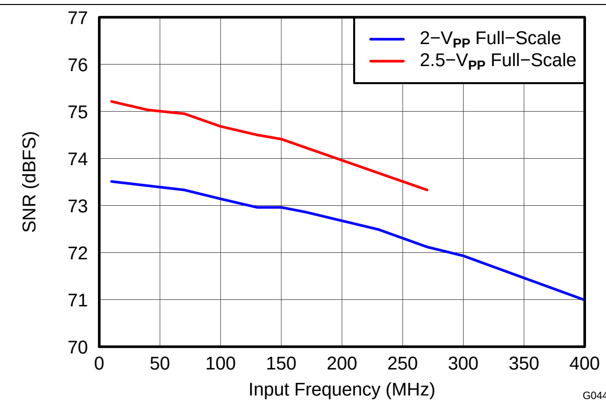


Figure 44. SNR vs Input Frequency

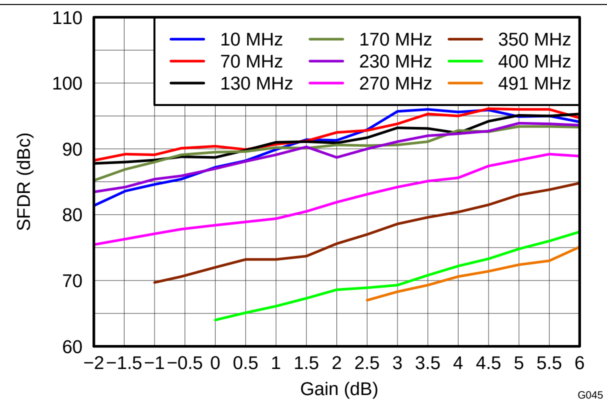


Figure 45. SFDR vs Digital Gain

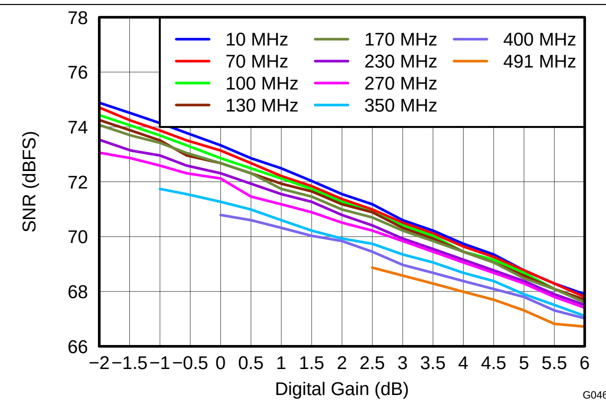


Figure 46. SNR vs Digital Gain

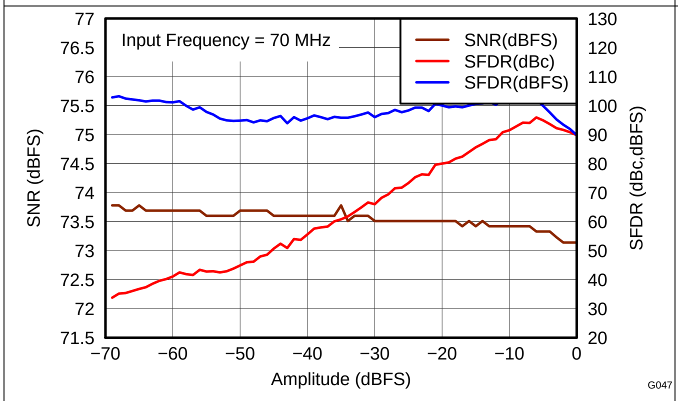


Figure 47. Performance Across Input Amplitude (70 MHz)

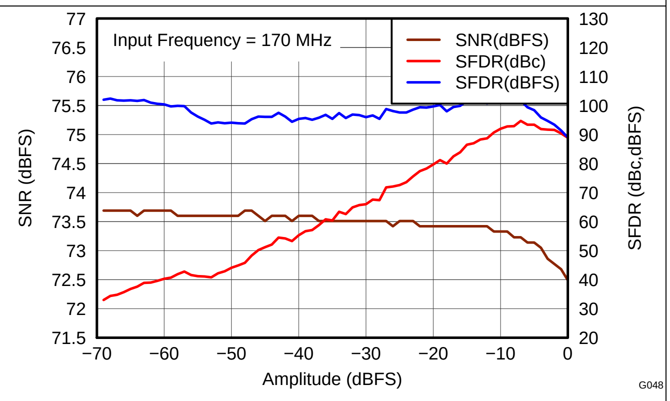


Figure 48. Performance Across Input Amplitude (170 MHz)

Typical Characteristics: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

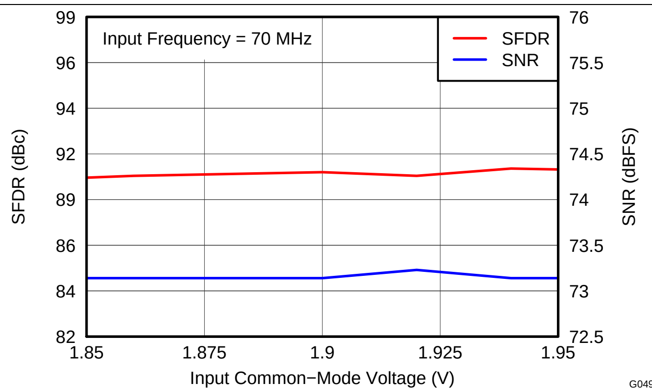


Figure 49. Performance vs Input Common-Mode Voltage (70 MHz)

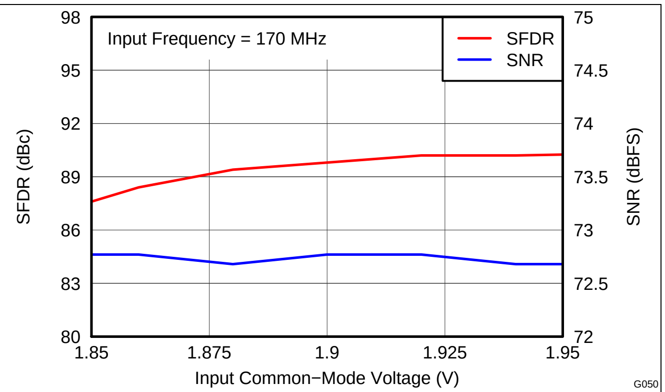


Figure 50. Performance vs Input Common-Mode Voltage (170 MHz)

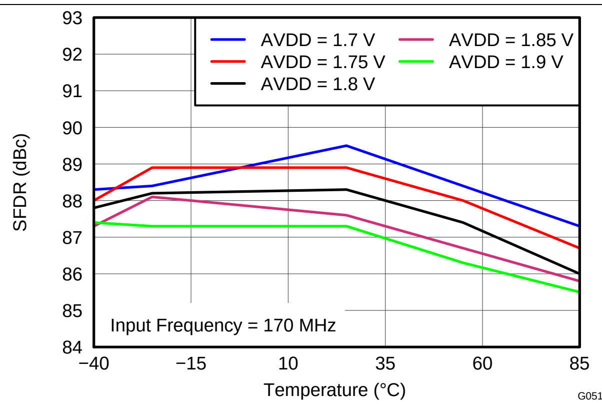


Figure 51. SFDR vs AVDD Supply and Temperature (170 MHz)

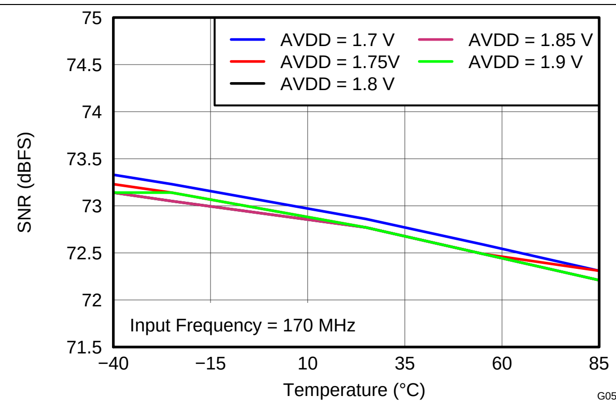


Figure 52. SNR vs AVDD Supply and Temperature (170 MHz)

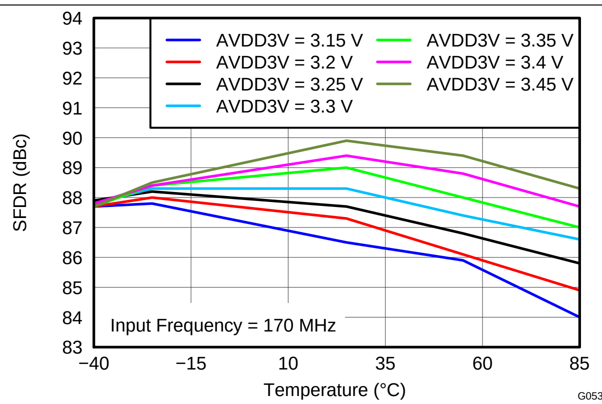


Figure 53. SFDR vs AVDD_BUF Supply and Temperature (170 MHz)

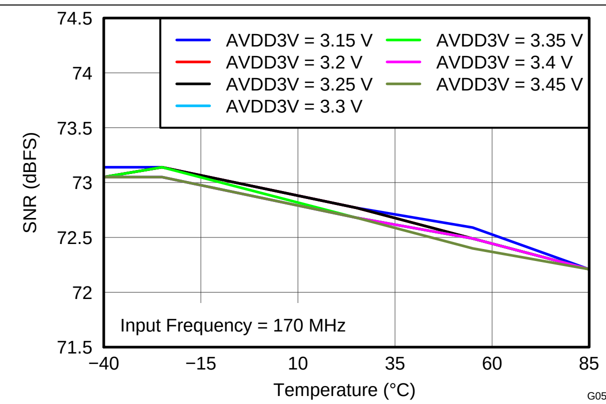


Figure 54. SNR vs AVDD_BUF Supply and Temperature (170 MHz)

Typical Characteristics: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

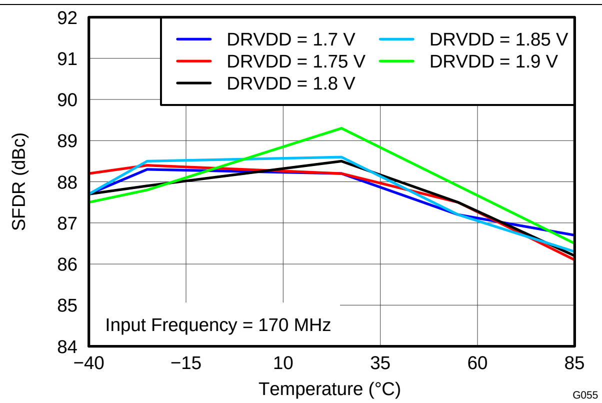


Figure 55. SFDR vs DRVDD Supply and Temperature (170 MHz)

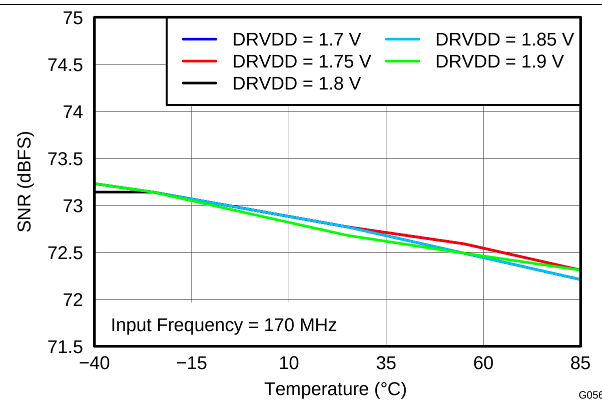


Figure 56. SNR vs DRVDD Supply and Temperature (170 MHz)

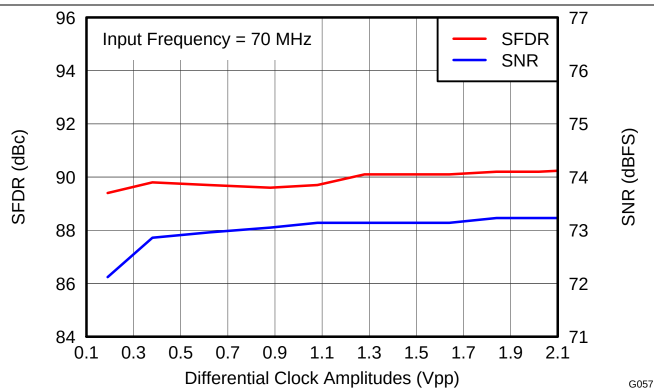


Figure 57. Performance vs Clock Amplitude (70 MHz)

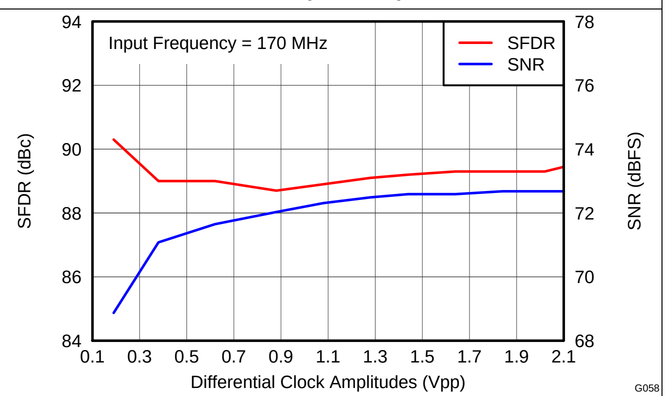


Figure 58. Performance vs Clock Amplitude (170 MHz)

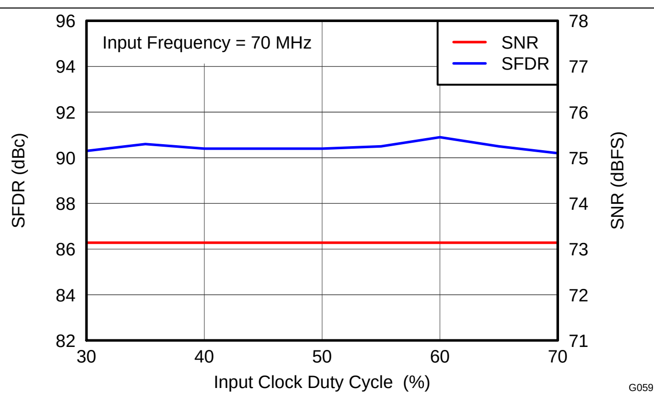


Figure 59. Performance vs Clock Duty Cycle (70 MHz)

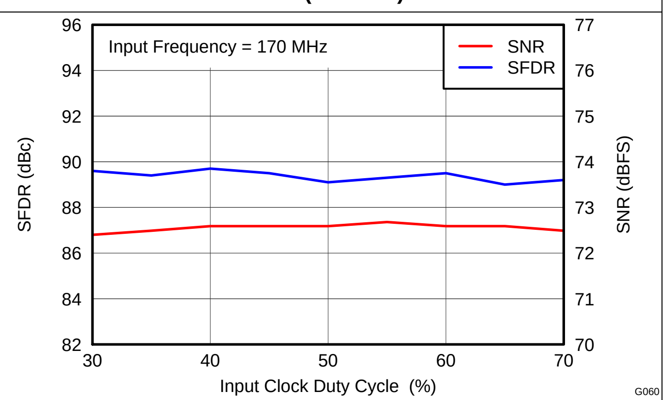


Figure 60. Performance vs Clock Duty Cycle (170 MHz)

6.14 Typical Characteristics: Common

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

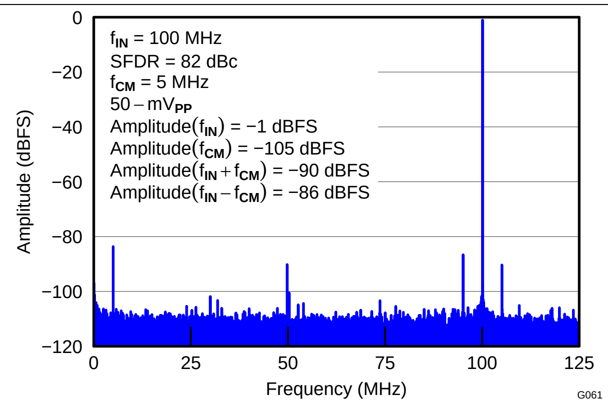


Figure 61. CMRR FFT

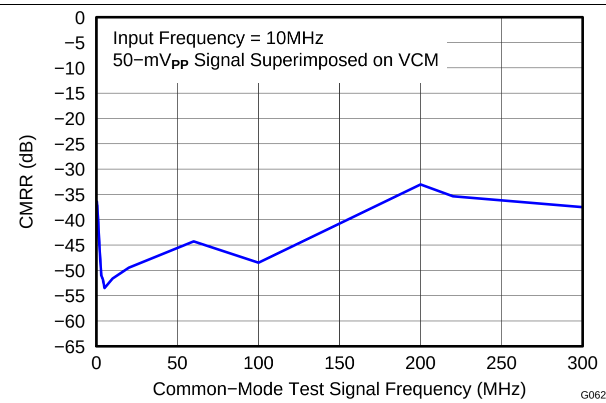


Figure 62. CMRR vs Test Signal Frequency

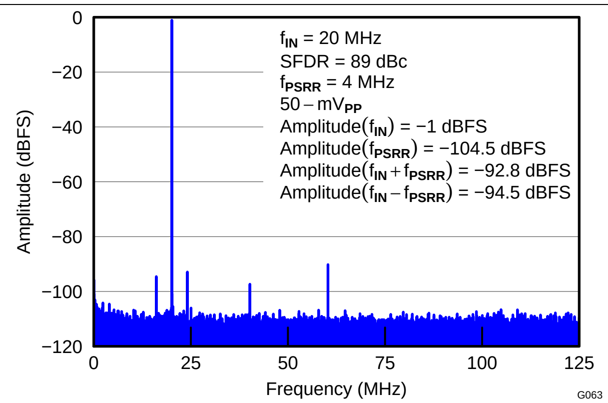


Figure 63. PSRR FFT for AVDD Supply

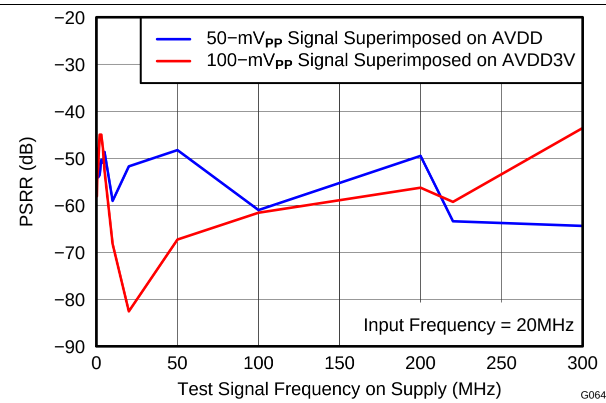


Figure 64. PSRR vs Test Signal Frequency

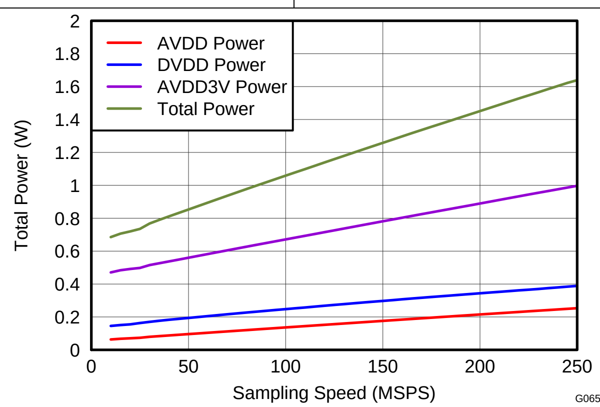


Figure 65. Total Power vs Sampling Frequency

6.15 Typical Characteristics: Contour

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 65k-point FFT, unless otherwise noted.

6.15.1 Spurious-Free Dynamic Range (SFDR): General

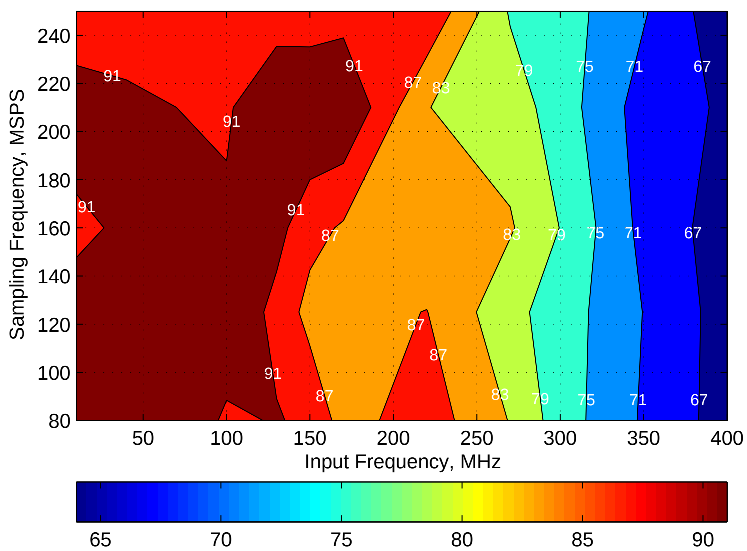


Figure 66. SFDR (0-dB Gain)

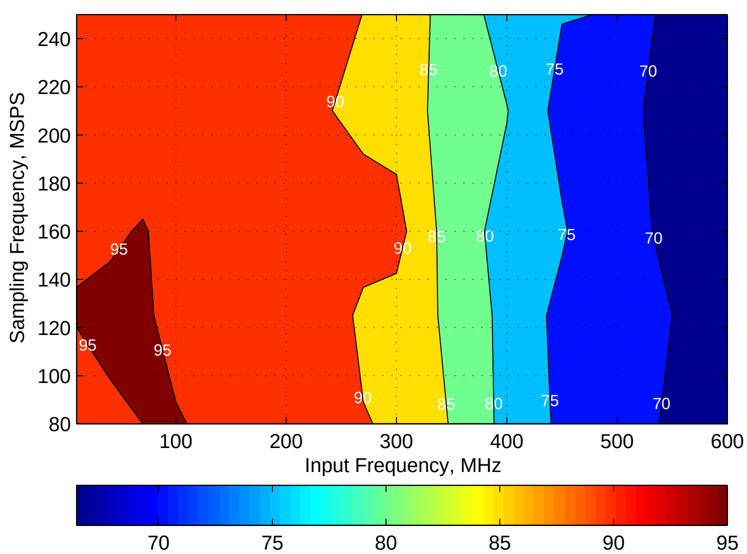


Figure 67. SFDR (6-dB Gain)

6.15.2 Signal-to-Noise Ratio (SNR): ADS42LB69

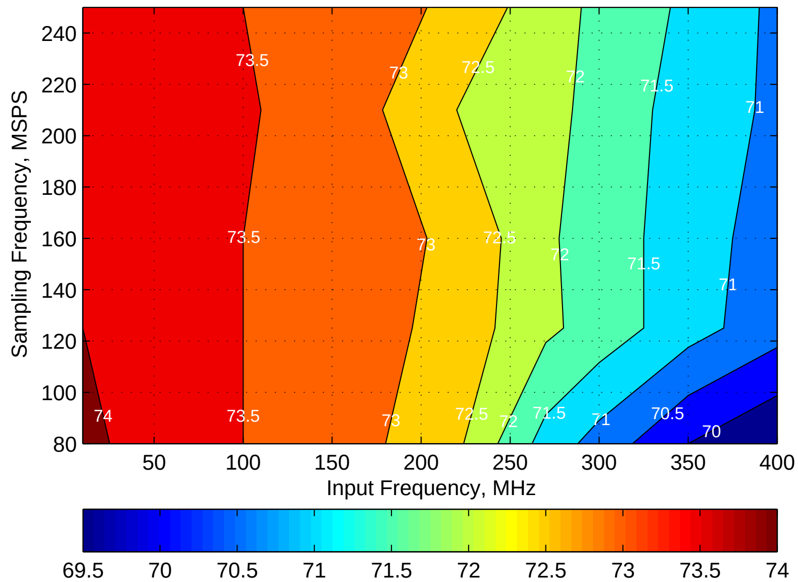


Figure 68. SNR (0-dB Gain, 16 Bits)

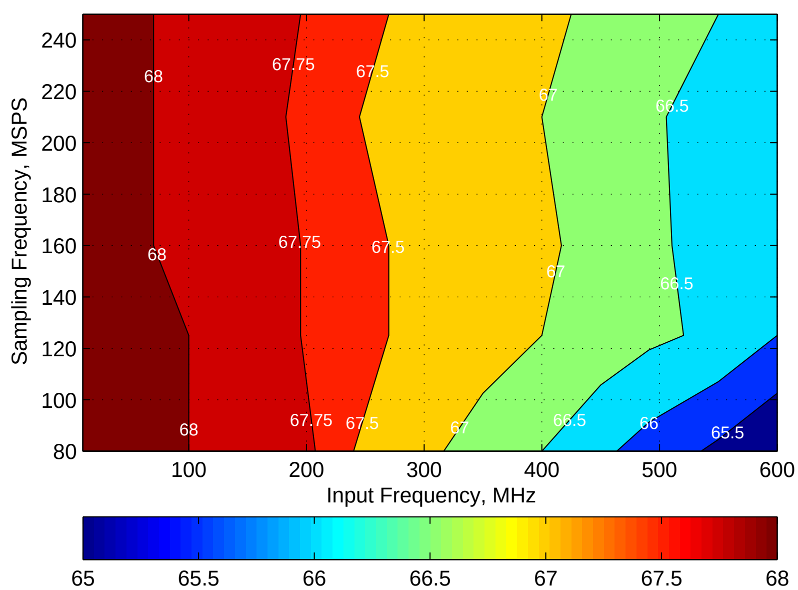


Figure 69. SNR (6-dB Gain, 16 Bits)

6.15.3 Signal-to-Noise Ratio (SNR): ADS42LB49

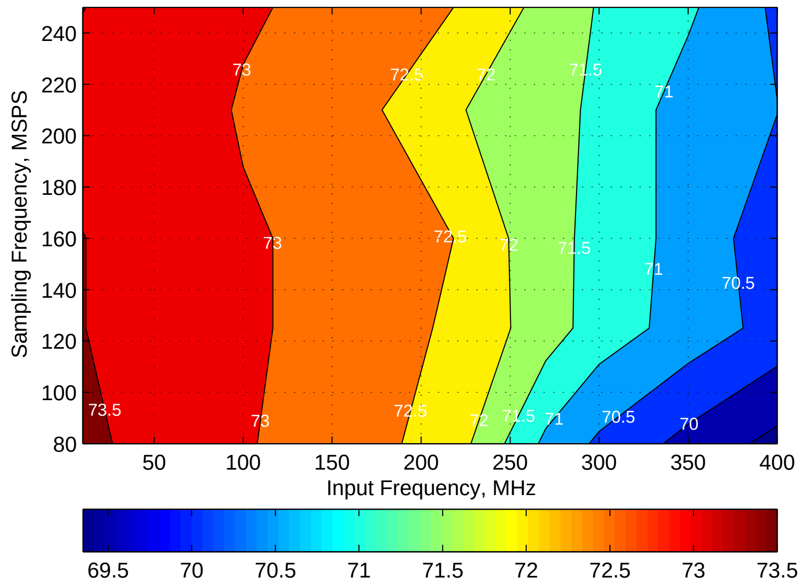


Figure 70. SNR (0-dB Gain, 14 Bits)

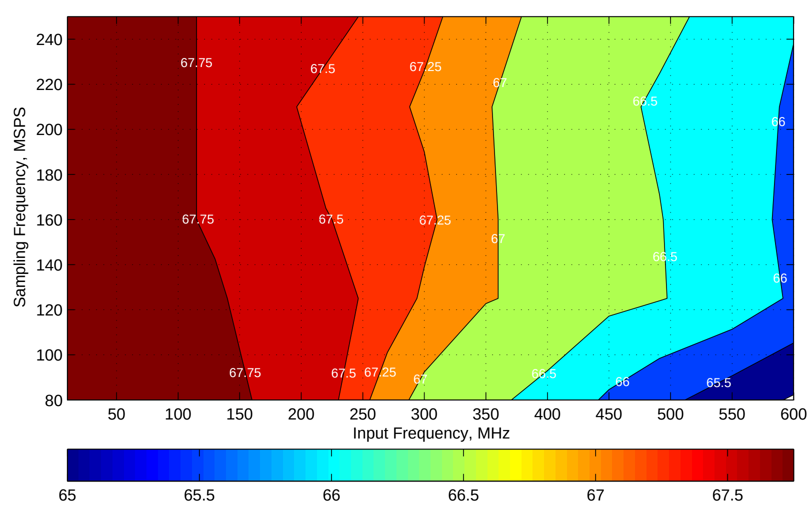


Figure 71. SNR (6-dB Gain, 14 Bits)

7 Parameter Measurement Information

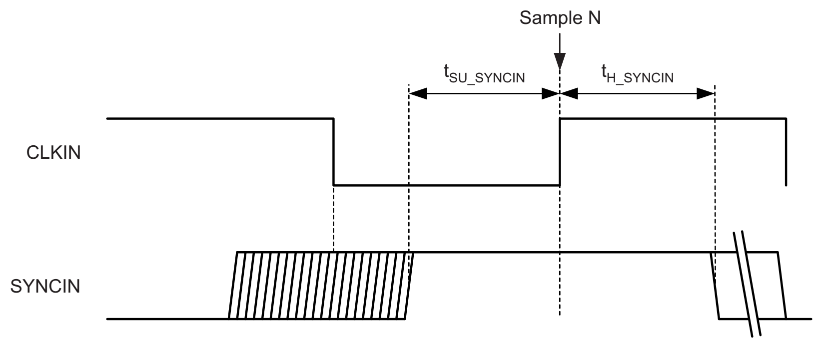


Figure 72. Timing Diagram for SYNCINP and SYNCINM Inputs

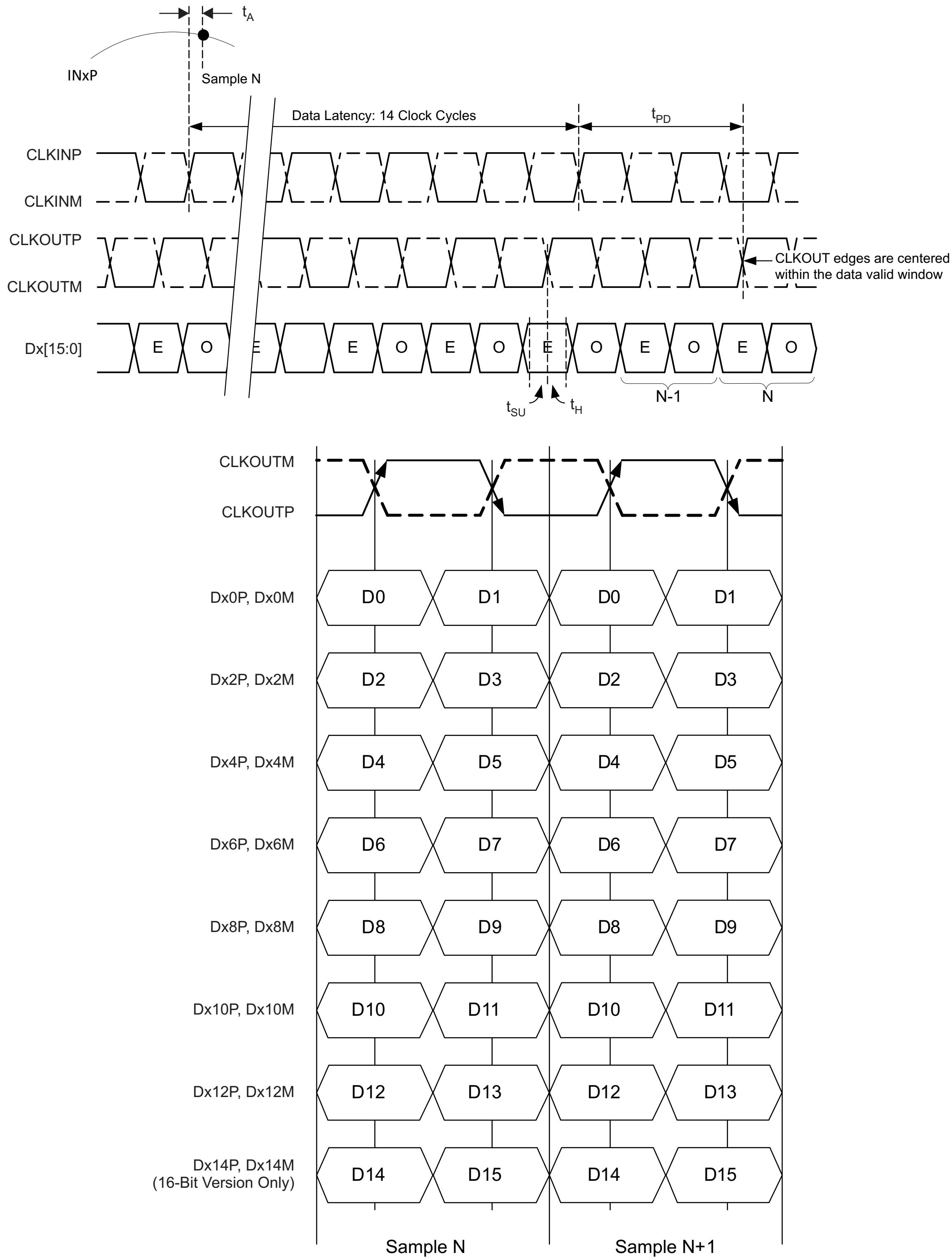


Figure 73. DDR LVDS Output Timing Diagram

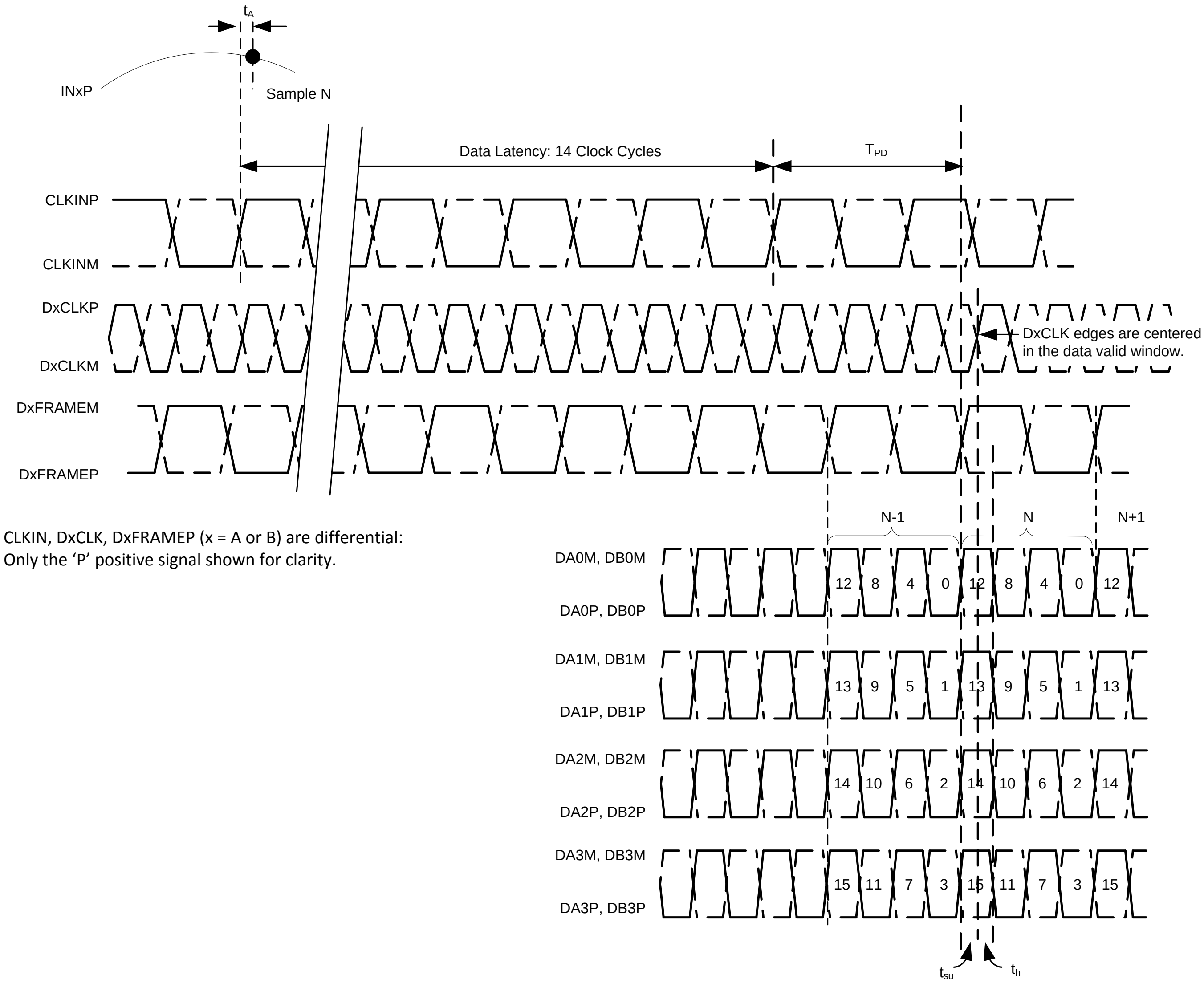
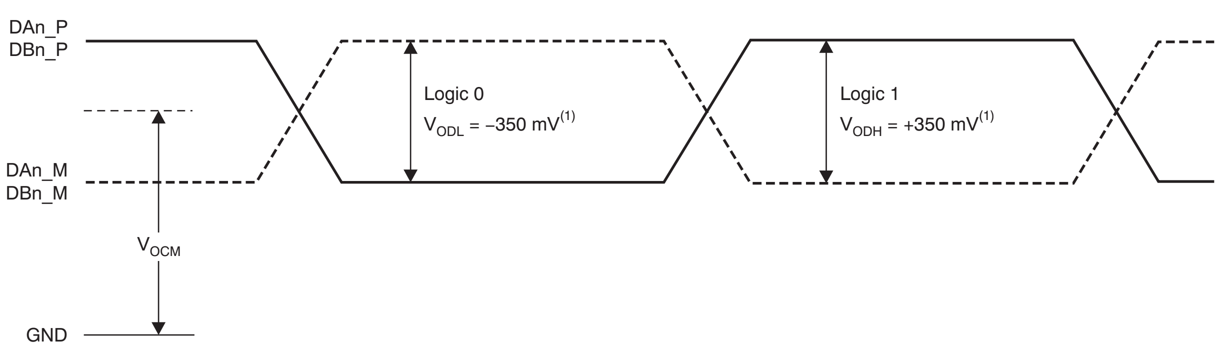


Figure 74. QDR LVDS Output Timing Diagram



(1) With an external 100-Ω termination.

Figure 75. DDR LVDS Output Voltage Levels

8 Detailed Description

8.1 Overview

The ADS42LB69 and ADS42LB49 is a family of high linearity, buffered analog input, dual-channel ADCs with maximum sampling rates up to 250 MSPS employing either a quadruple data rate (QDR) or double data rate (DDR) LVDS interface. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 14 clock cycles. The output is available in LVDS logic levels in SPI-programmable QDR or DDR options.

8.2 Functional Block Diagrams

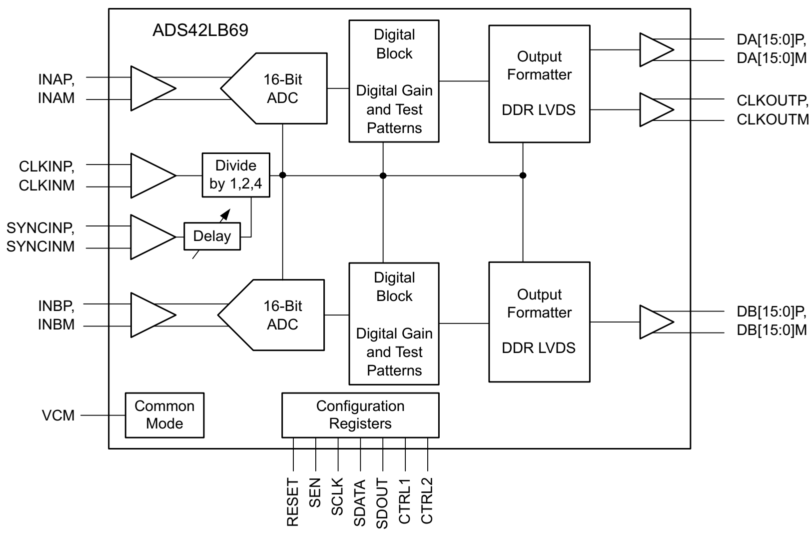


Figure 76. ADS42LB69 DDR LVDS

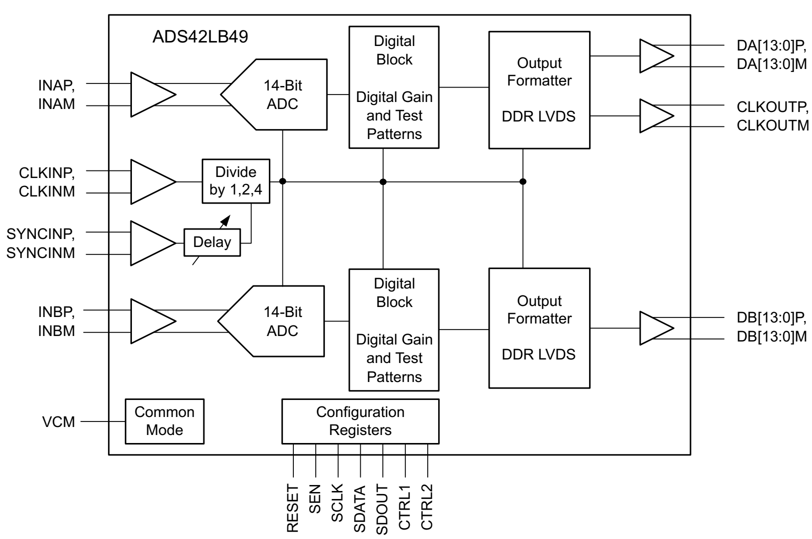


Figure 77. ADS42LB49 DDR LVDS

Functional Block Diagrams (continued)

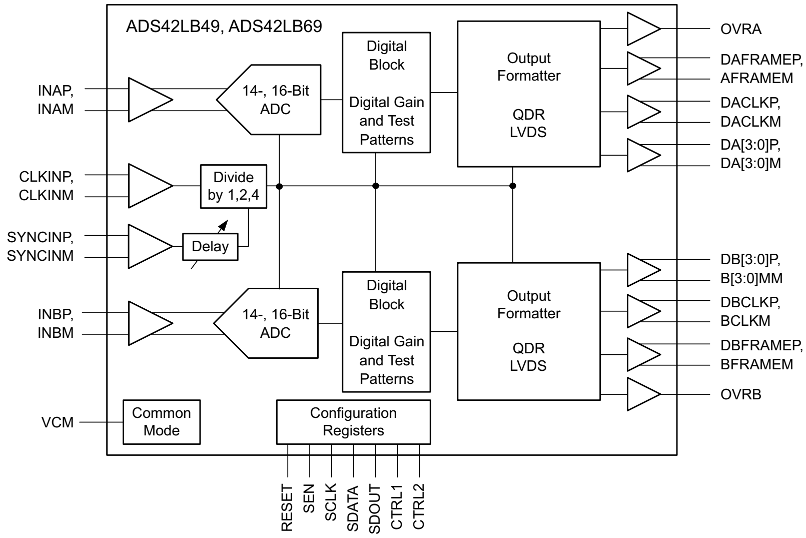


Figure 78. ADS42LB69, ADS42LB49 QDR LVDS

8.3 Feature Description

8.3.1 Digital Gain

The device includes gain settings that can be used to obtain improved SFDR performance (compared to no gain). Gain is programmable from –2 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally. Table 3 shows how full-scale input voltage changes when digital gain are programmed in 1-dB steps. Refer to Table 16 to set digital gain using a serial interface register.

SFDR improvement is achieved at the expense of SNR; for a 1-dB increase in digital gain, SNR degrades approximately between 0.5 dB and 1 dB (refer to Figure 15 and Figure 16). Therefore, gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB with a 2.0-V_{PP} full-scale voltage.

Table 3. Full-Scale Range Across Gains

DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
–2 dB	2.5 V_{PP} (1)
–1 dB	2.2 V_{PP}
0 dB (default)	2.0 V_{PP}
1 dB	1.8 V_{PP}
2 dB	1.6 V_{PP}
3 dB	1.4 V_{PP}
4 dB	1.25 V_{PP}
5 dB	1.1 V_{PP}
6 dB	1.0 V_{PP}

(1) Shaded cells indicate performance settings used in the *Electrical Characteristics* and *Typical Characteristics*.

8.3.2 Input Clock Divider

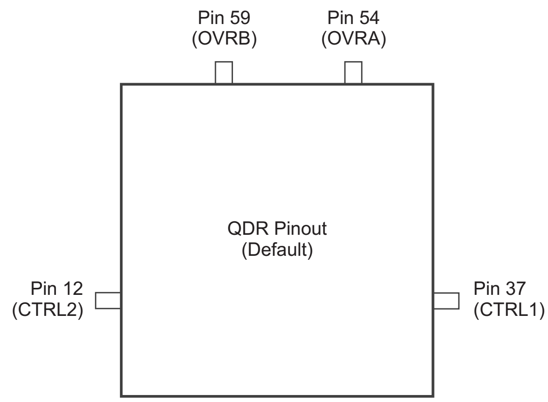
The device is equipped with an internal divider on the clock input. This divider allows operation with a faster input clock, simplifying the system clock distribution design. The clock divider can be bypassed (divide-by-1) for operation with a 250-MHz clock. The divide-by-2 option supports a maximum 500-MHz input clock and the divide-by-4 option supports a maximum 1-GHz input clock frequency.

8.3.3 Overrange Indication

The device provides two different overrange indications: normal OVR and fast OVR. Normal OVR (default) is triggered if the final 16-bit data output exceeds the maximum code value. Normal OVR latency is the same as the output data (that is, 14 clock cycles). Fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after a latency of only nine clock cycles, thus enabling a quicker reaction to an overrange event.

8.3.3.1 OVR in a QDR Pinout

In a QDR interface, the overrange indication is output on the OVRA and OVRB pins (pin 54 and 59) in 1.8-V CMOS logic levels. The same overrange indication can also be made available on the bidirectional CTRL1, CTRL2 pins by using the PDN/OVR FOR CTRL PINS register bit, as described in Figure 79. Using the FAST OVR EN register bit, the fast OVR indication can be presented on these pins instead of normal OVR.



NOTE: By default, normal OVR is output on the OVRA and OVRB pins. Using the FAST OVR EN register bit, fast OVR can be presented on these pins instead.

NOTE: When the PDN/OVR FOR CTRL PINS register bit is set, the CTRL1 and CTRL2 pins function as output pins and carry the same information as the OVRA and OVRB pins (respectively) in 1.8-V CMOS logic levels.

Figure 79. OVR in a QDR Pinout

8.3.3.2 OVR in a DDR Pinout

In the DDR interface, there are no dedicated pins to provide overrange indication. However, by choosing the appropriate register bits, OVR can be transferred on the LSB of 16-bit output data as well as on the bidirectional CTRL1 and CTRL2 pins, as shown in Figure 80.

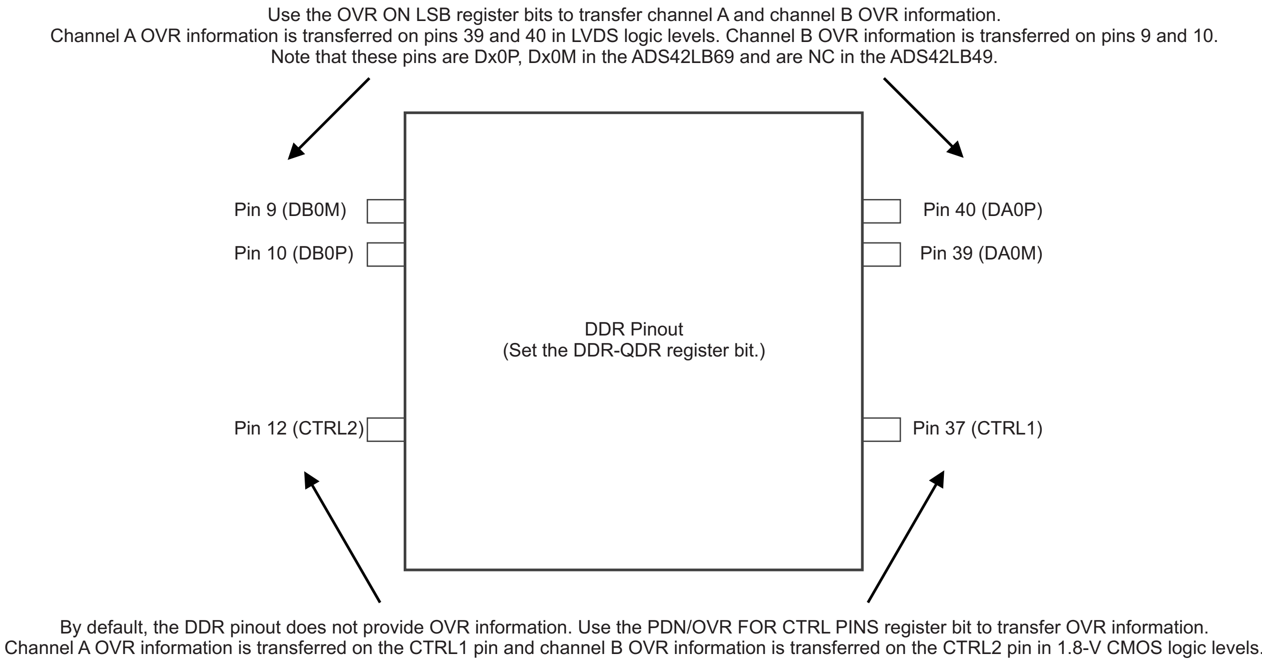


Figure 80. OVR in a DDR Pinout

The FAST OVR EN register bit can be used to transfer fast OVR indication on the CTRL1 and CTRL2 pins instead of normal OVR. The OVR ON LSB register bits can be used to transfer fast OVR indication on the LSB bits (Dx0P, Dx0M), as described in Table 4.

Table 4. Fast OVR Transfer

OVR ON LSB BIT SETTINGS	PIN STATE FOR PINS 9, 10 AND 39, 40
00	D0 and D1 are output in the ADS42LB69, NC for the ADS42LB49
01	Fast OVR in LVDS logic level
10	Normal OVR in LVDS logic level
11	D0 and D1 are output in the ADS42LB69, NC for the ADS42LB49

Table 5 summarizes the availability of OVR information on different pins in the QDR and DDR interfaces and the required register settings.

Table 5. OVR Information Availability

INTERFACE	SETTINGS	OVR INFORMATION AVAILABILITY		
		PINS 9, 10 AND 39, 40 (LVDS Logic Levels)	PINS 12 AND 37 (CMOS Logic Levels)	PINS 54 AND 59 (CMOS Logic Levels)
QDR	Default	Not applicable	No	Yes
	Use the PDN/OVR FOR CTRL PINS register bits	Not applicable	Yes	Yes
DDR	Default	No	No	Not applicable
	Use the OVR ON LSB register bits	Yes	No	Not applicable
	Use the PDN/OVR FOR CTRL PINS register bits	No	Yes	Not applicable
	Use the OVR ON LSB and PDN/OVR FOR CTRL PINS register bits	Yes	Yes	Not applicable

8.3.3.3 Programming Threshold for Fast OVR

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. Fast OVR is triggered nine output clock cycles after the overload condition occurs. The threshold voltage amplitude at which fast OVR is triggered is Equation 1:

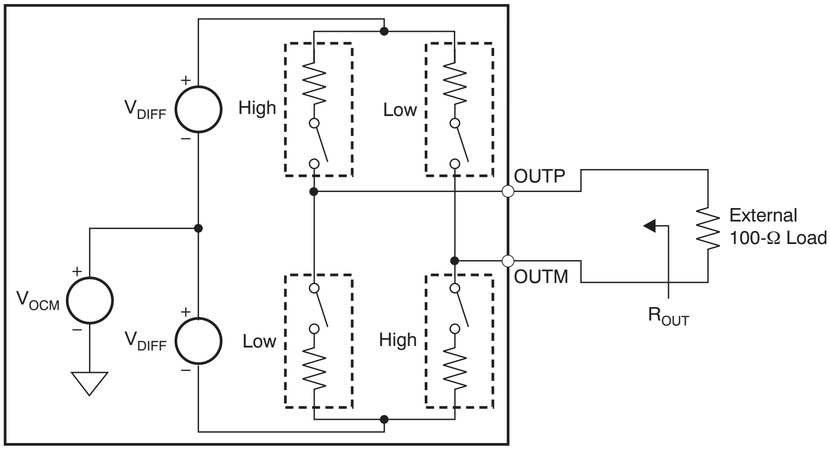
$$1 \times \text{[the decimal value of the FAST OVR THRESH bits]} / 127 \quad (1)$$

When digital gain is programmed (for gain values > 0 dB), the threshold voltage amplitude is Equation 2:

$$10^{-\text{Gain} / 20} \text{ x [the decimal value of the FAST OVR THRESH bits]} / 127 \quad (2)$$

8.3.4 LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 81. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100-Ω termination.



NOTE: Default swing across 100-Ω load is ±350 mV. Use the LVDS SWING bits to change the swing.

Figure 81. LVDS Buffer Equivalent Circuit

The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50-Ω differential termination, as shown in Figure 82. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. The mode can be enabled for LVDS output data (and for the frame clock in the QDR interface) buffers by setting the LVDS DATA STRENGTH register bit. For LVDS output clock buffers (applicable for both DDR and QDR interfaces), set both the LVDS CLKOUT STRENGTH EN and LVDS CLKOUT STRENGTH register bits to '1'.

The buffer output impedance behaves in the same way as a source-side series termination. Absorbing reflections from the receiver end helps improve signal integrity.

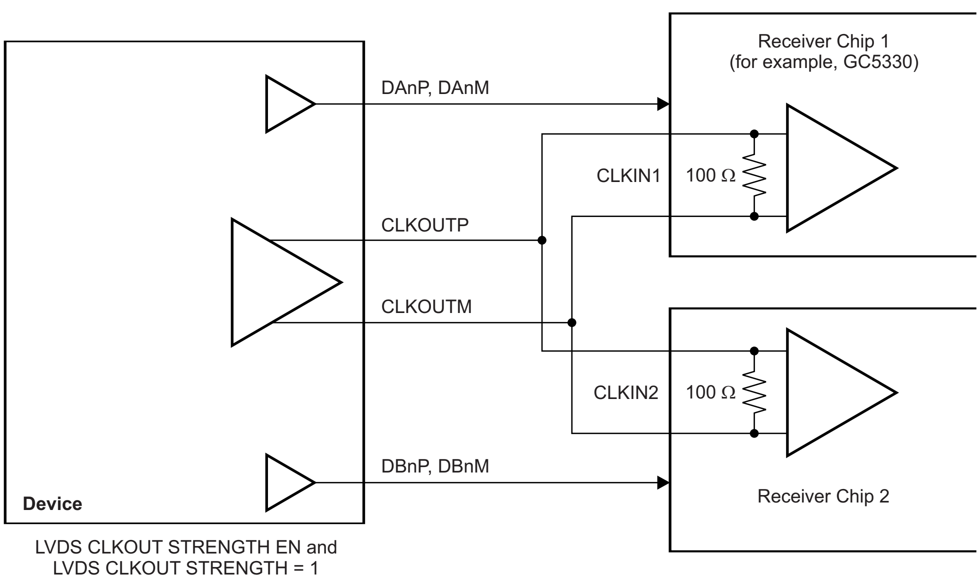


Figure 82. LVDS Buffer Differential Termination

8.3.5 Output Data Format

Two output data formats are supported: twos complement and offset binary. The format can be selected using the DATA FORMAT serial interface register bit.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 3FFFh for the ADS42LB49 and ADS42LB69 in offset binary output format; the output code is 1FFFh for the ADS42LB49 and ADS42LB69 in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 2000h for the ADS42LB49 and ADS42LB69 in twos complement output format.

8.4 Device Functional Modes

8.4.1 Digital Output Information

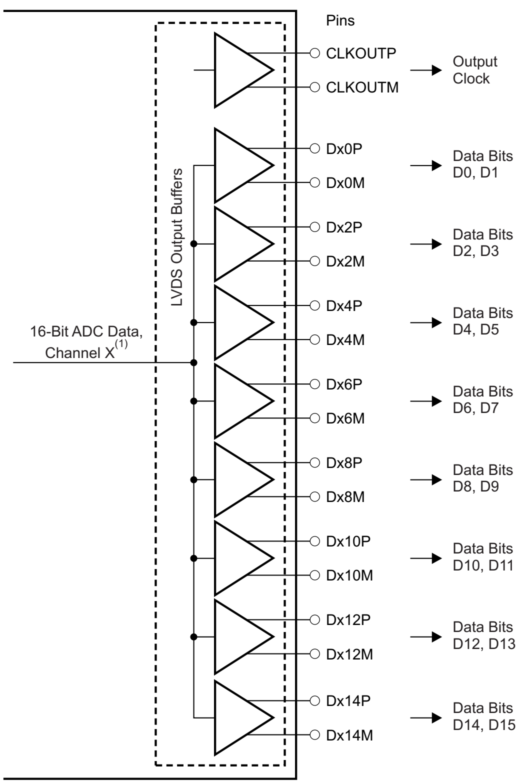
The ADS42LB49 and ADS42LB69 provides 14- and 16-bit digital data for each channel and output clock synchronized with the data.

8.4.1.1 Output Interface

Digital outputs are available in quadruple data rate (QDR) LVDS, and double data rate (DDR) LVDS formats, selectable by the DDR – QDR serial register bit.

8.4.1.2 DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 83.



(1) X = A or B (for channel A or channel B).

Figure 83. DDR LVDS Interface

Device Functional Modes (continued)

Even data bits (D0, D2, D4, and so forth) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, and so forth) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits, as shown in Figure 84.

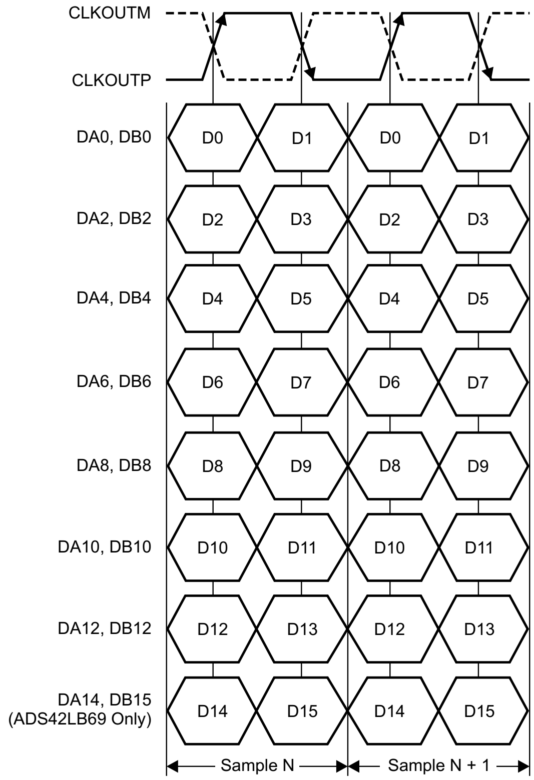
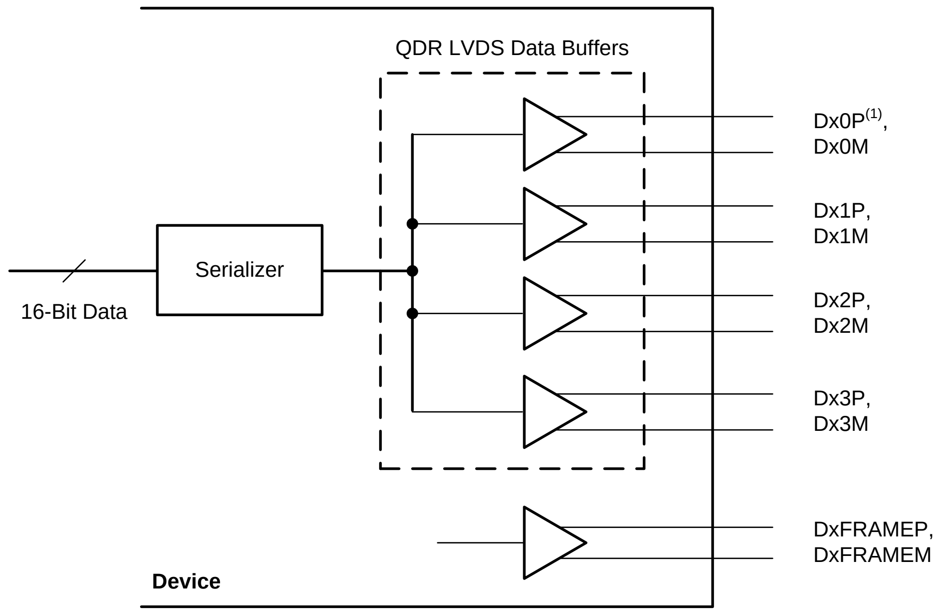


Figure 84. DDR LVDS Interface Timing

Device Functional Modes (continued)

8.4.1.3 QDR LVDS Outputs

The data bits and output clocks are output using low-voltage differential signal (LVDS) levels. Four data bits are multiplexed and output on each LVDS differential data pair and are accompanied by a bit clock and a frame clock for each channel, as shown in Figure 85.



(1) X = channels A and B.

Figure 85. QDR LVDS Interface

Device Functional Modes (continued)

Figure 86 shows the QDR interface bit order for the ADS42LB69 and Figure 87 shows the QDR interface bit order for the ADS42LB49.

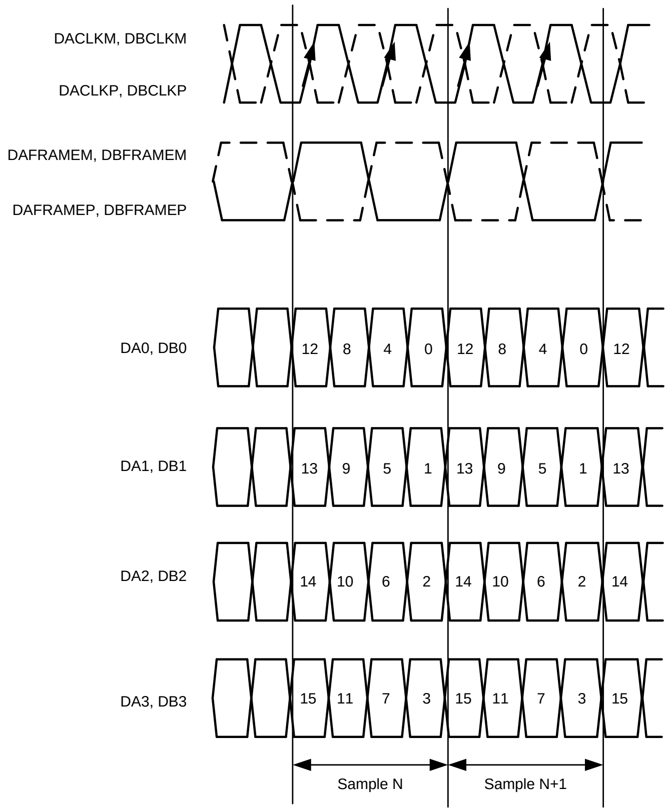


Figure 86. QDR LVDS Interface Timing: ADS42LB69

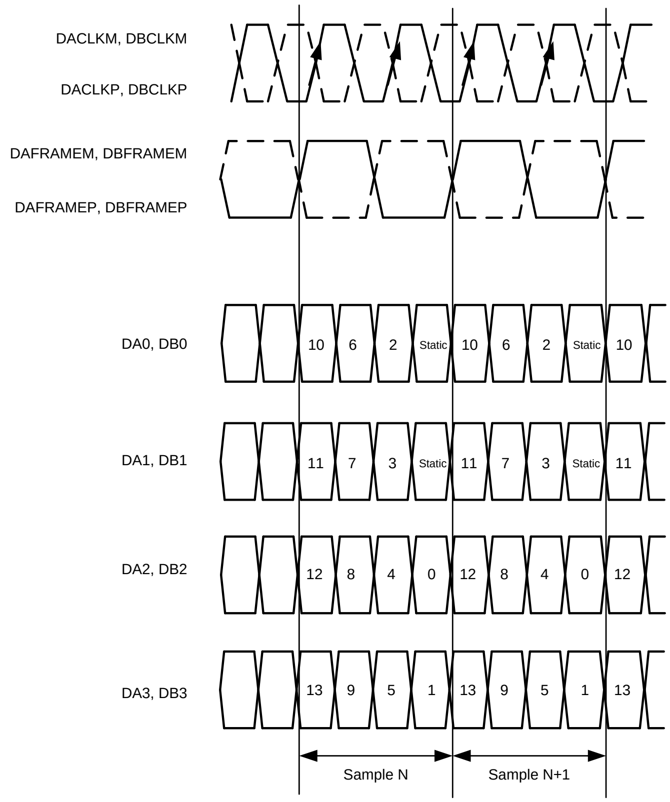


Figure 87. QDR LVDS Interface Timing: ADS42LB49

8.5 Programming

8.5.1 Device Configuration

The ADS42LB49 and ADS42LB69 can be configured using a serial programming interface, as described in this section. In addition, the device has two bidirectional parallel pins (CTRL1 and CTRL2). By default, these pins act as input pins and control the power-down modes, as described in Table 6 and Table 7. These pins can be programmed as output pins that deliver overrange information by setting the PDN/OVR_FOR_CTRL_PINS register bit.

Table 6. PDN/OVR_FOR_CTRL_PINS Bit (Set to '0')

CTRL2	CTRL1	PIN DIRECTION	FUNCTION
Low	Low	Input	Default operation
Low	High	Input	Channel A power-down
High	Low	Input	Channel B powers down in QDR mode. Do not use in DDR mode.
High	High	Input	Channels A and B power-down

Table 7. PDN/OVR_FOR_CTRL_PINS Bit (Set to '1')

CTRL2	CTRL1	PIN DIRECTION
Carries OVR for channel B	Carries OVR for channel A	Output

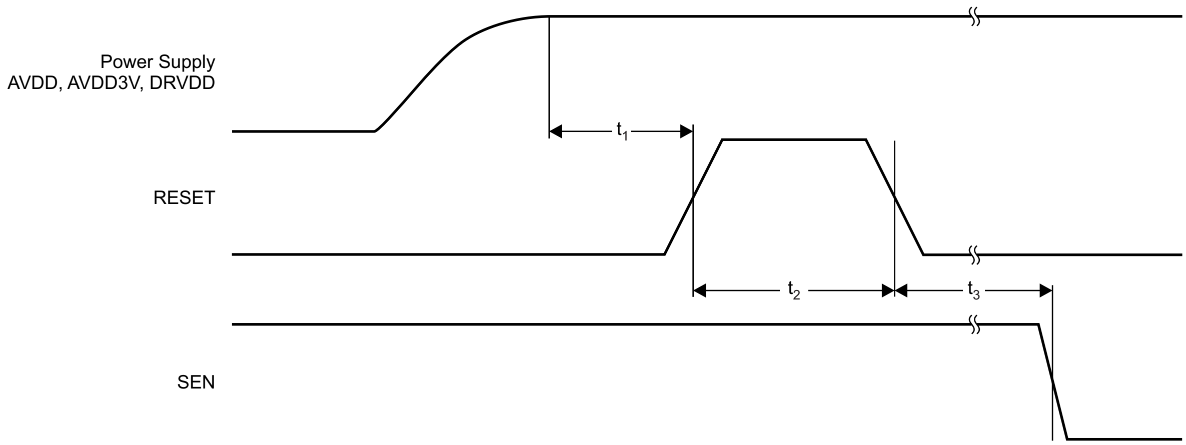
8.5.2 Details of Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and SDOUT (serial interface data output) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The interface can work with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

8.5.2.1 Register Initialization

After power-up, the internal registers must be initialized to their default values through a *hardware reset* by applying a high pulse on the RESET pin (of durations greater than 10 ns); see Figure 88 and Table 8. If required, serial interface registers can later be cleared during operation by:

1. Either through a hardware reset or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 08h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.



NOTE: After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin.

Figure 88. Reset Timing Diagram

Table 8. Reset Timing(1)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

8.5.2.2 Serial Register Write

The internal register of the ADS42LB49 and ADS42LB69 can be programmed following these steps:

1. Drive SEN pin low
2. Set the R/W bit to ‘0’ (bit A7 of the 8 bit address)
3. Set bit A6 in the address field to ‘0’
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content must be written
5. Write 8 bit data which is latched in on the rising edge of SCLK.

Figure 89 and Table 9 illustrate these steps.

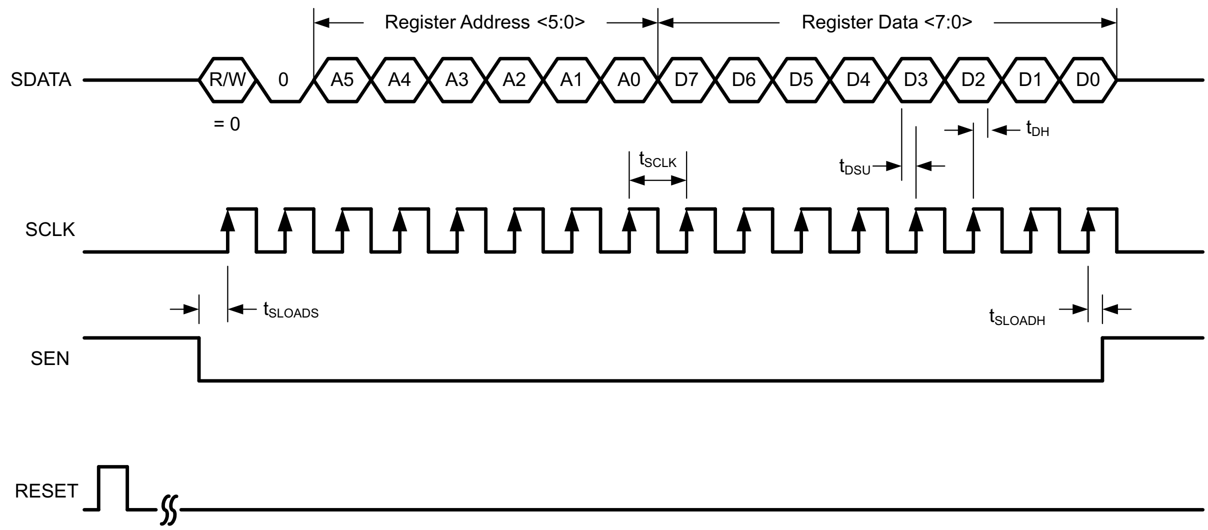


Figure 89. Serial Register Write Timing Diagram

Table 9. Serial Interface Timing (Only when Serial Interface is Used)(1)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD3V = 3.3 V, and AVDD = DRVDD = 1.8 V, unless otherwise noted.

8.5.2.3 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This read-back mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Drive SEN pin low
2. Set the R/W bit (A7) to '1'. This setting disables any further writes to the registers
3. Set bit A6 in the address field to 0.
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content has to be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK falling edge.
7. To enable register writes, reset the R/W register bit to '0'.

Figure 90 illustrates these steps. When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float.

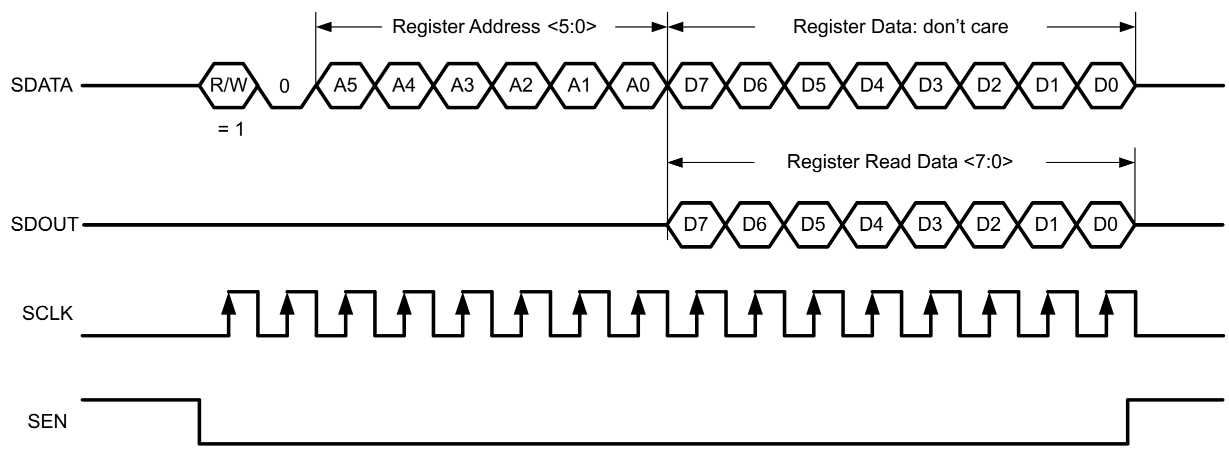


Figure 90. Serial Register Readout Timing Diagram

8.6 Register Maps

The serial interface registers are summarized in Table 10.

Table 10. Summary of Serial Interface Registers

<table>
<tr><th>REGISTER ADDRESS</th><th colspan="8">REGISTER DATA</th></tr>
<tr><th>A[7:0] (Hex)</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>06</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">CLK DIV</td></tr>
<tr><td>07</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">SYNCIN DELAY</td></tr>
<tr><td>08</td><td>PDN CHA</td><td>PDN CHB</td><td>STDBY</td><td>DATA FORMAT</td><td>DIS CTRL PINS</td><td>TEST PAT ALIGN</td><td>0</td><td>RESET</td></tr>
<tr><td>0B</td><td colspan="5">CHA GAIN</td><td>CHA GAIN EN</td><td>0</td><td>FLIP DATA</td></tr>
<tr><td>0C</td><td colspan="5">CHBGAIN</td><td>CHB GAIN EN</td><td colspan="2">OVR ON LSB</td></tr>
<tr><td>0D</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>FAST OVR ON PIN</td></tr>
<tr><td>0F</td><td colspan="4">CHA TEST PATTERNS</td><td colspan="4">CHB TEST PATTERNS</td></tr>
<tr><td>10</td><td colspan="8">CUSTOM PATTERN 1 (15:8)</td></tr>
<tr><td>11</td><td colspan="8">CUSTOM PATTERN 1 (7:0)</td></tr>
<tr><td>12</td><td colspan="8">CUSTOM PATTERN 2 (15:8)</td></tr>
<tr><td>13</td><td colspan="8">CUSTOM PATTERN 2 (7:0)</td></tr>
<tr><td>14</td><td>0</td><td>0</td><td>0</td><td>0</td><td>LVDS CLK STRENGTH</td><td>LVDS DATA STRENGTH</td><td>DISABLE OUTPUT CHA</td><td>DISABLE OUTPUT CHB</td></tr>
<tr><td>15</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DDR – QDR</td></tr>
<tr><td>16</td><td>0</td><td>0</td><td colspan="5">DDR OUTPUT TIMING</td><td>0</td></tr>
<tr><td>17</td><td>LVDS CLK STRENGTH EN</td><td>0</td><td colspan="5">QDR TIMING CHA</td><td>INV CLK OUT CHA</td></tr>
<tr><td>18</td><td>0</td><td>0</td><td colspan="5">QDR TIMING CHB</td><td>INV CLK OUT CHB</td></tr>
<tr><td>1F</td><td>Always write '0'</td><td colspan="7">FAST OVR THRESHOLD</td></tr>
<tr><td>20</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PDN/OVR FOR CTRL PINS</td></tr>
</table>

Table 11. High-Frequency Modes Summary

REGISTER ADDRESS	VALUE	DESCRIPTION
0Dh	90h	Enable high-frequency modes for input frequencies greater than 250 MHz.
0Eh	90h	Enable high-frequency modes for input frequencies greater than 250 MHz.

8.6.1 Description of Serial Interface Registers

8.6.1.1 Register 6 (offset = 06h) [reset = 80h]

Figure 91. Register 6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	CLK DIV	
W-1h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 12. (For example, CONTROL_REVISION Register) Field Descriptions

Bit	Field	Type	Reset	Description
D7	1	W	1h	Always write '1'
D[6:2]	0	W	0h	Always write '0'
D[1:0]	CLK DIV	R/W	0h	Internal clock divider for input sample clock 00 : Divide-by-1 (clock divider bypassed) 01 : Divide-by-2 10 : Divide-by-1 11 : Divide-by-4

8.6.1.2 Register 7 (offset = 07h) [reset = 00h]

Figure 92. Register 7

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	SYNCIN DELAY		
W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h		

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 13. Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:3]	0	W	0h	Always write '0'
D[2:0]	SYNCIN DELAY	R/W	0h	Controls the delay of the SYNCIN input with respect to the input clock. Typical values for the expected delay of different settings are: 000 : 0-ps delay 001 : 60-ps delay 010 : 120-ps delay 011 : 180-ps delay 100 : 240-ps delay 101 : 300-ps delay 110 : 360-ps delay 111 : 420-ps delay

8.6.1.3 Register 8 (offset = 08h) [reset = 00h]

Figure 93. Register 8

D7	D6	D5	D4	D3	D2	D1	D0
PDN CHA	PDN CHB	STDBY	DATA FORMAT	DIS CTRL PINS	TEST PAT ALIGN	0	RESET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 14. Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:6]	PDN CHA, PDN CHB	R/W	0h	Power-down channels A and B. Effective only when bit DIS CTRL PINS is set to '1'. 00 : Normal operation 01 : Channel B powers down. Use only if the QDR interface is selected. Do not use in the DDR interface. 10 : Channel A powers down. Functions in both QDR and DDR interfaces. 11 : Both channels power down. Functions in both QDR and DDR interfaces.
D5	STDBY	R/W	0h	Dual ADC is placed into standby mode 0 : Normal operation 1 : Power down
D4	DATA FORMAT	R/W	0h	Digital output data format 0 : Twos complement 1 : Offset binary
D3	DIS CTRL PINS	R/W	0h	Disables power-down control from the CTRL1, CTRL2 pins. This bit also functions as an enable bit for the INV CLK OUT CHA, INV CLK OUT CHB, and DDR OUTPUT TIMING bits. 0 : CTRL1 and CTRL2 pins control power-down options for channels A and B 1 : The PDN CHA and PDN CHB register bits determine power-down options for channels A and B. The INV CLK OUT CHA, INV CLK OUT CHB, and DDR OUTPUT TIMING register bits become effective.
D2	TEST PAT ALIGN	R/W	0h	Aligns test patterns of two channels 0 : Test patterns for channel A and channel B are free running 1 : Test patterns for both channels are synchronized
D1	0	W	0h	Always write '0'
D0	RESET	R/W	0h	Software reset applied This bit resets all internal registers to the default values and self-clears to ‘0’

8.6.1.4 Register B (offset = 0Bh) [reset = 00h]

Figure 94. Register B

D7	D6	D5	D4	D3	D2	D1	D0
CHA GAIN					CHA GAIN EN	0	FLIP DATA
R/W-0h					R/W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 15. Register B Field Descriptions

Bit	Field	Type	Reset	Description
D[7:3]	CHA GAIN	R/W	0h	Digital gain for channel A. Effective when the CHA GAIN EN register bit is set to '1'. Bit descriptions are listed in Table 16.
D2	CHA GAIN EN	R/W	0h	Digital gain enable bit for channel A 0 : Digital gain disabled 1 : Digital gain enabled
D1	0	W	0h	Always write '0'
D0	FLIP DATA	R/W	0h	Flips bit order on the LVDS output bus (LSB versus MSB) 0 : Normal operation 1 : Output bus flipped. In the ADS42LB69, output data bit D0 becomes D15, D1 becomes D14, and so forth. In the ADS42LB49, output data bit D0 becomes D13, D1 becomes D12, and so forth.

Table 16. Digital Gain for Channel A

DIGITAL GAIN FOR CHANNEL A	DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})		DIGITAL GAIN FOR CHANNEL A	DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})
00000	0	2.0		01010	1.5	1.7
00001	Do not use	—		01011	2	1.6
00010	Do not use	—		01100	2.5	1.5
00011	–2.0	2.5		01101	3	1.4
00100	–1.5	2.4		01110	3.5	1.3
00101	–1.0	2.2		01111	4	1.25
00110	–0.5	2.1		10000	4.5	1.2
00111	0	2.0		10001	5	1.1
01000	0.5	1.9		10010	5.5	1.05
01001	1	1.8		10011	6	1.0

8.6.1.5 Register C (offset = 0Ch) [reset = 00h]

Figure 95. Register C

D7	D6	D5	D4	D3	D2	D1	D0
CHB GAIN					CHB GAIN EN	OVR ON LSB	
R/W-0h					R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 17. Register C Field Descriptions

Bit	Field	Type	Reset	Description
D[7:3]	CHB GAIN	R/W	0h	Digital gain for channel B. Effective when the CHB GAIN EN register bit is set to '1'. Bit descriptions are listed in Table 18.
D2	CHB GAIN EN	R/W	0h	Digital gain enable bit for channel B 0 : Digital gain disabled 1 : Digital gain disabled
D[1:0]	OVR ON LSB	R/W	0h	Functions only with the DDR interface option. Replaces the LSB pair of 16-bit data (D1, D0) with OVR information. See the *Overrange Indication* section. 00 : D1 and D0 are output in the ADS42LB69, NC for the ADS42LB49 01 : Fast OVR in LVDS logic level 10 : Normal OVR in LVDS logic level 11 : D1 and D0 are output in the ADS42LB69, NC for the ADS42LB49

Table 18. Digital Gain for Channel B

DIGITAL GAIN FOR CHANNEL B	DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})		DIGITAL GAIN FOR CHANNEL B	DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})
00000	0	2.0		01010	1.5	1.7
00001	Do not use	—		01011	2	1.6
00010	Do not use	—		01100	2.5	1.5
00011	–2.0	2.5		01101	3	1.4
00100	–1.5	2.4		01110	3.5	1.3
00101	–1.0	2.2		01111	4	1.25
00110	–0.5	2.1		10000	4.5	1.2
00111	0	2.0		10001	5	1.1
01000	0.5	1.9		10010	5.5	1.05
01001	1	1.8		10011	6	1.0

8.6.1.6 Register D (offset = 0Dh) [reset = 6Ch]

Figure 96. Register D

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	1	0	FAST OVR ON PIN
W-0h	W-1h	W-1h	W-0h	W-1h	W-1h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 19. Register D Field Descriptions

Bit	Field	Type	Reset	Description
D7	0	W	0h	Always write '0'
D[6:5]	1	W	1h	Always write '1'
D4	0	W	0h	Always write '0'
D[3:2]	1	W	1h	Always write '1'
D1	0	W	0h	Always write '0'
D0	FAST OVR ON PIN	R/W	0h	Determines whether normal OVR or fast OVR information is brought on the OVRx, CTRL1, and CTRL2 pins. See the *Overrange Indication* section. 0 : Normal OVR available on the OVRx, CTRL1, and CTRL2 pins 1 : Fast OVR available on the OVRx, CTRL1, and CTRL2 pins

8.6.1.7 Register F (offset = 0Fh) [reset = 00h]

Figure 97. Register F

D7	D6	D5	D4	D3	D2	D1	D0
CHA TEST PATTERNS				CHB TEST PATTERNS			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 20. Register F Field Descriptions

Bit	Field	Type	Reset	Description
D[7:4]	CHA TEST PATTERNS	R/W	0h	Channel A test pattern programmability 0000 : Normal operation 0001 : Outputs all 0s 0010 : Outputs all 1s 0011 : Outputs toggle pattern: In the ADS42LB69, data are an alternating sequence of *1010101010101010* and *0101010101010101*. In the ADS42LB49, data alternate between *10101010101010* and *01010101010101*. 0100 : Output digital ramp: In the ADS42LB69, data increment by 1 LSB every clock cycle from code 0 to 65535. In the ADS42LB49 data increment by 1 LSB every fourth clock cycle from code 0 to 16383. 0101 : Increment pattern: Do not use 0110 : Single pattern: In the ADS42LB69, data are the same as programmed by the CUSTOM PATTERN 1[15:0] registers bits. In the ADS42LB49, data are the same as programmed by the CUSTOM PATTERN 1[15:2] register bits. 0111 : Double pattern: In the ADS42LB69, data alternate between CUSTOM PATTERN 1[15:0] and CUSTOM PATTERN 2[15:0]. In the ADS42LB49 data alternate between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2]. 1000 : Deskew pattern: In the ADS42LB69, data are AAAAh. In the ADS42LB49, data are 3AAAh. 1001 : Do not use 1010 : PRBS pattern: Data are a sequence of pseudo-random numbers 1011 : 8-point sine wave: In the ADS42LB69, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 1, 9598, 32768, 55938, 65535, 55938, 32768, and 9598. In the ADS42LB49, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, and 2399.
D[3:0]	CHB TEST PATTERNS	R/W	0h	Channel B test pattern programmability 0000 : Normal operation 0001 : Outputs all 0s 0010 : Outputs all 1s 0011 : Outputs toggle pattern: In the ADS42LB69, data are an alternating sequence of *1010101010101010* and *0101010101010101*. In the ADS42LB49, data alternate between *10101010101010* and *01010101010101*. 0100 : Output digital ramp: In the ADS42LB69, data increment by 1 LSB every clock cycle from code 0 to 65535. In the ADS42LB49 data increment by 1 LSB every fourth clock cycle from code 0 to 16383. 0101 : Increment pattern: Do not use 0110 : Single pattern: In the ADS42LB69, data are the same as programmed by the CUSTOM PATTERN 1[15:0] registers bits. In the ADS42LB49, data are the same as programmed by the CUSTOM PATTERN 1[15:2] register bits. 0111 : Double pattern: In the ADS42LB69, data alternate between CUSTOM PATTERN 1[15:0] and CUSTOM PATTERN 2[15:0]. In the ADS42LB49 data alternate between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2]. 1000 : Deskew pattern: In the ADS42LB69, data are AAAAh. In the ADS42LB49, data are 3AAAh. 1001 : Do not use 1010 : PRBS pattern: Data are a sequence of pseudo-random numbers 1011 : 8-point sine wave: In the ADS42LB69, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 1, 9598, 32768, 55938, 65535, 55938, 32768, and 9598. In the ADS42LB49, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, and 2399.

8.6.1.8 Register 10 (offset = 10h) [reset = 00h]

Figure 98. Register 10

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN 1[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 21. Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:0]	CUSTOM PATTERN 1[15:8]	R/W	0h	Sets the CUSTOM PATTERN 1[15:8] with these bits for both channels

8.6.1.9 Register 11 (offset = 11h) [reset = 00h]

Figure 99. Register 11

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN 1[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 22. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:0]	CUSTOM PATTERN 1[7:0]	R/W	0h	Sets the CUSTOM PATTERN 1[7:0] with these bits for both channels

8.6.1.10 Register 12 (offset = 12h) [reset = 00h]

Figure 100. Register 12

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN 2[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 23. Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:0]	CUSTOM PATTERN 2[15:8]	R/W	0h	Sets the CUSTOM PATTERN 2[15:8] with these bits for both channels

8.6.1.11 Register 13 (offset = 13h) [reset = 00h]

Figure 101. Register 13

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN 2[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 24. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:0]	CUSTOM PATTERN 2[7:0]	R/W	0h	Sets the CUSTOM PATTERN 2[7:0] with these bits for both channels

8.6.1.12 Register 14 (offset = 14h) [reset = 00h]

Figure 102. Register 14

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	LVDS CLK STRENGTH	LVDS DATA STRENGTH	DISABLE OUTPUT CHA	DISABLE OUTPUT CHB
W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 25. Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:4]	0	W	0h	Always write '0'
D3	LVDS CLK STRENGTH	R/W	0h	Increases the LVDS drive strength of the CLKOUTP, CLKOUTM buffers in the DDR pinout and the DxCLKP, DxCLKM buffers in the QDR pinout 0 : LVDS output clock buffer at default strength used with 100-Ω external termination 1 : LVDS output clock buffer has double strength used with 50-Ω external termination. Effective only when the LVDS CLK STRENGTH EN bit is set to '1'.
D2	LVDS DATA STRENGTH	R/W	0h	Increases the LVDS drive strength 0 : LVDS output data buffers (including frame clock buffers in the QDR interface) at default strength used with a 100-Ω external termination 1 : LVDS output data buffers (including frame clock buffers in the QDR interface) at double strength used with a 50-Ω external termination
D1	DISABLE OUTPUT CHA	R/W	0h	Disables LVDS output buffers of channel A 0 : Normal operation 1 : Channel A output buffers are in 3-state
D0	DISABLE OUTPUT CHB	R/W	0h	Disables LVDS output buffers of channel B 0 : Normal operation 1 : Channel B output buffers are in 3-state

8.6.1.13 Register 15 (offset = 15h) [reset = 00h]

Figure 103. Register 15

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	DDR – QDR
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 26. Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:1]	0	W	0h	Always write '0'
D0	DDR – QDR	R/W	0h	Selects output interface between DDR and QDR LVDS mode 0 : QDR LVDS mode 1 : DDR LVDS mode

8.6.1.14 Register 16 (offset = 16h) [reset = 00h]

Figure 104. Register 16

D7	D6	D5	D4	D3	D2	D1	D0
0	0	DDR OUTPUT TIMING					0
W-0h	W-0h	R/W-0h					W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 27. Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:6]	0	W	0h	Always write '0'
D[5:1]	DDR OUTPUT TIMING	R/W	0h	Effective only when the DIS CTRL PINS bit is set to '1'. Bit descriptions are listed in Table 28.
D0	0	W	0h	Always write '0'

Table 28. DDR Output Timing (After Setting Bits DIS CTRL PINS To '1')

BIT SETTING	DELAY (ps) IN OUTPUT CLOCK WITH RESPECT TO DEFAULT POSITION			
	f_S = 250 MSPS	f_S = 200 MSPS	f_S = 150 MSPS	f_S = 100 MSPS
00101	–180	–220	–310	–440
00111	–100	–130	–190	–260
00000	0	0	0	0
01101	120	130	170	260
01110	230	240	330	520
01011	320	360	480	740
10100	400	460	620	940
10000	500	600	790	1220

8.6.1.15 Register 17 (offset = 17h) [reset = 00h]

Figure 105. Register 17

D7	D6	D5	D4	D3	D2	D1	D0
LVDS CLK STRENGTH EN	0	QDR OUTPUT TIMING CHA					INVCLK OUT CHA
R/W-0h	W-0h	R/W-0h					R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 29. Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
D7	LVDS CLK STRENGTH EN	R/W	0h	0 : Default 1 : Enables clock strength programmability with the LVDS CLK STRENGTH bit
D6	0	W	0h	Always write '0'
D[5:1]	QDR OUTPUT TIMING CHA	R/W	0h	Adjusts position of output data clock on channel A with respect to output data. Bit settings are listed in Table 30.
D0	INV CLK OUT CHA	R/W	0h	Inverts polarity of the output clock for channel A (QDR mode only) 0 : Normal operation 1 : Polarity of channel A output clock DACLKP, DACLKM is inverted. Effective only when the DIS CTRL PINS bit is set to '1'.

Table 30. QDR Timing Channel A Timing

BIT SETTING	DELAY (ps) IN OUTPUT CLOCK WITH RESPECT TO DEFAULT POSITION			
	f_S = 250 MSPS	f_S = 200 MSPS	f_S = 150 MSPS	f_S = 100 MSPS
00101	–80	–120	–150	–225
00111	–55	–75	–90	–130
00000	0	0	0	0
01101	55	65	90	130
01110	95	115	165	235
01011	140	165	230	350
10100	180	220	290	450
10000	230	290	370	565

8.6.1.16 Register 18 (offset = 18h) [reset = 00h]

Figure 106. Register 18

D7	D6	D5	D4	D3	D2	D1	D0
0	0	QDR OUTPUT TIMING CHB					INVCLK OUT CHB
W-0h	W-0h	R/W-0h					R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 31. Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:6]	0	W	0h	Always write '0'
D[5:1]	QDR OUTPUT TIMING CHB	R/W	0h	Adjusts position of output data clock on channel B with respect to output data. Bit settings are listed in Table 32.
D0	INV CLK OUT CHB	R/W	0h	Inverts output clock polarity for channel B in QDR mode, or output clock CLKOUTP, CLKOUTM in DDR mode. 0 : Normal operation 1 : In QDR mode, the polarity of the channel B output clock DBCLKP, DBCLKM is inverted. Effective only when the DIS CTRL PINS bit is set to '1'. In DDR mode, the output clock polarity of CLKOUTP, CLKOUTM is inverted.

Table 32. QDR Timing Channel B Timing

BIT SETTING	DELAY (ps) IN OUTPUT CLOCK WITH RESPECT TO DEFAULT POSITION			
	f_S = 250 MSPS	f_S = 200 MSPS	f_S = 150 MSPS	f_S = 100 MSPS
00101	–80	–120	–150	–225
00111	–55	–75	–90	–130
00000	0	0	0	0
01101	55	65	90	130
01110	95	115	165	235
01011	140	165	230	350
10100	180	220	290	450
10000	230	290	370	565

8.6.1.17 Register 1F (offset = 1Fh) [reset = 7Fh]

Figure 107. Register 1F

D7	D6	D5	D4	D3	D2	D1	D0
0	FAST OVR THRESHOLD						
W-0h	R/W-0h						

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 33. Register 1F Field Descriptions

Bit	Field	Type	Reset	Description
D7	0	W	1h	Always write '0' Default value of this bit is '1'. Always write this bit to '0' when fast OVR thresholds are programmed.
D[6:0]	FAST OVR THRESHOLD	R/W	0h	The device has a fast OVR mode that indicates an overload condition at the ADC input. The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered nine output clock cycles after the overload condition occurs. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESHOLD bits] / 127). See the *Overrange Indication* section for details.

8.6.1.18 Register 20 (offset = 20h) [reset = 00h]

Figure 108. Register 20

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	PDN/OVR FOR CTRL PINS
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 34. Register 20 Field Descriptions

Bit	Field	Type	Reset	Description
D[7:1]	0	W	0h	Always write '0'
D0	PDN/OVR FOR CTRL PINS	R/W	0h	Determines if the CTRL1, CTRL2 pins are power-down control or OVR outputs 0 : CTRL1 and CTRL2 pins function as input pins to control power-down operation. 1 : CTRL1 and CTRL2 pins function as output pins for overrange indications of channels A and B, respectively. The PDN CH A, PDN CH B register bits along with DIS CTRL PINS can be used for power-down operation.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

To obtain the best performance in an application, careful consideration must be given to the design of the input analog circuit and common-mode, clock circuit, and power-supply rails. The *Typical Application* section discusses these critical design considerations in detail.

9.2 Typical Application

Because the ADS42LBx9 is a dual-channel device, it can be used in a dual-channel superheterodyne receiver, as shown in Figure 109. In a superheterodyne receiver, the high-frequency RF signal is first mixed down to a lower Intermediate frequency (IF). The ADS42LBxx can be used in the IF stage to sample and digitize the IF signal. The digital data can be encoded either in offset binary or twos complement format and transmitted to a field-programmable gate array (FPGA) or application-specific integrated circuit (ASIC). Inside the FPGA or ASIC, the digital data are down-converted to the baseband frequency with a digital mixer and numerically controlled oscillator (NCO).

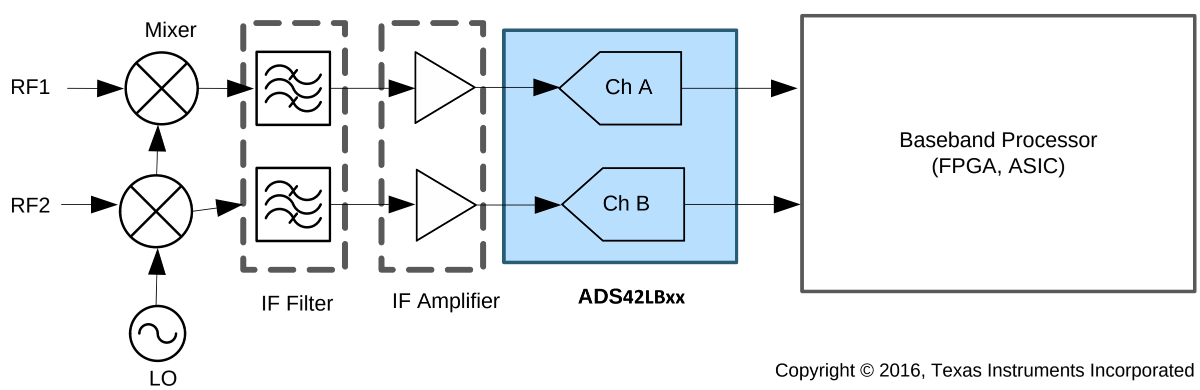


Figure 109. The ADS42LBx9 in a Dual-Channel Superheterodyne Receiver

9.2.1 Design Requirements

Specific design requirements are provided in Table 35.

Table 35. ADS42LBx9 Design Requirements

DESIGN PARAMETER	VALUE
$f_{SAMPLING}$	250 MSPS
IF	10 MHz (Figure 123), 170 MHz (Figure 124)
SNR	> 72 dBc
SFDR	> 80 dBc
HDn	> 90 dBc

9.2.2 Detailed Design Procedure

The choice of drive circuit at the analog and clock inputs can degrade the performance of the ADC. In order to obtain the design specifications given in Table 35, the following design guidelines discussed in this section must be followed.

9.2.2.1 Analog Input

The analog input pins have analog buffers (running from the AVDD3V supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (at dc, a 10-kΩ differential input resistance is provided in shunt with a 4-pF differential input capacitance). The buffer helps isolate the external driving source from the switching currents of the sampling circuit. This buffering makes driving the buffered inputs easier than when compared to an ADC without the buffer.

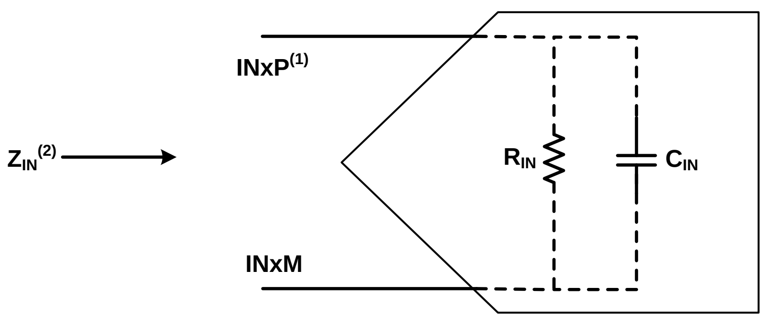
The input common-mode is set internally using a 5-kΩ resistor from each input pin to VCM so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. When programmed for 2.5-V_{PP} full-scale, each input pin must swing symmetrically between VCM + 0.625 V and VCM – 0.625 V.

The input sampling circuit has a high 3-dB bandwidth that extends up to 900 MHz (measured with a 50-Ω source driving a 50-Ω termination between INP and INM). The dynamic offset of the first-stage sub-ADC limits the maximum analog input frequency to approximately 250 MHz (with a 2.5-V_{PP} full-scale amplitude) and to approximately 400 MHz (with a 2-V_{PP} full-scale amplitude). This maximum analog input frequency is different than the analog bandwidth of 900 MHz, which is only an indicator of signal amplitude versus frequency.

9.2.2.1.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 110, Figure 111, and Figure 112 show the differential impedance ($Z_{IN} = R_{IN} || C_{IN}$) at the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1 GHz.



(1) X = A or B.

(2) $Z_{IN} = R_{IN} || (1 / j\omega C_{IN})$.

Figure 110. ADC Equivalent Input Impedance

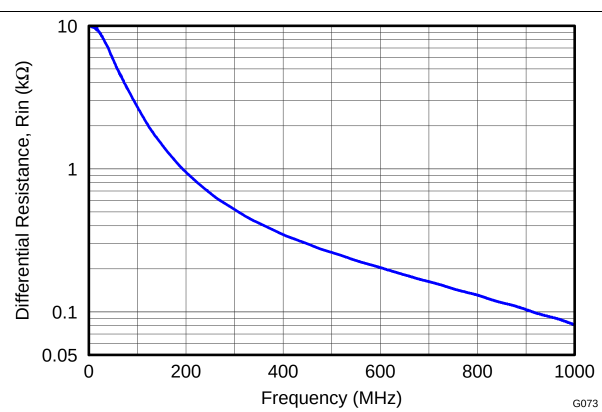


Figure 111. ADC Analog Input Resistance (R_{IN}) Across Frequency

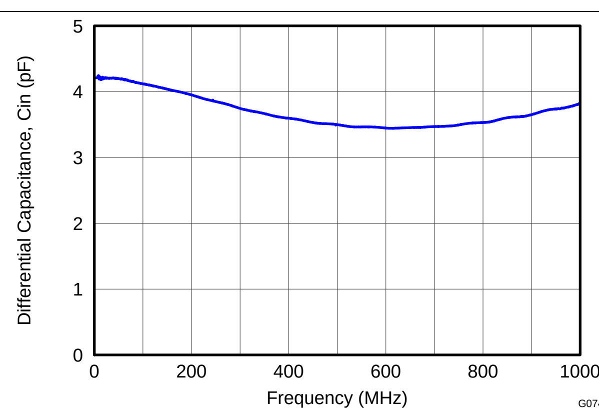


Figure 112. ADC Analog Input Capacitance (C_{IN}) Across Frequency

9.2.2.1.2 Driving Circuit

An example driving circuit configuration is shown in Figure 113. To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended, as shown in Figure 113. Note that the drive circuit is terminated by 50 Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage. If HD2 optimization is a concern, using a 10-Ω series resistor on the INP side and a 9.5-Ω series resistor on the INM side may help improve HD2 by 2 dB to 3 dB at a 85-dBFS level on a 170-MHz IF. An additional R-C-R (39 Ω - 6.8 pF - 39 Ω) circuit placed near device pins helps further improve HD3.

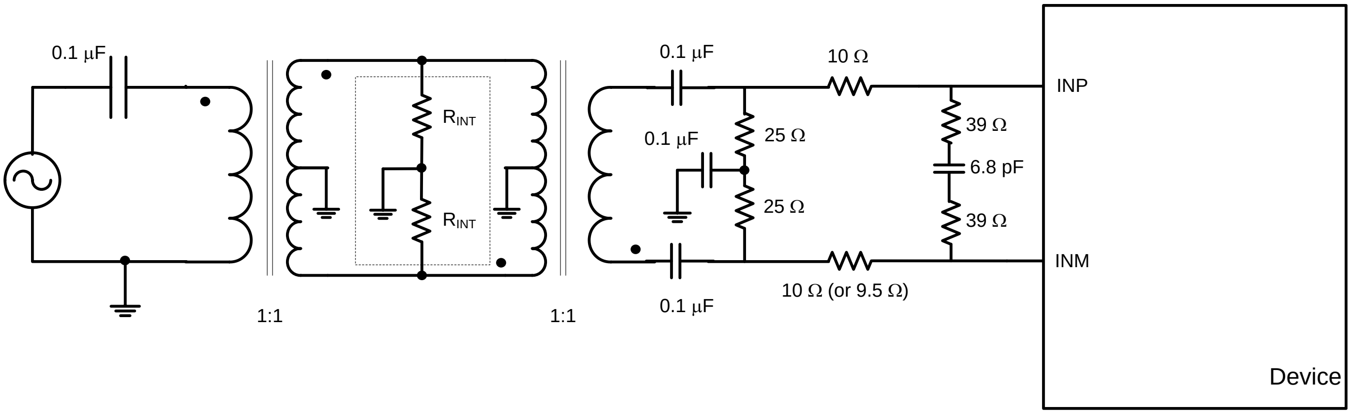


Figure 113. Drive Circuit for Input Frequencies up to 250 MHz

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 113. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance). For high input frequencies (>250MHz), the R-C-R circuit can be removed as indicated in Figure 114.

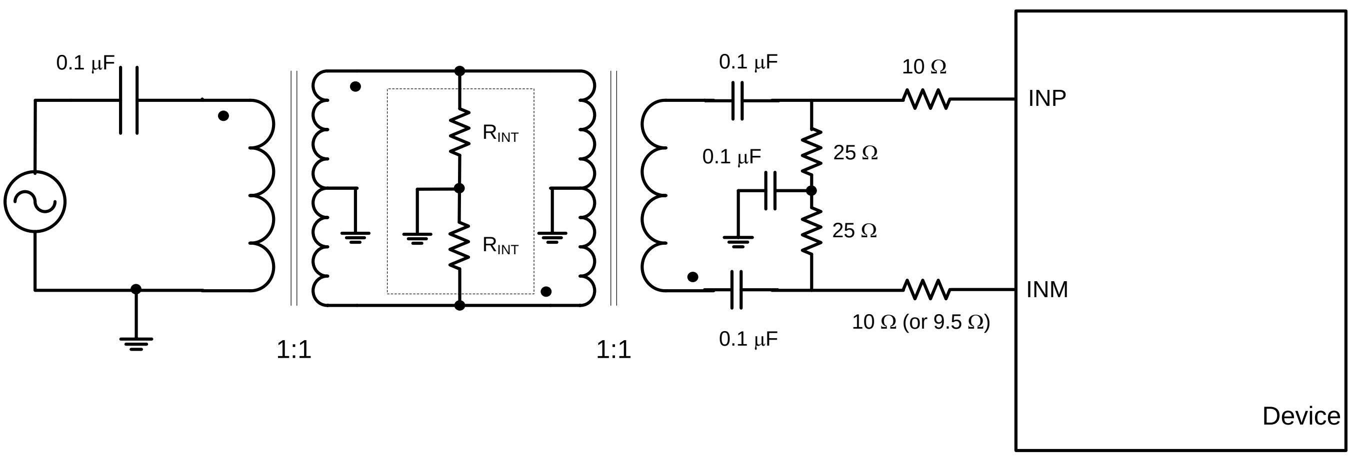


Figure 114. Drive Circuit for Input Frequencies > 250 MHz

9.2.2.1.3 Using the ADS42LBx9 In Time-Domain, Low-Frequency Pulse Applications

The analog buffers inside the device are implemented to provide excellent linearity over a wide range of frequencies. However, at very low frequencies (< 100 kHz) the buffer presents a high-pass response, as shown in Figure 115 and Figure 116. This response does not affect most frequency-domain applications, but can require compensation techniques for time-domain, dc-coupled applications. Application report SBAA220 discusses simple techniques to compensate for the analog buffer response.

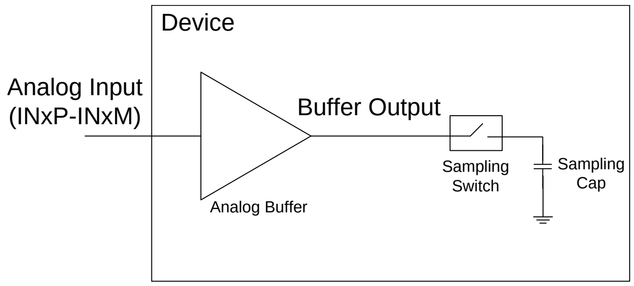


Figure 115. Analog Buffer in the ADS42LBx9

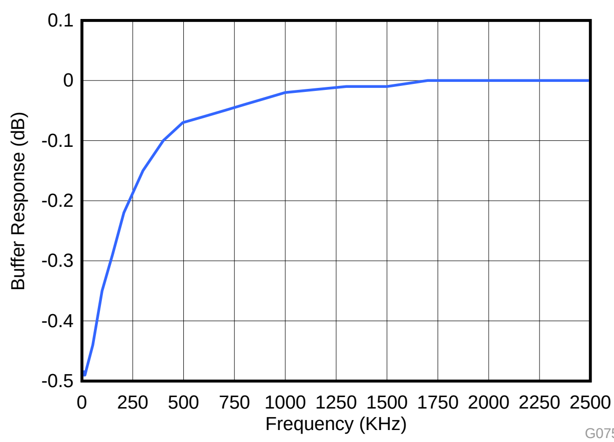


Figure 116. Buffer Response at Very Low Input Frequencies

9.2.2.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 1.4 V using internal 5-kΩ resistors. The self-bias clock inputs of the ADS42LB69 and ADS42LB49 can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 117, Figure 118, and Figure 119. Figure 119 details the internal clock buffer.

Note: R_T = termination resistor, if necessary.

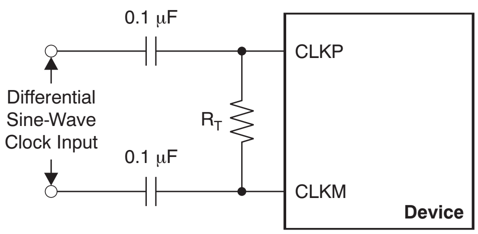


Figure 117. Differential Sine-Wave Clock Driving Circuit

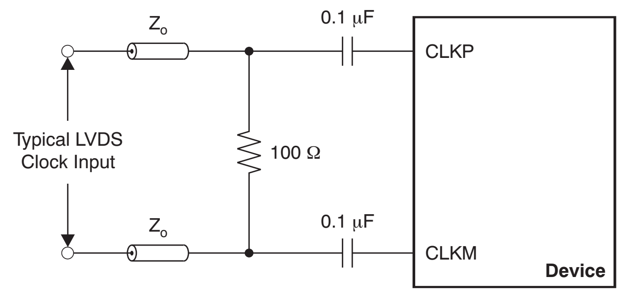


Figure 118. LVDS Clock Driving Circuit

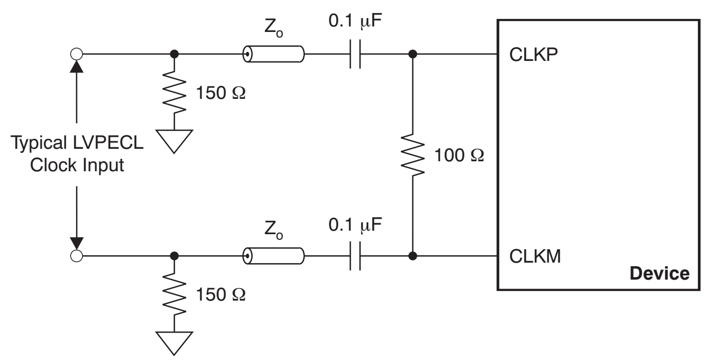
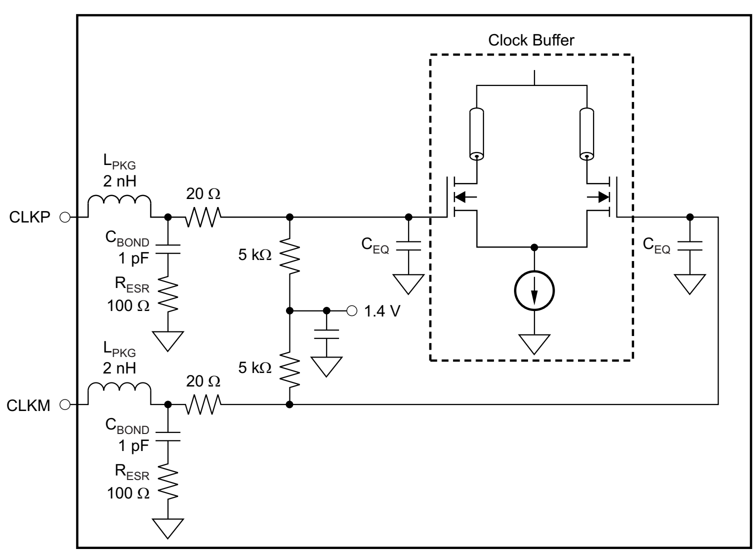


Figure 119. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 120. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 121. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

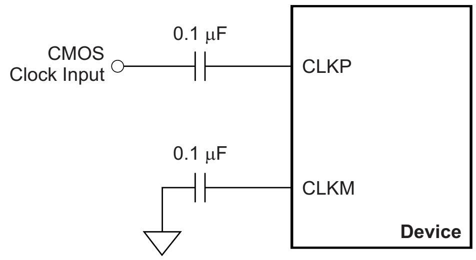


Figure 121. Single-Ended Clock Driving Circuit

9.2.2.3 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors, as shown in Equation 3. Quantization noise is typically not noticeable in pipeline converters and is 96 dBFS for a 16-bit ADC. Thermal noise limits SNR at low input frequencies and clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10^{-\frac{SNR_{Quantization\_Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{ThermalNoise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (3)$$

SNR limitation is a result of sample clock jitter and can be calculated by Equation 4:

$$SNR_{Jitter}\,[dBc] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}) \quad (4)$$

The total clock jitter (T_{Jitter}) has three components: the internal aperture jitter (85 f_S for the device) is set by the noise of the clock input buffer, the external clock jitter, and the jitter from the analog input signal. T_{Jitter} can be calculated by Equation 5:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (5)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improves ADC aperture jitter. The device has a 74.1-dBFS thermal noise and an 85-f_S internal aperture jitter. The SNR value depends on the amount of external jitter for different input frequencies, as shown in Figure 122.

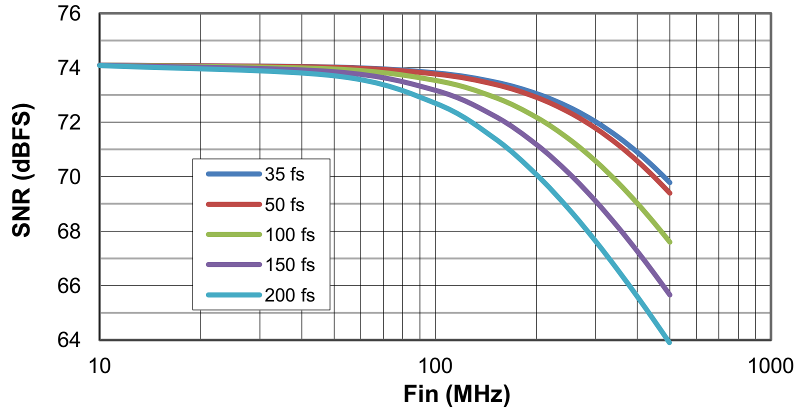


Figure 122. SNR versus Input Frequency and External Clock Jitter

9.2.3 Application Curves

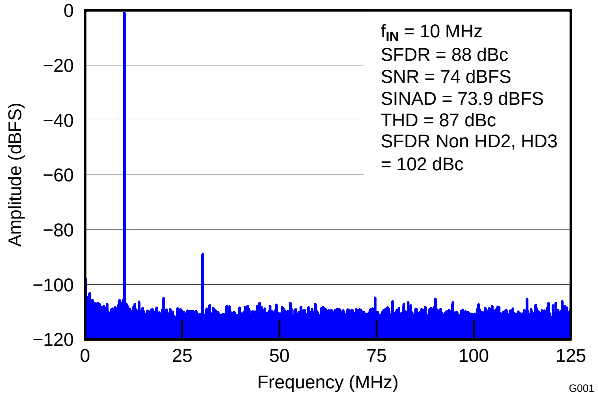


Figure 123. FFT for 10-MHz Input Signal

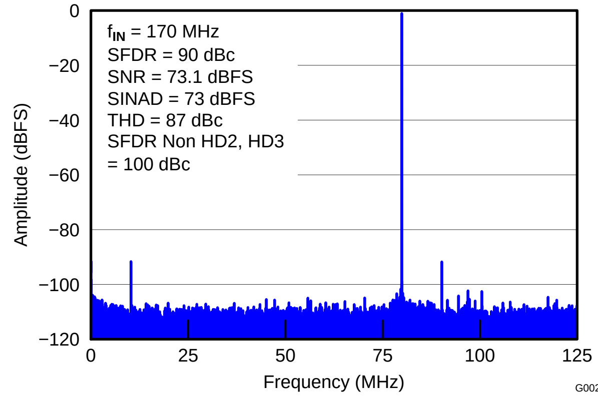


Figure 124. FFT for 170-MHz Input Signal

10 Power Supply Recommendations

Three different power-supply rails are required for the ADS42LBx9:

- A 3.3-V AVDD is used to power the analog buffers.
- A 1.8-V AVDD is used to power the analog core of the ADC.
- A 1.8-V DRVDD is used to power the digital core of the ADC.

TI recommends providing the 1.8-V digital and analog supplies from separate sources because of the switching activities on the digital rail. An example power-supply scheme suitable for the ADS42LBx9 device family is shown in Figure 125. In this example supply scheme, AVDD is provided from a dc-dc converter and an low-dropout (LDO) regulator to increase the efficiency of the implementation. Where cost and area rather than power-supply efficiency are the main design goals, AVDD can be provided using only the LDO.

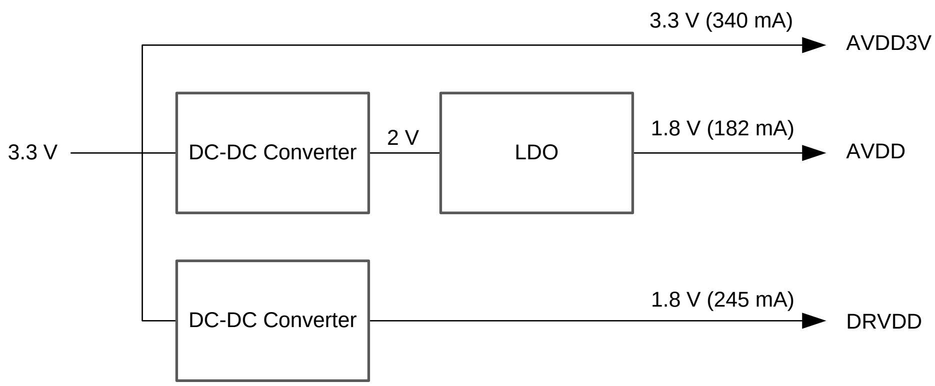


Figure 125. Example Power-Supply Scheme

11 Layout

11.1 Layout Guidelines

- The length of the positive and negative traces of a differential pair must be matched to within 2 mils of each other.
- Each differential pair length must be matched within 10 mils of each other.
- When the ADC is used on the same printed circuit board (PCB) with a digital intensive component [such as a field-programmable gate array (FPGA) or application-specific integrated circuit (ASIC)], use separate digital and analog ground planes to minimize undesired coupling. Note that these ground planes must not overlap.
- Connect decoupling capacitors directly to ground and place these capacitors close to the ADC power pins and the power-supply pins to filter high-frequency current transients directly to the ground plane, as illustrated in Figure 126.
- Ground and power planes must be wide enough to keep the impedance very low. In a multilayer PCB, dedicate one layer to ground and another to power planes.

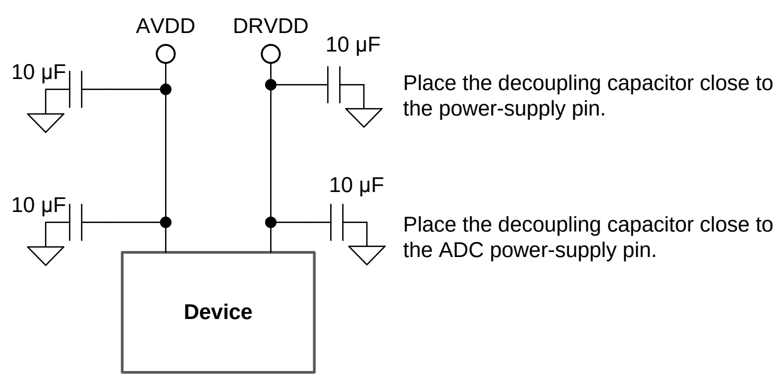


Figure 126. Recommended Placement of Power-Supply Decoupling Capacitors

11.2 Layout Example

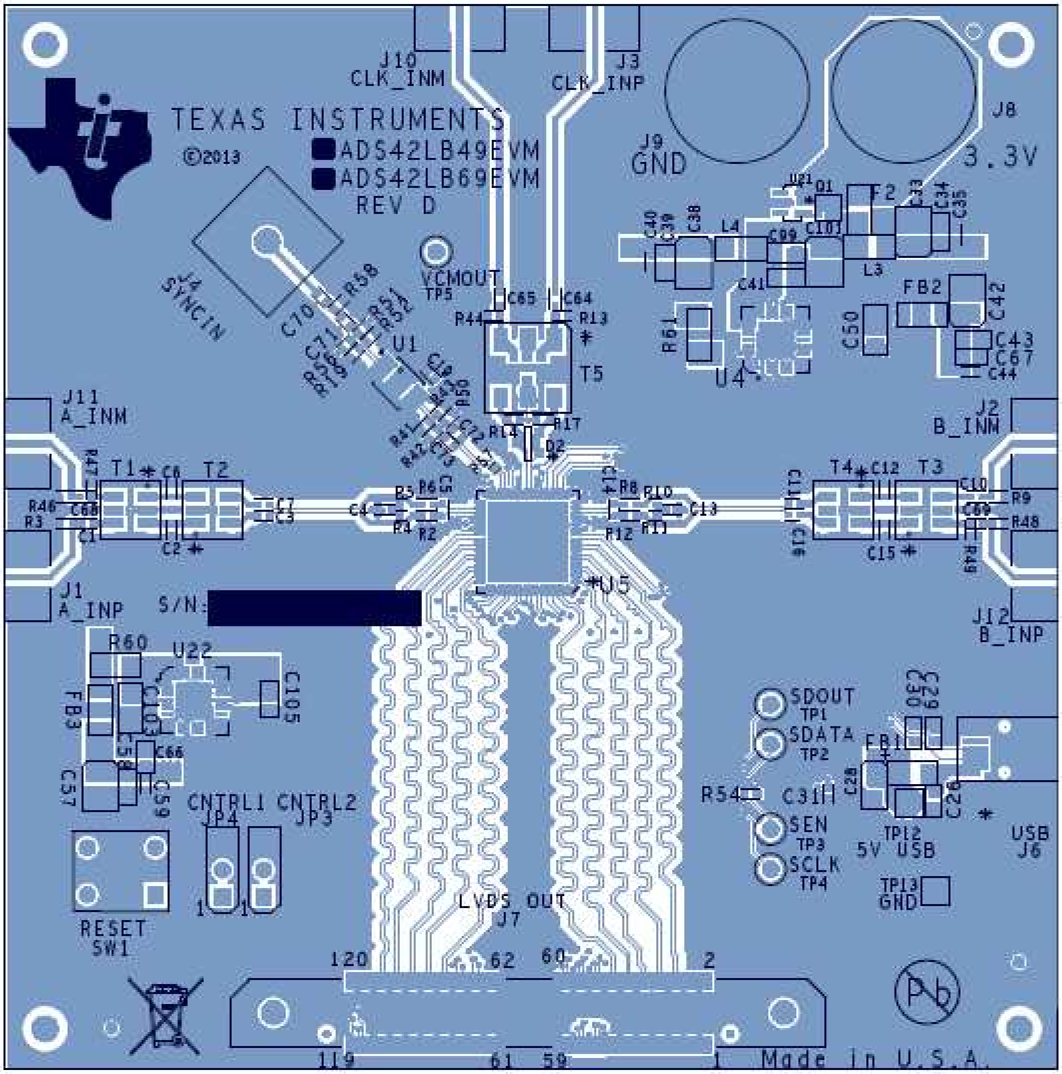


Figure 127. Example Layout

Layout Example (continued)

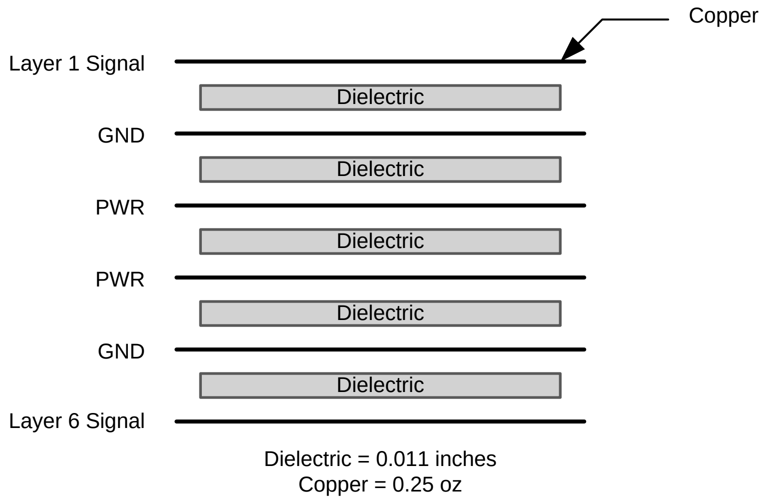


Figure 128. Example PCB Layer Stack

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 36. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS42LB49	Click here	Click here	Click here	Click here	Click here
ADS42LB69	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS42LB49IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB49	Samples
ADS42LB49IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB49	Samples
ADS42LB49IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB49	Samples
ADS42LB69IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB69	Samples
ADS42LB69IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB69	Samples
ADS42LB69IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB69	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

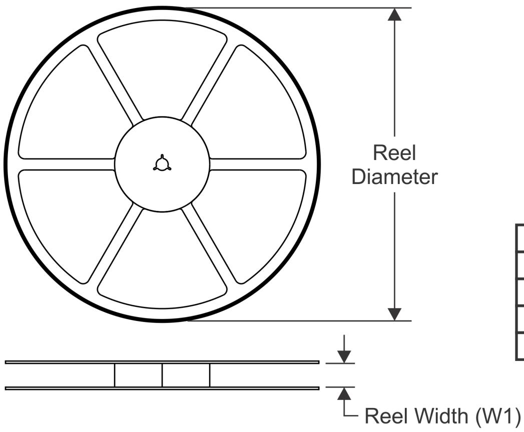
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

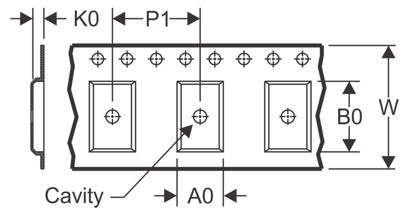
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

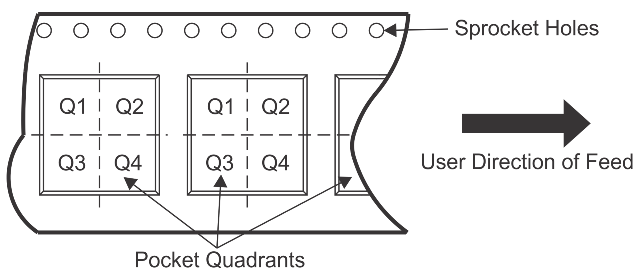


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

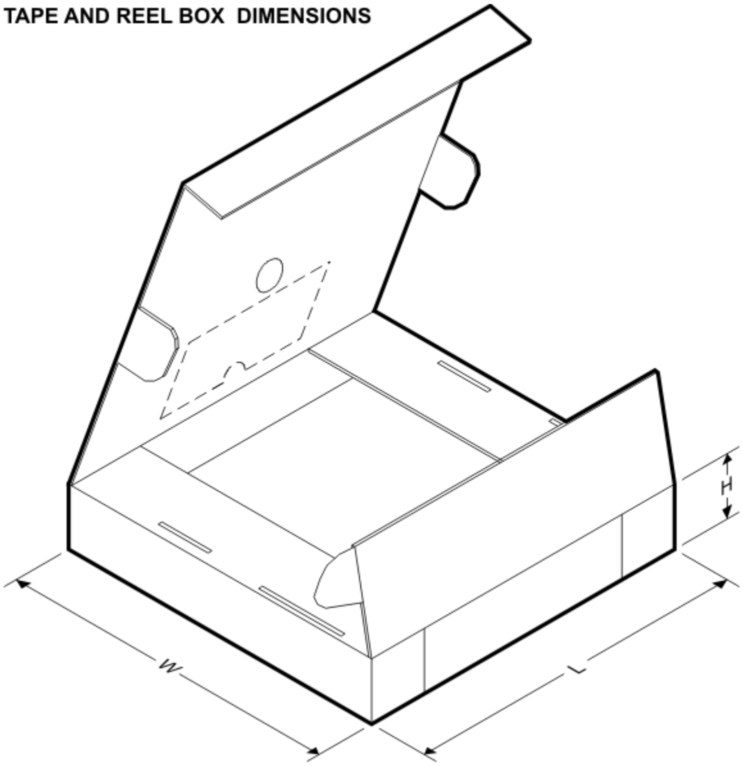
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS42LB49IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42LB49IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42LB69IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42LB69IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

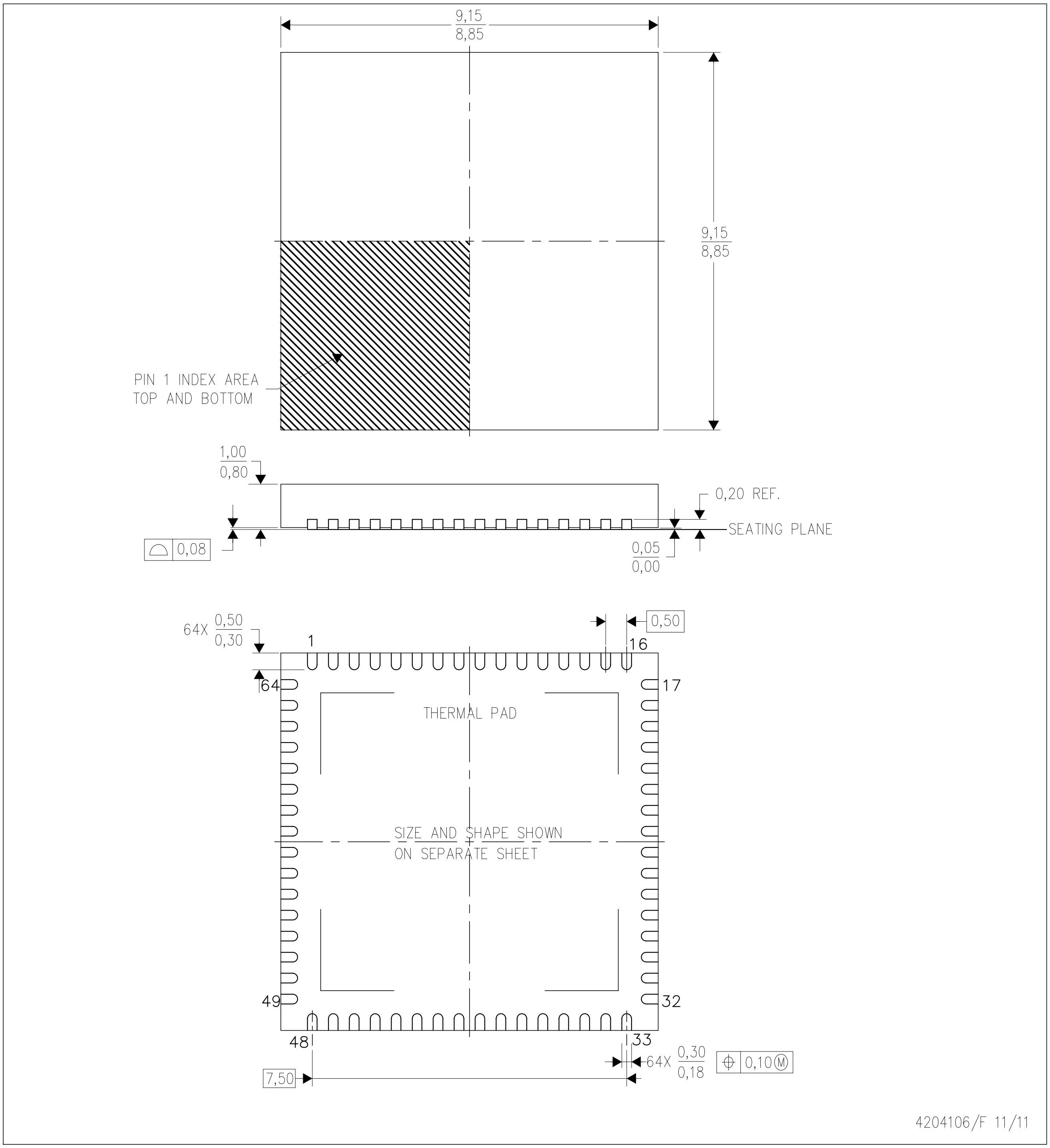
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS42LB49IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS42LB49IRGCT	VQFN	RGC	64	250	213.0	191.0	55.0
ADS42LB69IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS42LB69IRGCT	VQFN	RGC	64	250	213.0	191.0	55.0

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

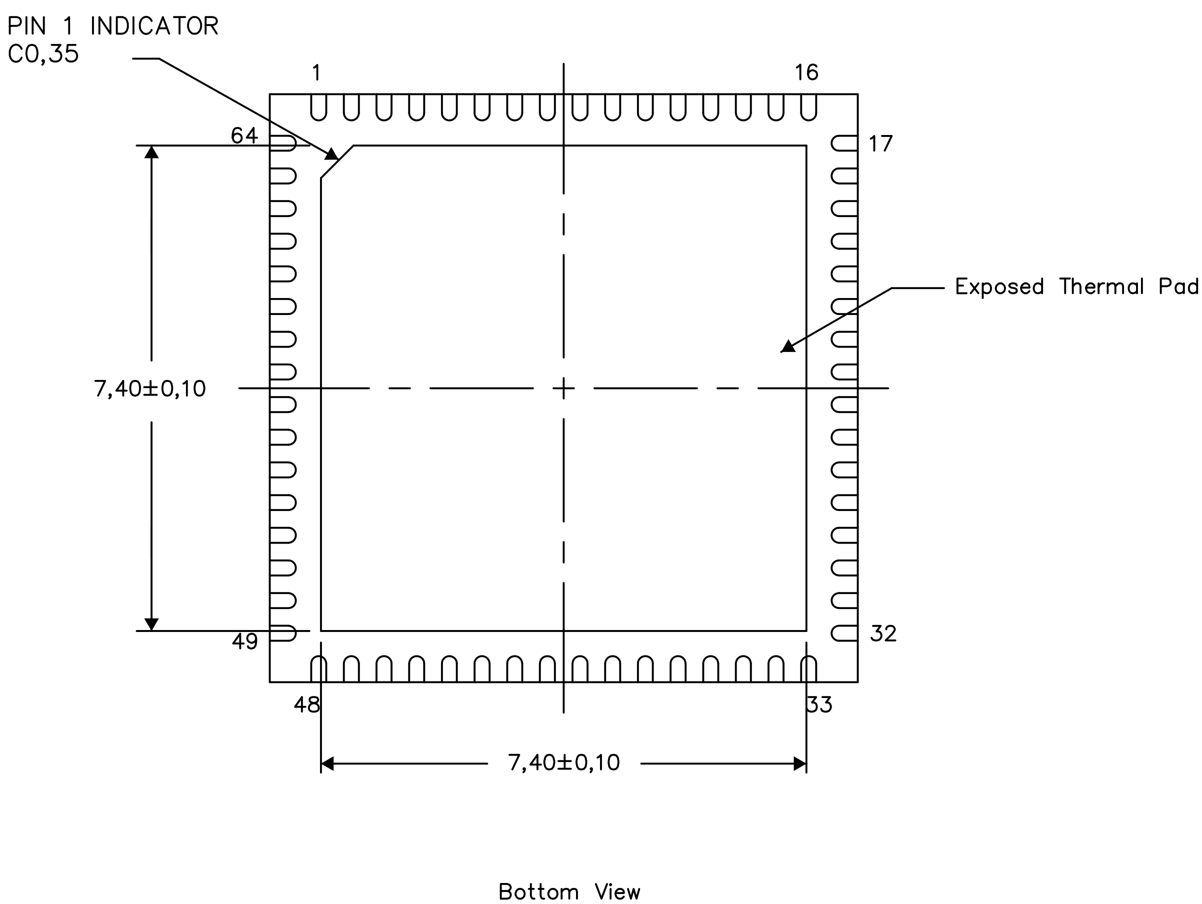
RGC (S-PVQFN-N64) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

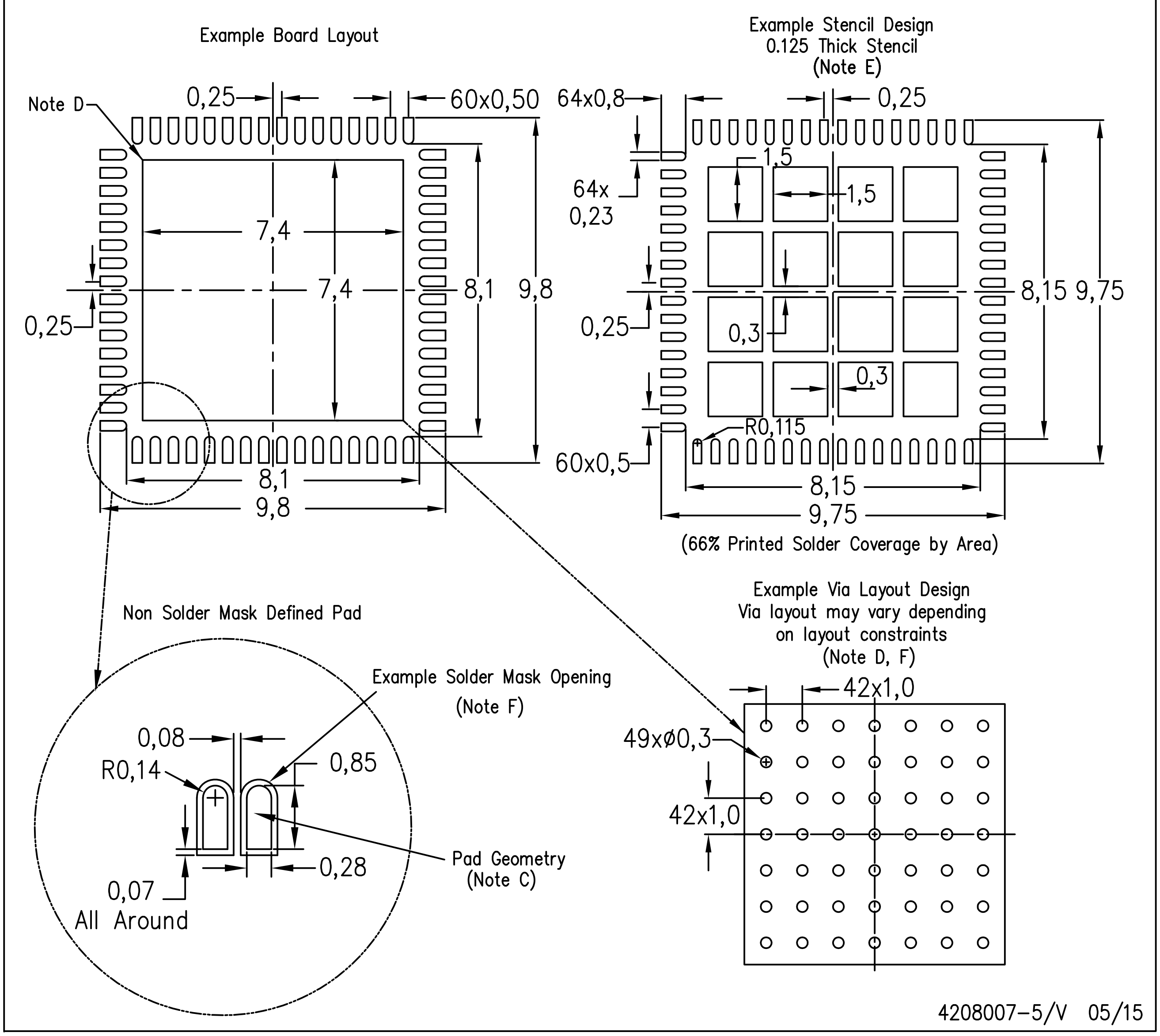


Exposed Thermal Pad Dimensions

4206192-4/AE 03/15

NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.