VOICE OTP IC

aP89682K – 682sec

aP89341K – 341sec

aP89170K – 170sec

aP89085K – 85sec

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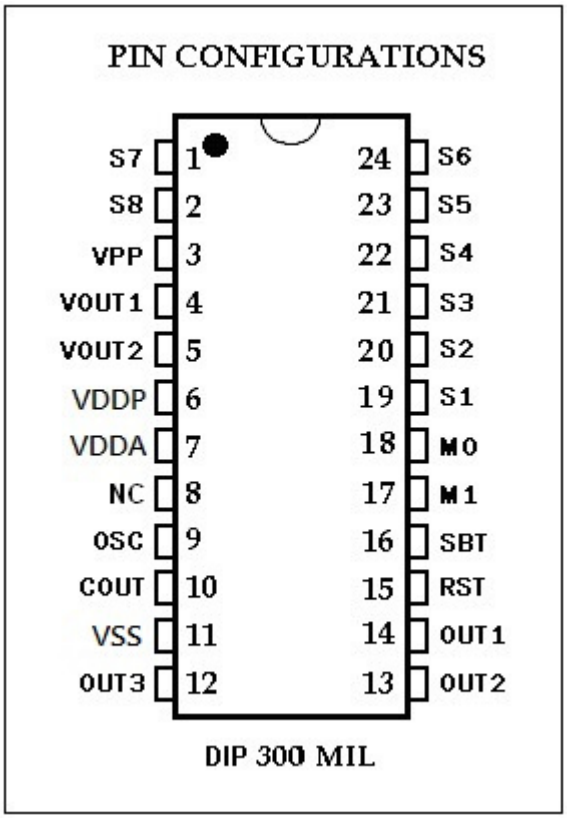
FEATURES

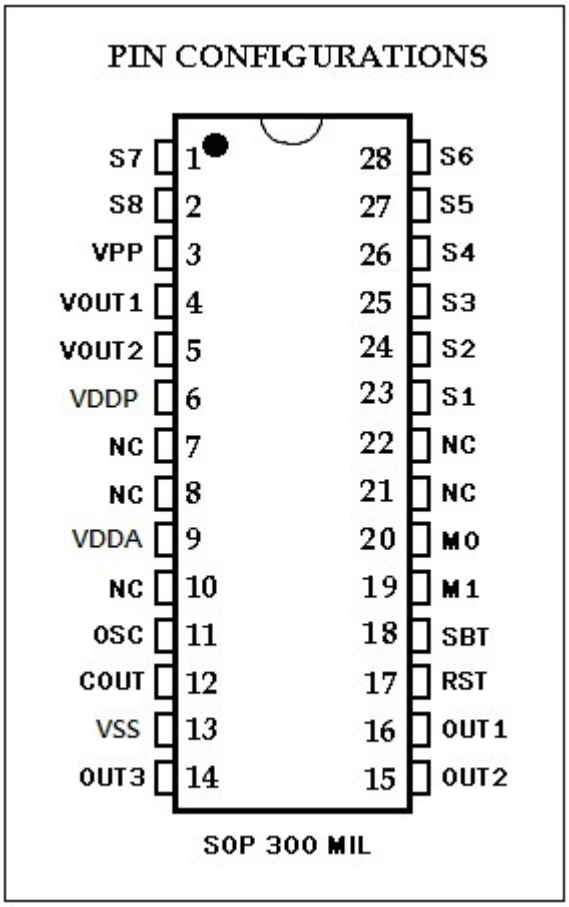
- Standard CMOS process.
- Embedded 16M/8M/4M/2M EPROM.
- 682/341/170/85 sec Voice Length at 6KHz sampling and 4-bit ADPCM compression.
- Maximum 1024 voice groups.
- Maximum 48KHz sample rate.
- Combination of voice blocks to extend playback duration.
- User selectable PCM16 or UALW or PCM8 or ADPCM data compression
- 7 triggering modes are available :
  - Key Mode - S1 ~ S8 to trigger up to 57 voice groups; SBT to trigger up to 1024 voice groups sequentially; Power on play function.
  - CPU Parallel Mode - S[8:1] services as 8-bits address to trigger up to 256 voice groups with SBT goes HIGH to strobe the address bits.
  - SPI Mode - 3 wire address control up to 1024 voice groups.
  - I2C Mode - 2 wire address control up to 1024 voice groups.
  - MP3 Mode - S1:Backward. S2: Forward. S3:Stop. S4:Reset. SBT: Play/Pause Trigger up to 1024 voice groups.
  - aP89 Mode 1 – Function setting compatible aP89341/aP89170/aP89085
  - aP89 Mode 2 – In aP89 CPU Serial Command mode, add extra Volume control or Crystal oscillator setting function.

  Note : aP89 Mode is function setting compatible with APLUS 1st Generation OTP IC (aP89341/aP89170/aP89085) usage.
- Voice Group Trigger Options: Edge / Level; Hold / Un-hold; Retrigger / Non-retrigger.
- Optional 16ms or 65us (@ 8KHz sampling rate) selectable debounce time
- RST pin set HIGH to stop the playback at once
- LVR (Low voltage reset)
- 7 user programmable outputs for STOP pulse, BUSY signal and flashing LED.
- Three kind oscillator: Internal-Rosc、External-Rosc、Crystal.
- 2V – 5V single power supply and < 5uA low stand-by current.
- 16/8/4 level volume control setting available.
- Audio out 16 bit.
- PWM Vout1 and Vout2 drive speaker directly
- D/A COUT pin drives speaker through an external BJT
- Development System support voice compilation.

DESCRIPTION

aP89682K/341K/170K/085K series high performance Voice OTP is fabricated with Standard CMOS process with embedded 16M/8M/4M/2M bits EPROM. It can store up to 682/341/170/85 sec voice message with 4-bit ADPCM compression at 6KHz sampling rate. 16-bit PCM and 8-bit PCM is also available for user selecting. User selectable triggering and output signal options provide maximum flexibility to various applications. Built-in resistor controlled oscillator, 16-bit current mode DAC output and 14-bit current mode PWM direct speaker driving output minimize the number of external components. PC controlled programmer and developing software are available.





PIN NAMES

PIN (24-pin)	Playback Mode	OTP Program Mode	Description
1	S7		Trigger pin (I/O pin with internal pull-down)
2	S8		Trigger pin (I/O pin with internal pull-down)
3	VPP	VPP	Supply ground
4	VOUT1		PWM output to drive speaker directly
5	VOUT2		PWM output to drive speaker directly
6	VDDP	VDDP	Supply voltage
7	VDDA	VDDA	Analog supply voltage
8	NC		
9	OSC		Oscillator input
10	COUT		DAC current output
11	VSS	VSS	Supply ground
12	OUT3		Programmable output (I/O pin)
13	OUT2		Programmable output (I/O pin)
14	OUT1		Programmable output (I/O pin)
15	RST	RST	Reset pin (input pin with internal pull-down)
16	SBT		Trigger pin (I/O pin with internal pull-down)
17	M1		Mode select pin 1 (input with internal pull-down)
18	M0		Mode select pin 0 (input with internal pull-down)
19 ~ 24	S1~S6	S2、S3	Trigger input (I/O pin with internal pull-down)

PIN DESCRIPTIONS

S1 ~ S8

Input Trigger Pins:
- In Key Mode, S1 to S8 is used to trigger 57 Voice groups.
- In CPU Parallel Mode, S1 to S8 serve as Voice Group address inputs for 1024 Voice Groups with S1 as LSB and S8 as MSB.
- In SPI Mode, S1 is Chip Select (SC) pin to initiate the command input. S2 is the Serial Clock (SCK) pin which clocks the input command and data bits into the chip. S3 is the Data In (DI) pin in which command and data bits are shifted input into the chip.
- In I2C Mode,S2 is the Serial Clock (SCK) pin which clocks the input command and data bits into the chip. S3 is the Data In (DI) pin in which command and data bits are shifted input into the chip.
- In MP3 Mode, S1:Backward. S2 :Forward. S3:Stop. S4: Reset.
- In aP89 Mode 1 and Mode 2 : compatible with APLUS 1st Generation OTP IC (aP89341/aP89170/aP89085) usage.

SBT

Input Trigger Pin:
- In Key Mode, this pin is trigger pin to play Voice Groups one time or looping sequentially up to 1024 Voice Groups.
- In CPU Parallel Mode, this pin is used as address strobe to latch the Voice Group address input at S1 to S8 and starts the voice playback.
- In MP3 Mode, this pin is Play / Pause.

VDDP and VDDA

Power Supply Pins: These two pins must be connected together to the positive power supply.

VSS

Power Ground Pins: These two pins must be connected to the power ground.

M0 and M1

In Key Mode、CPU Parallel Mode、MP3 Mode、SPI Mode、I2C Mode and aP89 Mode 2, M0 and M1 can be used for Crystal oscillator or volume control.

In aP89 Mode 1 Operating Mode Setting Pins:
- M1=0, M0=0 set the chip into Key Trigger Mode
- M1=0, M0=1 set the chip into CPU Parallel Command Mode
- M1=1, M0=0 set the chip into CPU Serial Command Mode
- M1=1, M0=1 set the chip into OTP Programming Mode

VOUT1 and VOUT2

14-bit PWM output pins which can drive speaker and buzzer directly for voice playback.

OSC

During voice playback, an external resistor is connected between this pin and the VDD pin to set the sampling frequency. Or keep OSC floating if choosing INT-Rosc.

VPP

During voice playback, this pin must be connected together with VSS. In OTP Programming Mode, this pin is connected to a separate 8.5V power supply voltage for OTP programming.

OUT1, OUT2 and OUT3

OUT1,OUT2 and OUT3 can select output function as below :

0: DacEn : When voice is playing in DAC, output high level signal.
1: fsm_busy : When voice is playing, output high level signal.
2: fsm_led_out : When voice is playing, output high level signal
3: 3Hz : When voice is playing, output 3Hz pulse.
4: in_pause : When voice has been paused, output high level signal
5: fsm_stop_out : When voice plays finished, output stop pulse
6: LoadBit : After load voice data to buffer success, output logic high signal.
7: ~DacEn : Inverted output of DacEn
8: ~fsm_busy : Inverted output of fsm_busy
9: ~fsm_led_out : Inverted output of fsm_led_out
10: ~3Hz : Inverted output of 3Hz.
11: ~in_pause : Inverted output of in_pause .
12: ~fsm_stop_out : Inverted output of fsm_stop_out .
13: ~LoadBit : Inverted output of LoadBit.

COUT

16-bit current mode DAC output for voice playback

RST

Chip reset in playback mode.

VOICE SECTION COMBINATIONS

Voice files created by the PC base developing system are stored in the built-in EPROM of the aP89682K/341K/170K/085K chip as a number of fixed length Voice Blocks. Voice Blocks are then selected and grouped into Voice Groups for playback. Up to 1024 Voice Groups are allowed. A Voice Blocks Table is used to store the information of combinations of Voice Blocks and then group them together to form Voice Group.

Chip	aP89682K	aP89341K	aP89170K	aP89085K
Memory size	16M bits	8M bits	4M bits	2M bits
Max no. of Voice Block	2016	2016	2016	2016
Max. no. of Voice Group	1024	1024	1024	1024
Voice Length (@ 6KHz 4-bit ADPCM)	682 sec	341 sec	170 sec	85 sec

Example of Voice Block Combination

Assume here we have three voice files, they are "How are You?", Sound Effect and Music. Each of the voice file is divided into a number of fixed length Voice Block and stored into the memory.

Voice File 1 - "How are You?" is stored in Voice Block B0 to B12.
Voice File 2 - Sound Effect is stored in Voice Block B13 to B15.
Voice File 3 - Music is Voice Block B16 to B40.

Voice Blocks are grouped together using Voice Table to form Voice Group for playback:

Group no.	Voice Group contents	Voice Table Entries
Group 1	"How are You?"	B0 … B12
Group 2	Sound Effect + "How are You?"	B13 … B15 + B0 … B12
Group 3	"How are You?" + Music	B0 … B12 + B16 … B40
Group 4	Music	B16 … B40

Voice Data Compression

Voice File data is stored in the on-chip EPROM as either 4-bit ADPCM or 8-bit PCM/ UALW format or 16-bit PCM format. Voice data are stored as 16-bit PCM forma is without compression. The voice playback quality is best. Voice data stored as 4-bit ADPCM or 8-bit PCM/ UALW provide 4:2 data compression to save memory space. But voice playback quality with be lower than 16-bit PCM format.

Group Options

User selectable options that affect each individual group are called Group Options. They are:

- Edge or Level trigger
- Unholdable or Holdable trigger
- Re-triggerable or non-retriggerable
- Stop pulse disable or enable

Fig. 1 to Fig. 6 show the voice playback with different combination of triggering mode and the relationship between outputs and voice playback.

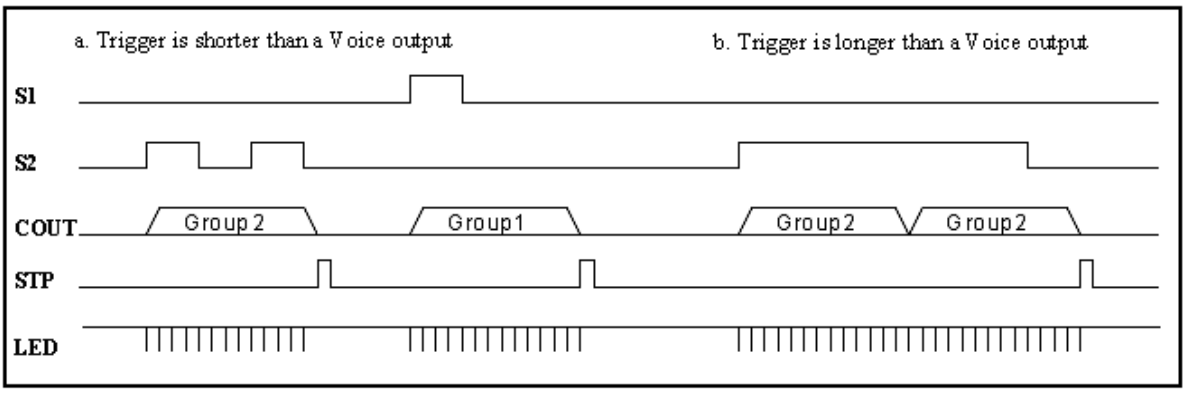


Fig. 1 Level, Unholdable, Non-retriggerable

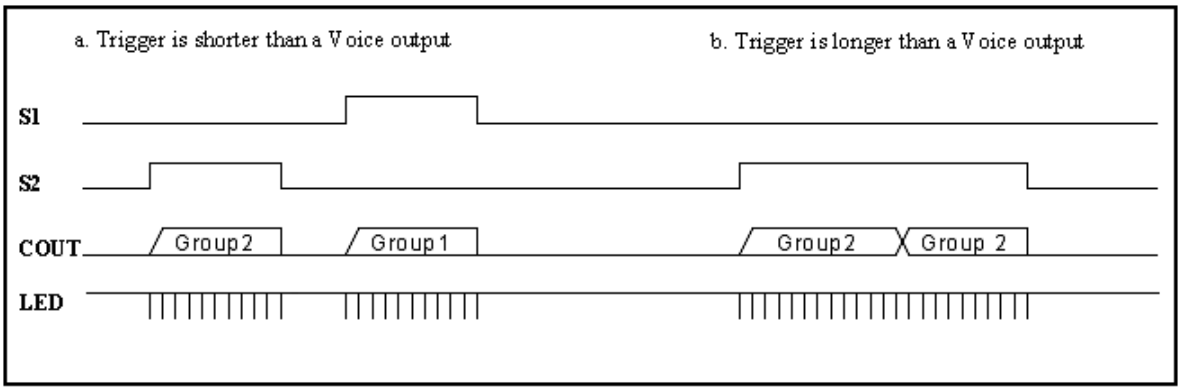


Fig. 2 Level Holdable

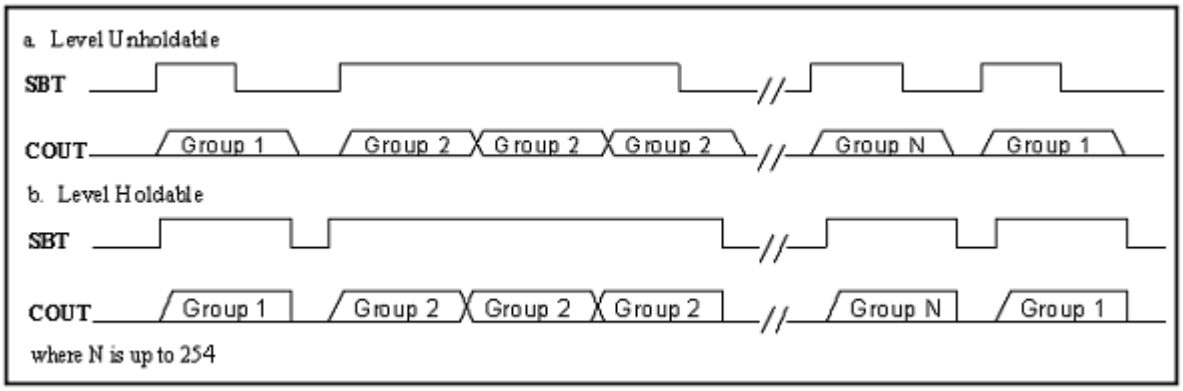


Fig. 3 SBT sequential trigger with Level Holdable and Unholdable

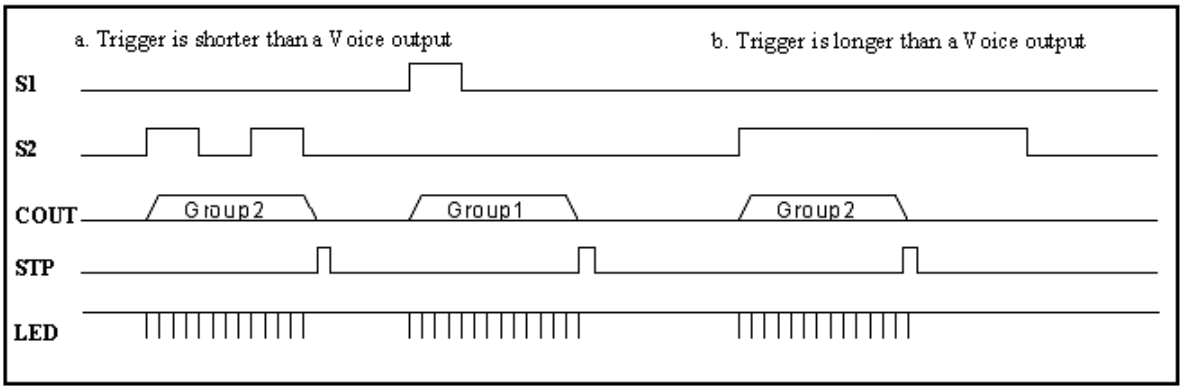


Fig. 4 Edge, Unholdable, Non-retrigger

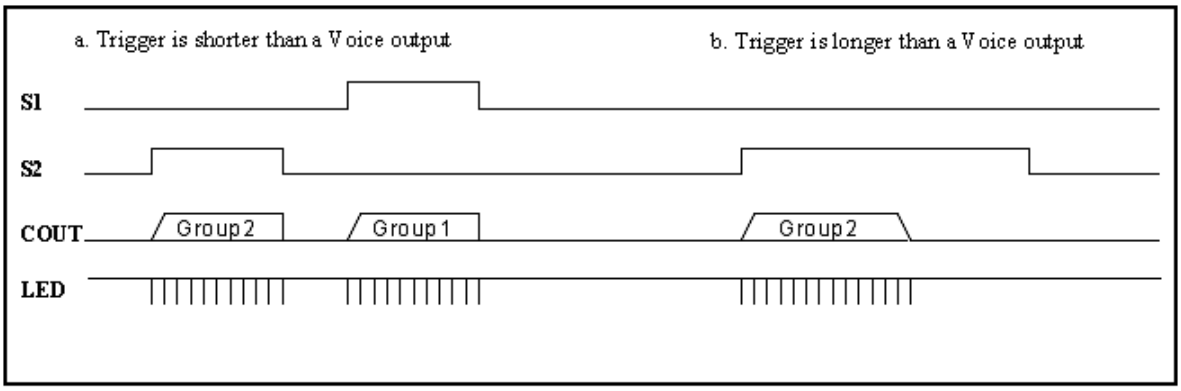


Fig. 5 Edge, Holdable

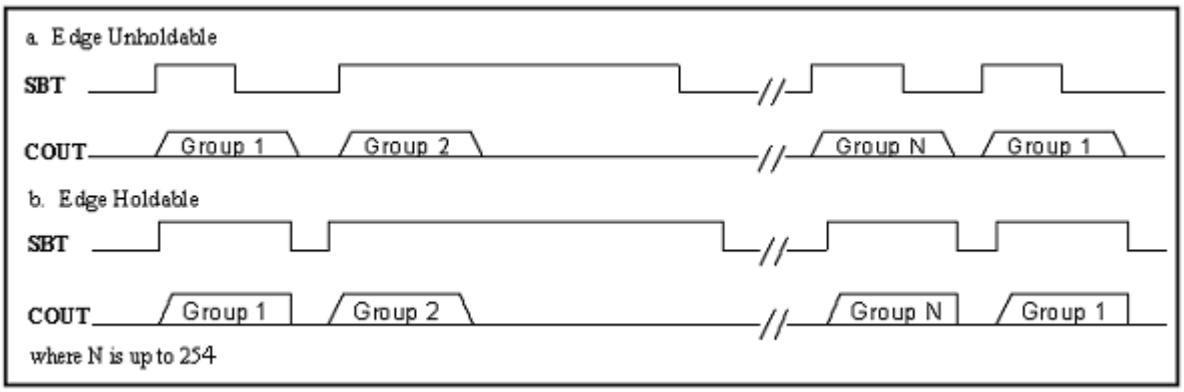


Fig. 6 SBT sequential trigger with Edge Holdable and Unholdable

TRIGGER MODES

There are seven trigger modes available for aP89682K/341K/170K/085K series.

- Key Mode
- CPU Parallel Mode
- aP89 Mode 1
- aP89 Mode 2
- SPI Mode
- I2C Mode
- MP3 Mode

Key Mode

With this trigger mode, the beginning 57 Voice Groups are triggered by setting S1 to S8 to HIGH or LOW in different combinations. Each Voice Group can have its only independent trigger options (See Fig. 1,2,4 and 5 for trigger options definition).

A maximum of 1024 Voice Groups are available. And can be triggered one by one sequentially with the SBT key (See Fig. 3 and 6).

The setting of S1 to S8 for triggering the 1st to the 57nd Voice Groups are as follow:

Voice Group	S1	S2	S3	S4	S5	S6	S7	S8
SW1	HIGH	NC	NC	NC	NC	NC	NC	NC
SW2	NC	HIGH	NC	NC	NC	NC	NC	NC
SW3	NC	NC	HIGH	NC	NC	NC	NC	NC
SW4	NC	NC	NC	HIGH	NC	NC	NC	NC
SW5	NC	NC	NC	NC	HIGH	NC	NC	NC
SW6	NC	NC	NC	NC	NC	HIGH	NC	NC
SW7	NC	NC	NC	NC	NC	NC	HIGH	NC
SW8	NC	NC	NC	NC	NC	NC	NC	HIGH
SW9	HIGH	HIGH	NC	NC	NC	NC	NC	NC
SW10	NC	HIGH	HIGH	NC	NC	NC	NC	NC
SW11	NC	NC	HIGH	HIGH	NC	NC	NC	NC
SW12	NC	NC	NC	HIGH	HIGH	NC	NC	NC
SW13	NC	NC	NC	NC	HIGH	HIGH	NC	NC
SW14	NC	NC	NC	NC	NC	HIGH	HIGH	NC
SW15	NC	NC	NC	NC	NC	NC	HIGH	HIGH
SW16	HIGH	NC	NC	NC	NC	NC	NC	HIGH
SW17	HIGH	HIGH	HIGH	NC	NC	NC	NC	NC
SW18	NC	HIGH	HIGH	HIGH	NC	NC	NC	NC
SW19	NC	NC	HIGH	HIGH	HIGH	NC	NC	NC
SW20	NC	NC	NC	HIGH	HIGH	HIGH	NC	NC
SW21	NC	NC	NC	NC	HIGH	HIGH	HIGH	NC
SW22	NC	NC	NC	NC	NC	HIGH	HIGH	HIGH
SW23	HIGH	NC	NC	NC	NC	NC	HIGH	HIGH
SW24	HIGH	HIGH	NC	NC	NC	NC	NC	HIGH
SW25	HIGH	HIGH	HIGH	HIGH	NC	NC	NC	NC
SW26	NC	HIGH	HIGH	HIGH	HIGH	NC	NC	NC
SW27	NC	NC	HIGH	HIGH	HIGH	HIGH	NC	NC
SW28	NC	NC	NC	HIGH	HIGH	HIGH	HIGH	NC
SW29	NC	NC	NC	NC	HIGH	HIGH	HIGH	HIGH
SW30	HIGH	NC	NC	NC	NC	HIGH	HIGH	HIGH
SW31	HIGH	HIGH	NC	NC	NC	NC	HIGH	HIGH
SW32	HIGH	HIGH	HIGH	NC	NC	NC	NC	HIGH
SW33	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC	NC
SW34	NC	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC
SW35	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH	NC
SW36	NC	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH
SW37	HIGH	NC	NC	NC	HIGH	HIGH	HIGH	HIGH
SW38	HIGH	HIGH	NC	NC	NC	HIGH	HIGH	HIGH
SW39	HIGH	HIGH	HIGH	NC	NC	NC	HIGH	HIGH
SW40	HIGH	HIGH	HIGH	HIGH	NC	NC	NC	HIGH
SW41	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC
SW42	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC
SW43	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
SW44	HIGH	NC	NC	HIGH	HIGH	HIGH	HIGH	HIGH
SW45	HIGH	HIGH	NC	NC	HIGH	HIGH	HIGH	HIGH
SW46	HIGH	HIGH	HIGH	NC	NC	HIGH	HIGH	HIGH
SW47	HIGH	HIGH	HIGH	HIGH	NC	NC	HIGH	HIGH
SW48	HIGH	HIGH	HIGH	HIGH	HIGH	NC	NC	HIGH
SW49	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC
SW50	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
SW51	HIGH	NC	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
SW52	HIGH	HIGH	NC	HIGH	HIGH	HIGH	HIGH	HIGH

SW53	HIGH	HIGH	HIGH	NC	HIGH	HIGH	HIGH	HIGH
SW54	HIGH	HIGH	HIGH	HIGH	NC	HIGH	HIGH	HIGH
SW55	HIGH	HIGH	HIGH	HIGH	HIGH	NC	HIGH	HIGH
SW56	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	NC	HIGH
SW57	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH

★★★ Note: NC represents open or no connection

CPU Parallel Mode

In this mode, S8 to S1 serve as 8-bit addresses input for 256 Voice Groups with S8 represents the MSB and S1 represents LSB. After Group address is set and ready, setting the SBT input pin to HIGH will trigger the corresponding Voice Group to playback.

Trigger options defined in Fig. 1,2, 4 and 5 are valid for this mode.

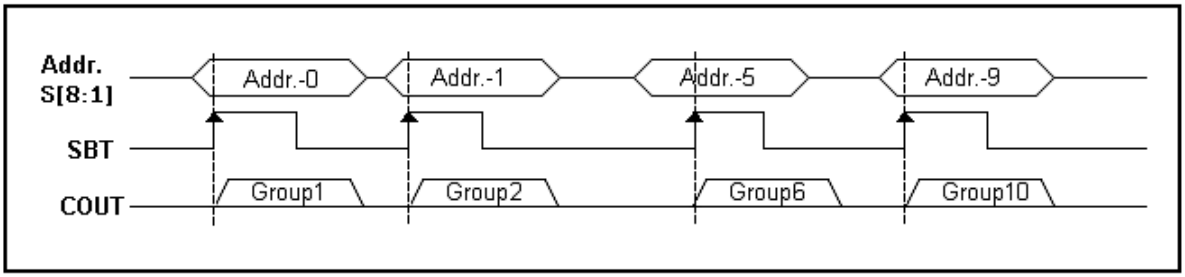


Fig. 7 CPU Parallel Trigger Mode

Note that SBT pin cannot be used as Single Button Sequential trigger in this mode. In stead, it acts as a Strobe input to clock-in the Voice Group address set at S8 to S1 into the chip.

Voice Groups are represented in Binary address format. For example:

S[8:1] = 0000 0000 (00hex) for Voice Group #1
S[8:1] = 0000 0001 (01hex) for Voice Group #2
• • •
S[8:1] = 0000 1000 (08 hex) for Voice Group #9
• • •
S[8:1] = 1000 1000 (88 hex) for Voice Group #137
• • •
S[8:1] = 1111 1111 (FF hex) for Voice Group #256

aP89 Mode 1

This trigger mode is function setting compatible with APLUS 1st Generation OTP IC (aP89341/aP89170/aP89085) usage.

aP89 Mode 2

Extra Volume control command under aP89 CPU Serial Command mode.

Command	D7	D6	D5	D4	D3	D2	D1	D0	Description
VOL-- (B1h)	1	0	1	1	0	0	0	1	Set volume level decrease
	0	0	0	0	0	0	0	0	Second byte is (00h)
VOL++ (B4h)	1	0	1	1	0	1	0	0	Set volume level increase.
	0	0	0	0	0	0	0	0	Second byte is (00h)
VOL SET (B2h)	1	0	1	1	0	0	1	0	Set volume level of value
	0	0	0	0	V3	V2	V1	V0	Second byte set volume level; max: 0, min: 15

*** Set 8 volume level by V2,V1 and V0 bit.
*** Set 4 volume level by V1 and V0 bit.

SPI Mode

This trigger mode is specially designed for simple CPU interface. The aP89682K/341K/170K/085K is controlled by command sent to it from the host CPU. S1 to S3 are used to input command word into the chip while OUT1 to OUT3 as output from the chip to the host CPU for feedback response.

- S1 acts as CS (Chip Select) to initiate the command word input
- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.
- OUT1 acts as BUSY to indicate the chip is in busy state.
- OUT2 acts as POUT to output user selected information.
- OUT3 acts as Load signal to indicate the Voice Group address buffer is full.
- M0 acts as volume level increase.
- M1 acts as volume level decrease.

Command input into the chip 16-bit data. The first 8-bit data is command bits while the second 8-bit data (if any) is the Voice Group address data or set volume of value. Table 1 summarize the available commands and their functions.

Table1

CMD	b-15	b-14	b-13	b-12	b-11	b-10	b- 9	b-8	b-7	b- 6	b- 5	b-4	b-3	b-2	b-1	b-0
STATUS	1	0	0	0	1	0	X	X	X	X	1	1	1	1	1	1
LOAD	1	0	0	1	0	1	Address									
PLAY	1	0	0	1	1	0	Address									
PU1	1	0	1	0	0	1	Don't care									
PU2	1	0	1	0	1	0	Don't care									
PD1	1	0	1	1	0	1	Don't care									
PD2	1	0	1	1	1	0	Don't care									
VOL	0	1	0	0	0	1	X	X	Mute		X	X	Vol_Lv			
VOL--	0	1	0	0	1	0	Don't care									
VOL++	0	1	0	1	0	1	Don't care									
PAUSE	0	1	1	0	0	1	Don't care									
RESUME	0	1	1	0	1	0	Don't care									
REWIND	0	1	1	1	0	1	Don't care									

b : bit

X : Don't care (maybe 1 or 0)

Load : The Load signal will become logic Low once the Voice Group is played and the address buffer is released and ready for next Play action. (Address of value is section number - 1)

Play : The Play command pre-load the next Voice Group Address into the address buffer and play voice. (Address of value is section number - 1)

PU1 : Power up the chip with NO ramp-up (suitable for VOUT direct drive)

PU2 : Power up the chip WITH ramp-up (suitable for COUT transistor drive)

PD1 : Power down the chip with NO ramp-down (suitable for VOUT direct drive)

PD2 : Power down the chip WITH ramp-down (suitable for COUT transistor drive)

VOL : Set voice of volume (volume level : 0 ~ 15 ; max = 0 , min = 15) and Mute (Mute:10B: set mute , Mute:01B: clear mute ,).

VOL-- : Set volume level decrease.

VOL++ : Set volume level increase.

Pause : Set voice pause.

Resume : Set voice resume.

Rewind : The voice repeat.

1.Set OUT2 pin status (STATUS:88FFh)

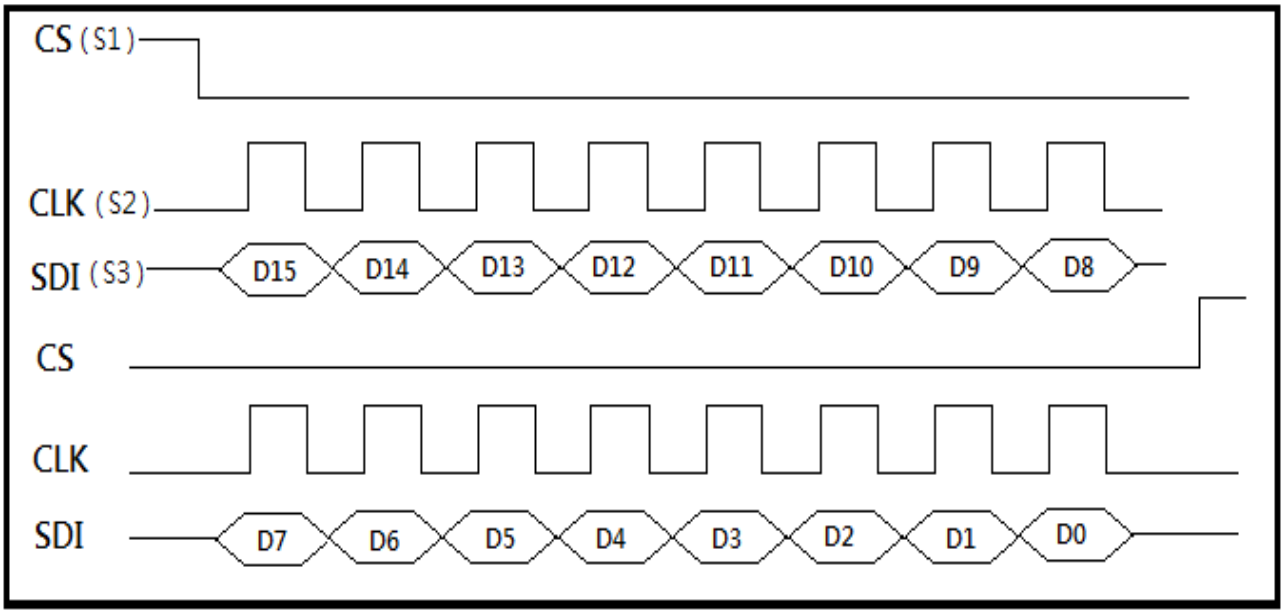


Fig. 8 SPI command timing

* The data bit only can be changed in CLK low level , but it has to be latched before rising edge of CLK.

2. Load Voice Group Address

a. Command timing reference Fig. 8 SPI command timing.
b. D9 to D0 total 10 bits to be the Group Address
c. The OUT3 output (LoadBit) will become logic high once the Group Address is successfully loaded.
d. The Load signal will become logic LOW once the Voice Group is played and the address buffer is released and ready for next Play action.

3. Play Voice Group Address

a. Command timing reference Fig. 8 SPI command timing.
b. D9 to D0 total10 bits as Group Address
c. Playing assign group address.
d. Using the PLAY make sure there is no gap between each Voice Group

4. Power up with RAMP-UP (PU2:A4xxh) or without RAMP-UP (PU1:A8xxh)

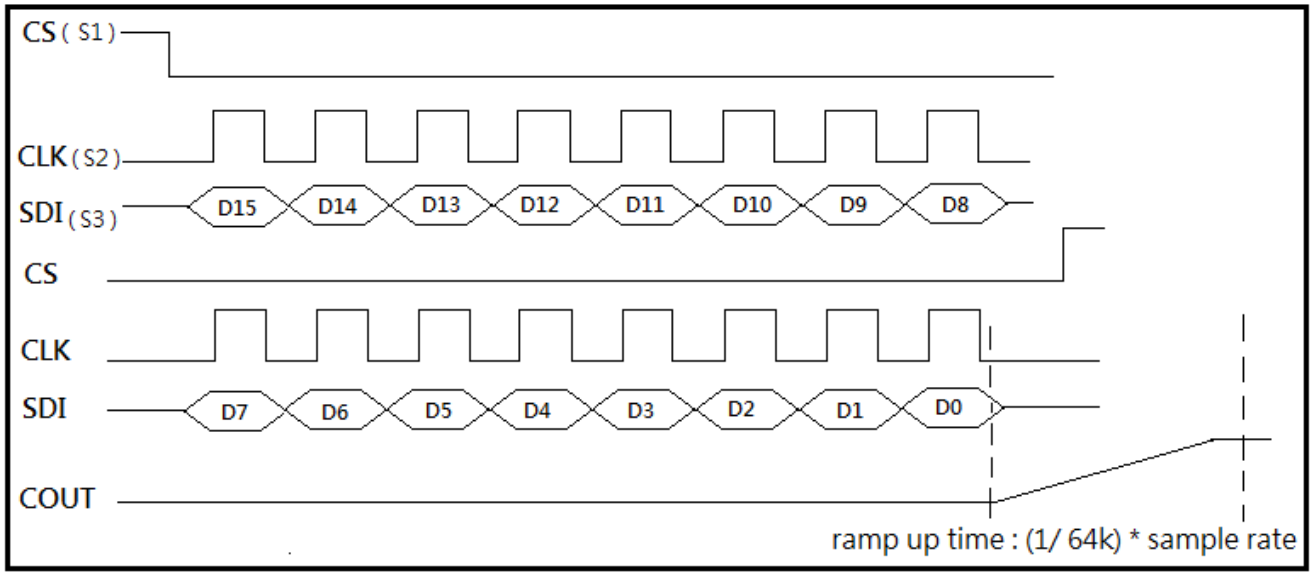


Fig. 9 Power-up command timing

PU1 : will power-up the chip and set the COUT to 80H immediately and stay there.
PU2 : will Ramp-up chip and ramp-up COUT from 00H to 80H and stay there.

a. Voice will be playback immediately after PU1 / PU2 completes if the section buffer is filled with the Play command before power-up

b. OUT1 (BUSY) will output logic HIGH during Ramp-up operation.
c. PDN2 (Power-down with ramp-down) will be executed correctly only if PU2 is executed before.

5. Power-down with RAMP-DOWN (PD2:B8xxh) or without RAMP-DOWN (PD1:B4xxh)

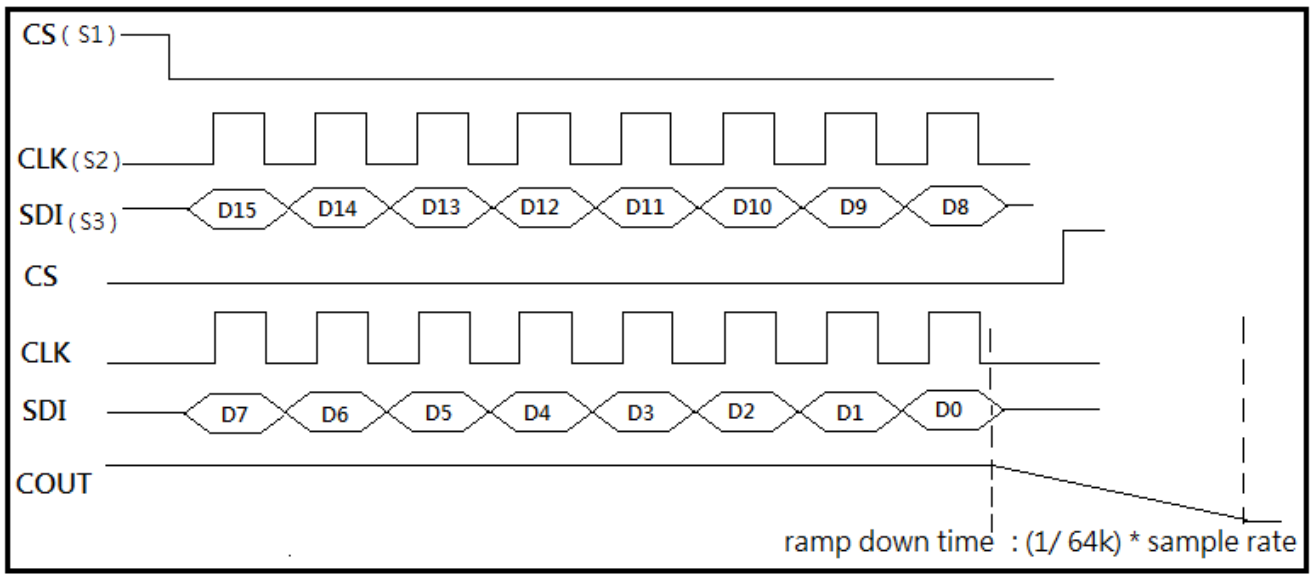


Fig. 10 Power-down commands timing

a. PDN1 will power-down the chip and set the COUT data to 00H immediately.
b. PDN2 will power-down the chip by Ramp-down the COUT from its current value to 00H.
c. The OUT1 pin (BUSY) will output logic HIGH during Ramp-down operation.
d. PDN2 (Power-down with ramp-down) will be executed correctly only if PU2 is executed before.

6. Volume Set
a. Command timing reference Fig. 8 SPI command timing.
b. D3 to D0 total 4bits (0 ~ 15) set volume level (max : 0 , min : 15)
c. If D7 D6 (10b) set mute , D7 D6 (01b) clear mute.

7. Volume - - (VOL - - : 48xxh)
a. Command timing reference Fig. 8 SPI command timing.
b. Set volume level decrease.

8. Volume + + (VOL + + : 54xxh)
a. command timing reference Fig. 8 SPI command timing.
b. Set volume level increase.

9. Pause and Resume (PAUSE:64h; RESUME:68h)
a. Command timing reference Fig. 8 SPI command timing.
b. In Pause state, VOUT1 and VOUT2 will stay at logic LOW while the COUT will stay at the current D/A data level (i.e. COUT is kept outputting an DC current). When Resume, the COUT data will continue at the current D/A data level.
c. The Pause state will be released by PDN1, PDN2 and RESUME commands.

10. Rewind (REWIND : 78xxh)
a. Command timing reference Fig. 8 SPI command timing.
b. The voice repeat.

I2C Mode

This trigger mode is specially designed for simple CPU interface. The aP89682K/341K/170K/085K is controlled by command sent to it from the host CPU. S2 and S3 are used to input command word into the chip while OUT1 to OUT3 as output from the chip to the host CPU for feedback response.

- S2 acts as SCK (Serial Clock) to clock-in the command word at rising edge.
- S3 acts as DI (Data-In) to input the command bits.
- OUT1 acts as BUSY to indicate the chip is in busy state.
- OUT2 acts as POUT to output user selected information.
- OUT3 acts as Load signal to indicate the Voice Group address buffer is full.
- M0 acts as volume level increase.
- M1 acts as volume level decrease.

Command input into the chip 16-bit data. The first 8-bit data is command bits while the second 8-bit data (if any) is the Voice Group address data or set volume of value. Table 1 summarize the available commands and their functions.

1. Command reference Table 1
2. Command timing as below and reference Fig. 11 commands timing.

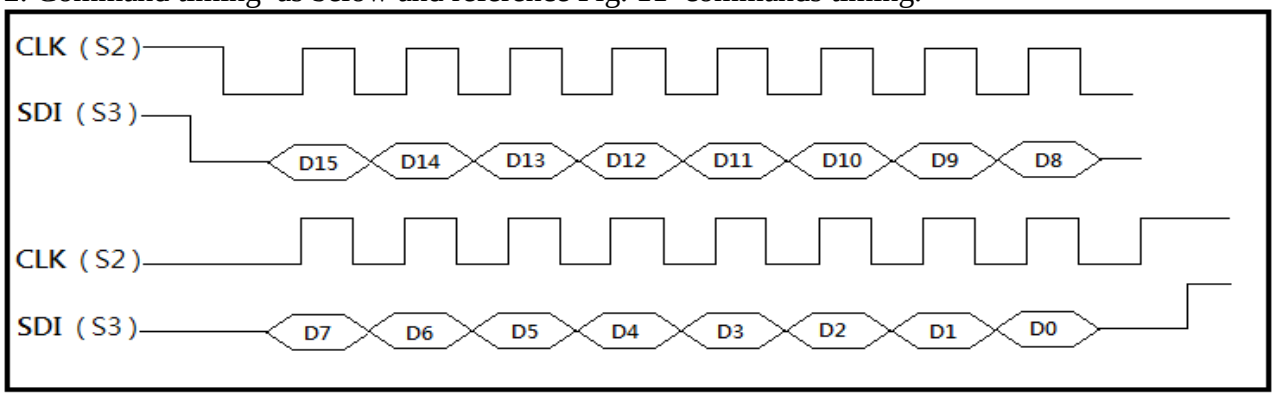


Fig. 11 commands timing

* The data bit only can be changed in CLK low level , but it has to be latched before rising edge of CLK

PU1 and PU2 command timing as below

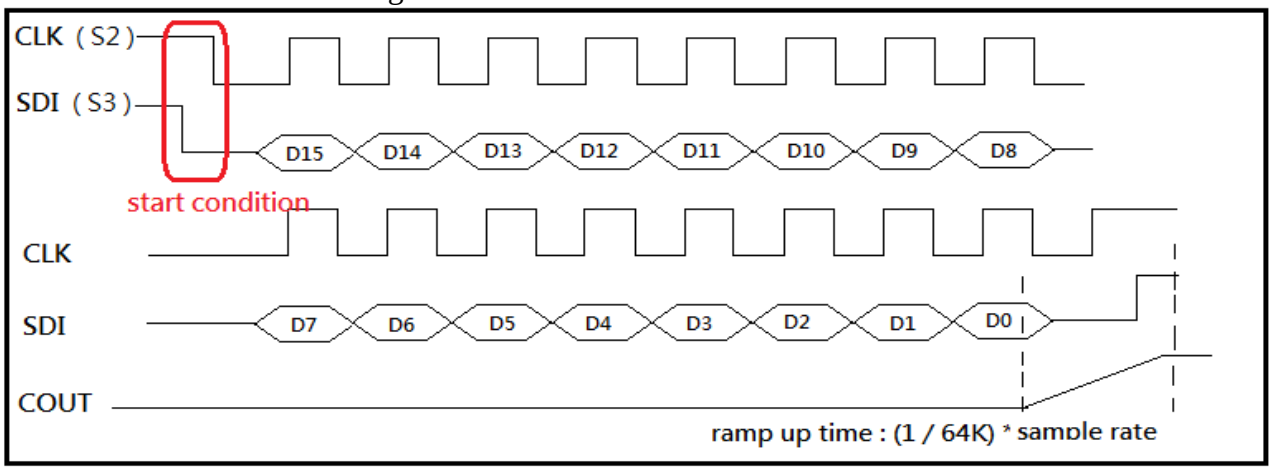


Fig. 12 Power-up commands timing

In Power up command : After start condition signal, add delay time more than 300us to wake up device.

PD1 and PD2 command timing as below

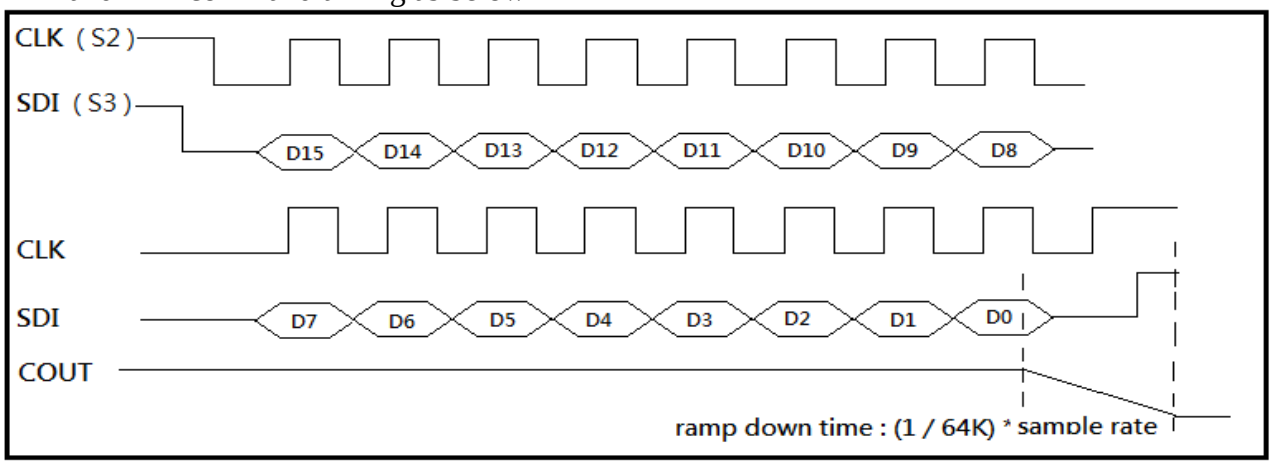


Fig. 13 Power-down commands timing

MP3 Mode
This trigger mode is specially designed for simple MP3 function.

User can start to Play or Pause the voice by SBT pin, and Backward or Forward play by S1 pin or S2 pin, up to 1024 Voice Sections.

- SBT acts as play / pause
- S1 acts as backward.
- S2 act as forward.
- S3 acts as stop.
- S4 act as reset
- M0 acts as volume level increase.
- M1 acts as volume level decrease.

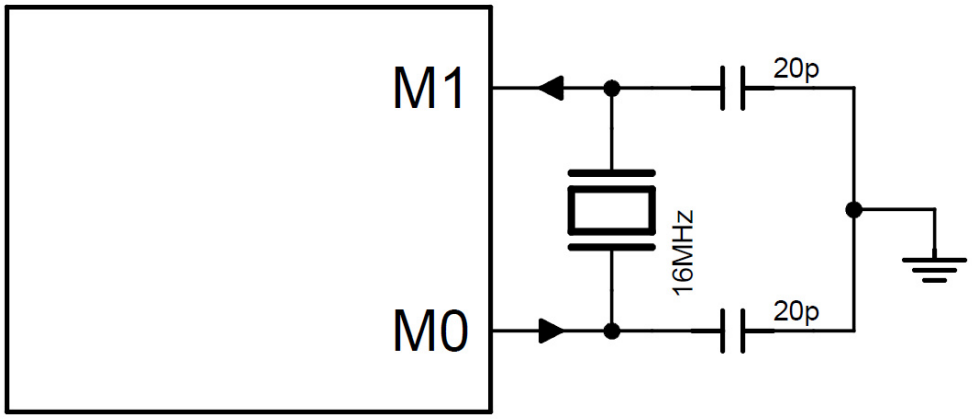
Oscillator Resistance
We have 3 modes can choose: Internal resistor、External resistor、Crystal resistance

Rosc Int – No need to add resistance

Rosc Ext – Use 68K ohm resistance in OSC pin

XT - Setting Crystal mode in M0 pin and M1 pin

1. Use 10pF ~ 30pF for capacitor.
2. The crystal use 16MHz.



BLOCK DIAGRAM

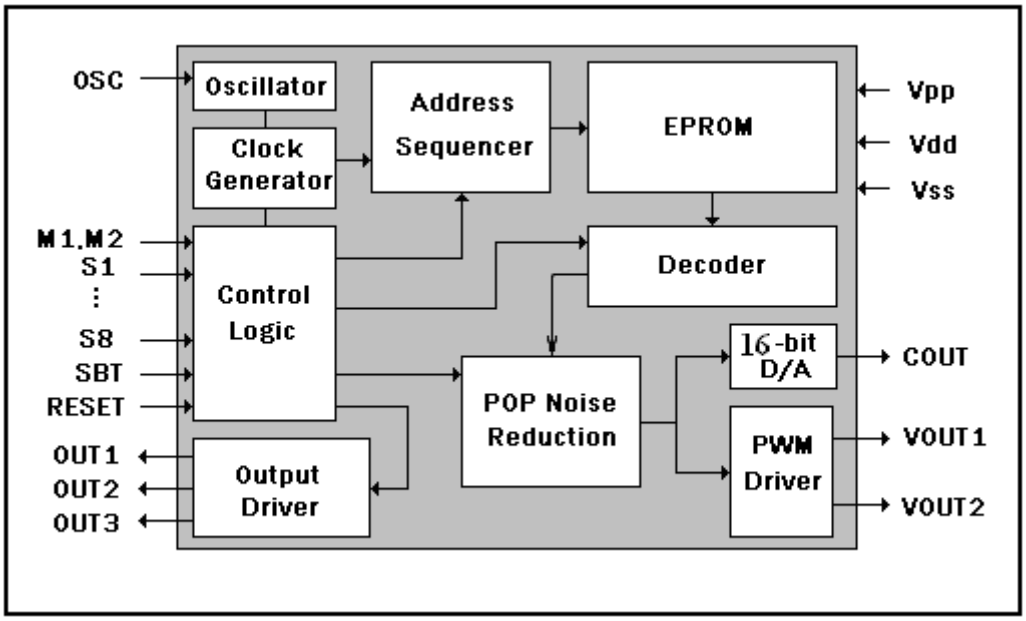


Fig. 14 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Unit
V_{DD} - V_{SS}	-0.5 ~ +5.0	V
V_{IN}	V_{SS} - 0.3<V_{IN}<V_{DD} + 0.3	V
V_{OUT}	V_{SS} <V_{OUT}<V_{DD}	V
T (Operating):	-10 ~ +85	℃
T (Junction)	-10 ~ +85	℃
T (Storage)	-10 ~ +85	℃

DC CHARACTERISTICS (T_A = 0 to 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.0		5.0	V	
ΔFc/Fc	Chip to chip frequency variation	-1.5		+1.5	%	

Symbol	Parameter	VDD	Min.	Typ.	Max.	Unit	Condition
I_{SB}	Standby current	3.3 4.5			1.0 1.0	uA	
I_{OP}	Operating current	3.3 4.5		11.0 18.3		mA	
I_{IH}	Input current	3.3 4.5		7.6 17.2		uA	V_{IL}=3.3V V_{IL}=4.5V
V_{IH}	Input high voltage	3.3 4.5		1.9 2.7		V	
V_{IL}	Input low voltage	3.3 4.5		1.0 1.7		V	
I_{OH}	Output high current	3.3 4.5		-16.6 -25.1		mA	V_{OH}=2.0V V_{OH}=3.5V
I_{OL}	Output low current	3.3 4.5		26.4 36.8		mA	V_{OL}=1.0V
I_{VOUT}	VOUT Current	3.3 4.5	-146.0 -218.0		153.0 227.0	mA	Load=8Ω
I_{COUT}	COUT Current	3.3 4.5	0.0 0.0		4.0 4.0	mA	V_{COUT}=1.0V
ΔF/F	Frequency Stability	3.3 4.5		1.5 1.5		%	Note1 Note2

Note1:

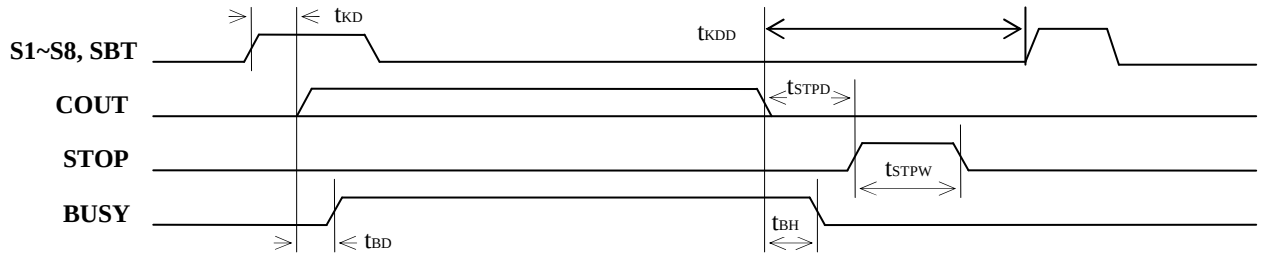
$$\frac{Fosc(3.3) - Fosc(2.7)}{Fosc(3.3)}$$

Note2:

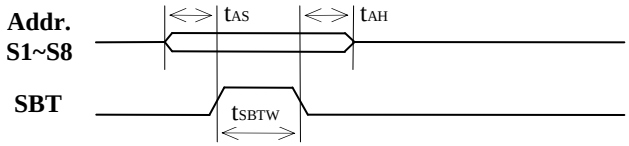
$$\frac{Fosc(5.0) - Fosc(4.5)}{Fosc(4.5)}$$

TIMING WAVEFORMS

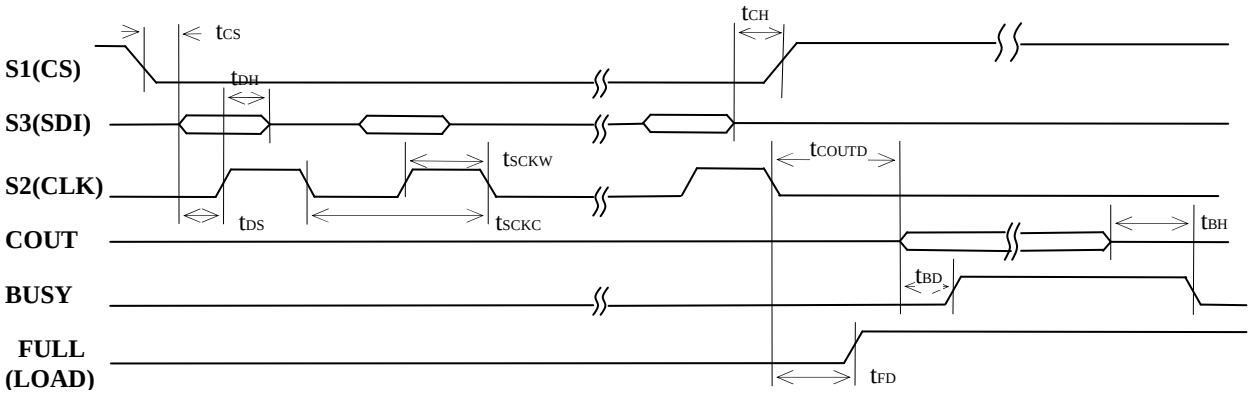
KEY Trigger Mode



CPU Parallel Mode



SPI Mode and aP89 Mode 2



I2C Mode

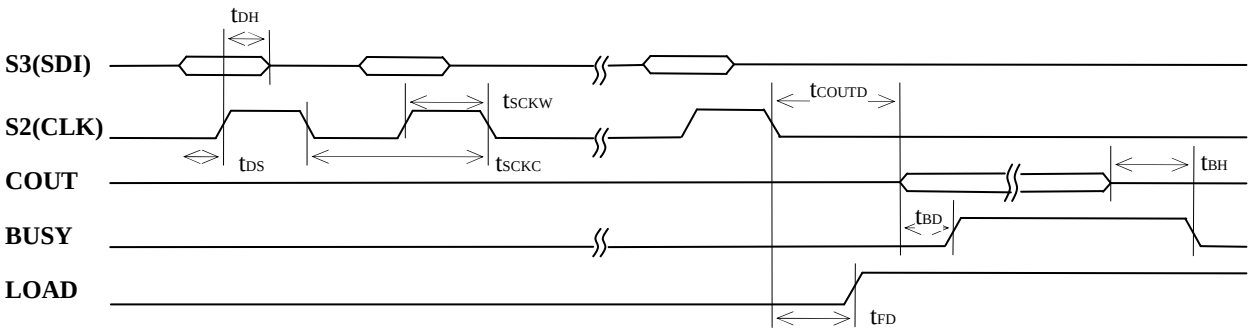


Fig. 15 Timing Waveform

AC CHARACTERISTICS (T_A = 0 to 70℃, V_{DD} = 3.3V, V_{SS} = 0V, 8KHz sampling)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
t_{KD}	Key trigger debounce time (long)	16	—	—	ms	1,2
t_{KD}	Key trigger debounce time (long) – retrigger option	24	—	—	ms	1,2
t_{KD}	Key trigger debounce time (short)	65	—	—	μs	1,2
t_{KD}	Key trigger debounce time (short) – retrigger option	200	—	—	μs	1,2
t_{KDD}	Key trigger delay after ramp down	256/Fs	—	—	s	4
t_{STPD}	STOP pulse output delay time	—	—	256	μs	
t_{STPW}	STOP pulse width	—	64	—	ms	1
t_{BD}	BUSY signal output delay time	—	—	100	ns	
t_{BH}	BUSY signal output hold time	—	100	—	ns	
t_{AS}	Address set-up time	100	—	—	ns	
t_{AH}	Address hold time	100	—	—	ns	
t_{SBTW}	SBT stroke pulse width (long)	16	—	—	ms	1,2
t_{SBTW}	SBT stroke pulse width (short)	65	—	—	μs	1,2
t_{CS}	Chip select set-up time	100	—	—	ns	
t_{CH}	Chip select hold time	100	—	—	ns	
t_{DS}	Data-in set-up time	100	—	—	ns	
t_{DH}	Data-in hold time	100	—	—	ns	
t_{SCKW}	Serial clock pulse width	1	—	—	μs	
t_{SCKC}	Serial clock cycle time	2	—	—	μs	
t_{COUTD}	COUT output delay time	—	—	256	μs	
t_{FD}	FULL signal output delay time	—	100	—	ns	
t_{LEDC}	LED flash frequency	—	3	—	Hz	3

Notes :

1. This parameter is inversely proportional to the sampling frequency.
2. The long or short debounce time is selectable as whole chip option during Voice Files Compiling.
3. This parameter is proportional to the sampling frequency.
4. Fs is sampling frequency in Hz

TYPICAL APPLICATIONS

Key Mode

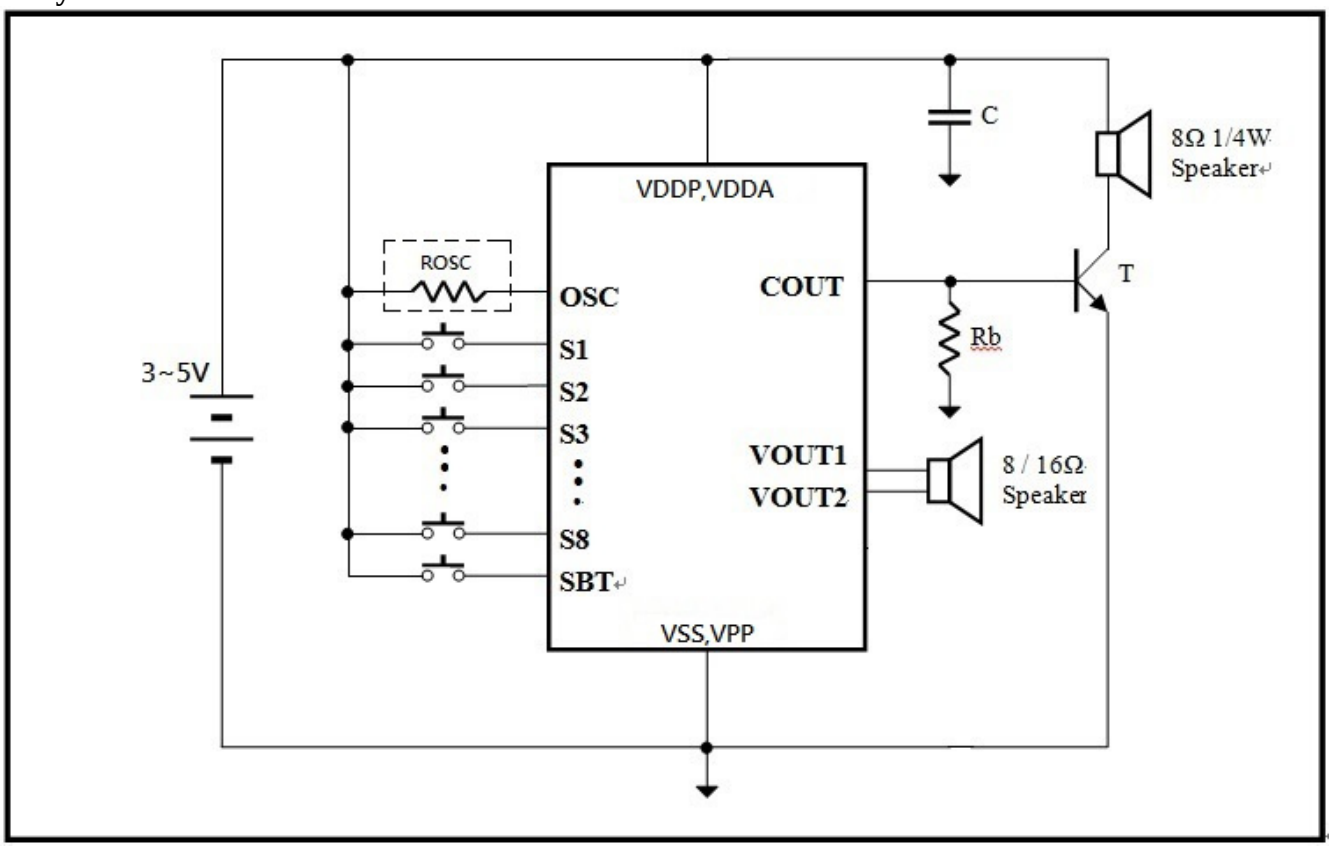


Fig. 16

CPU Parallel Mode

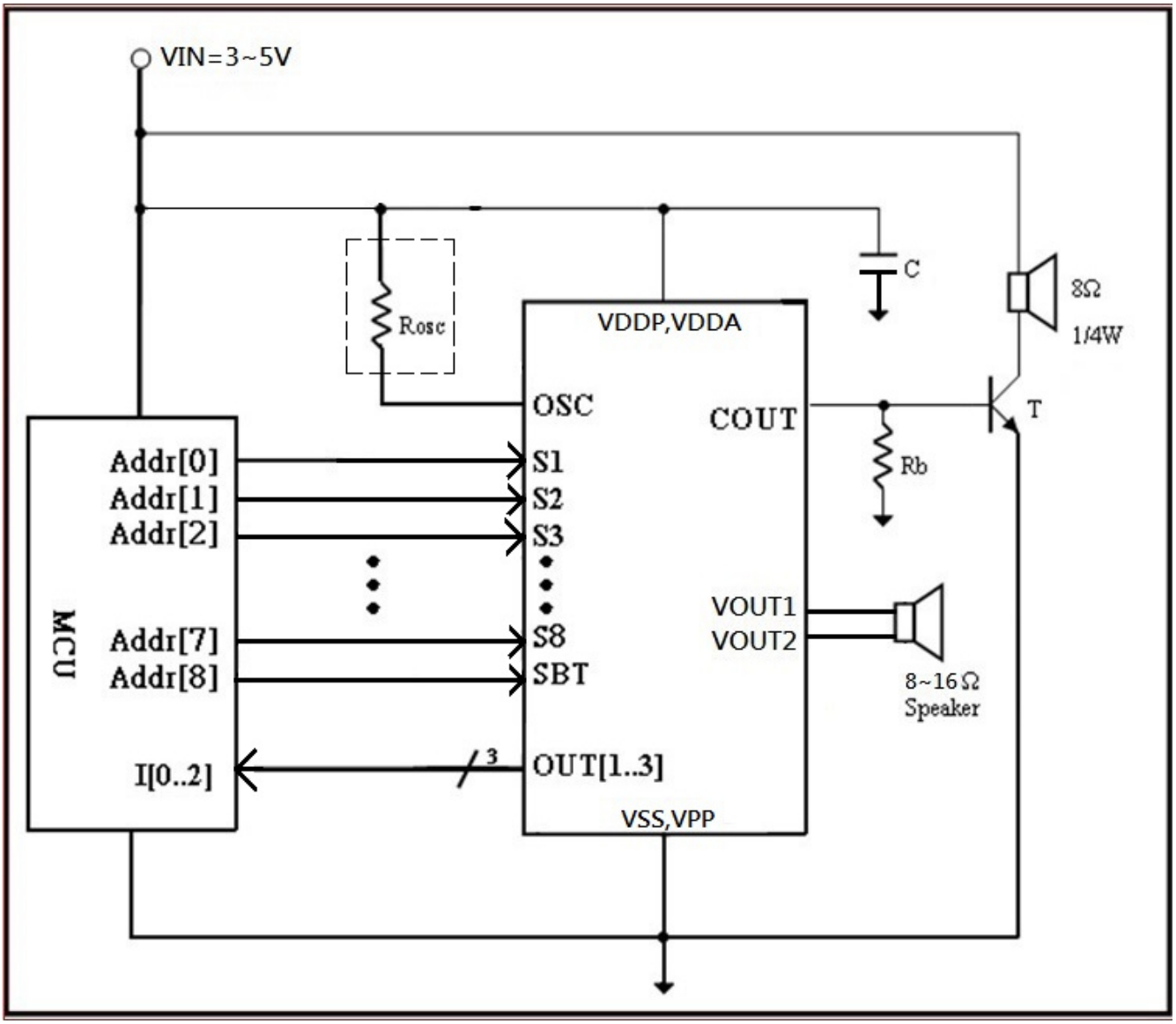


Fig. 17

Note:

1. C is capacitor from 0.1uF to 4.7uF depends on the kind of Vdd source and sound loudness.
2. Rb is base resistor from 120 Ohm to 390 Ohm depends on Vdd value and transistor gain.
3. T is an NPN transistor with beta larger than 150.
4. Reference value for the above components are Rb = 390 Ohm and T = 8050D.

aP89 Mode 2 and SPI Mode

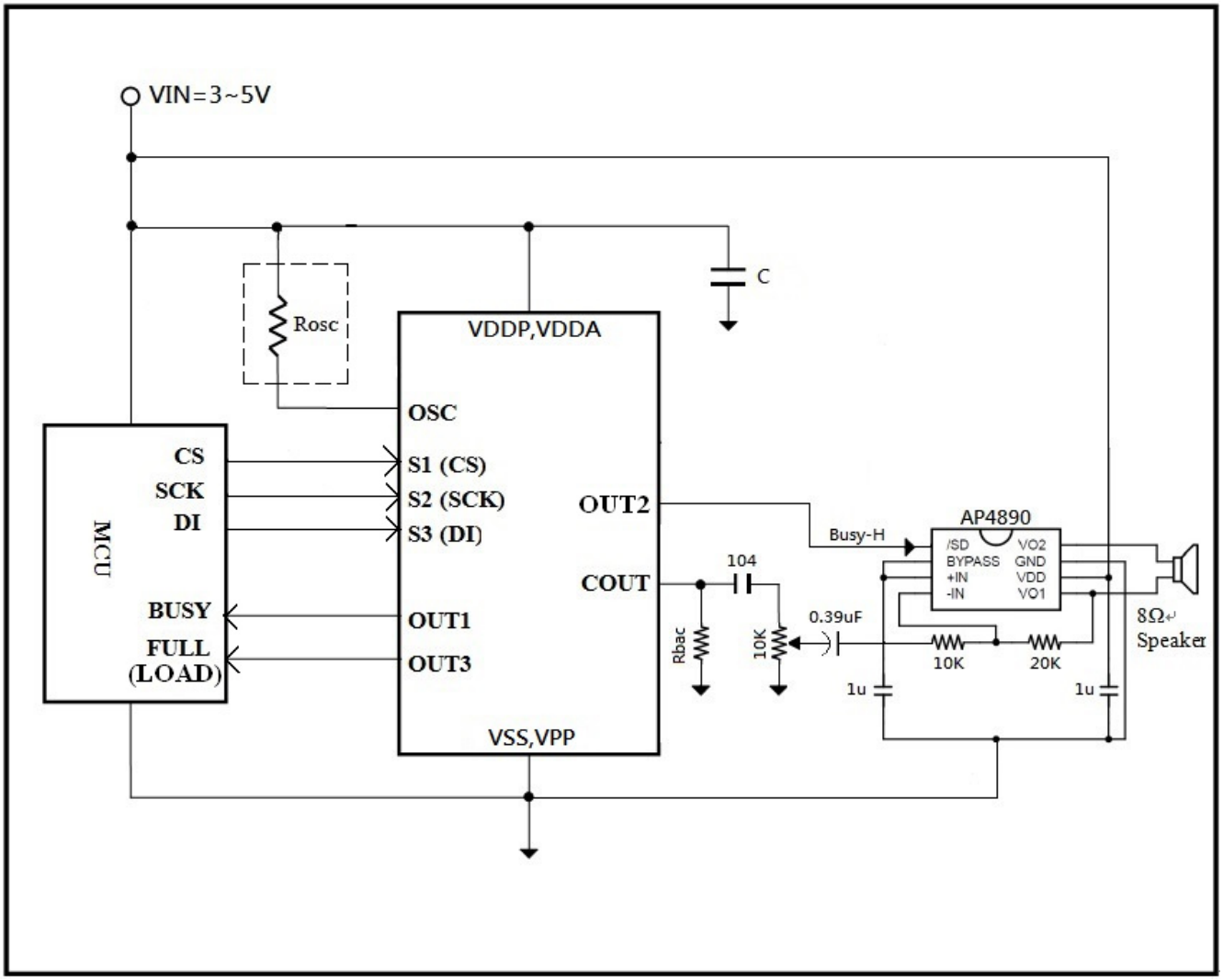


Fig. 18

I2C Mode

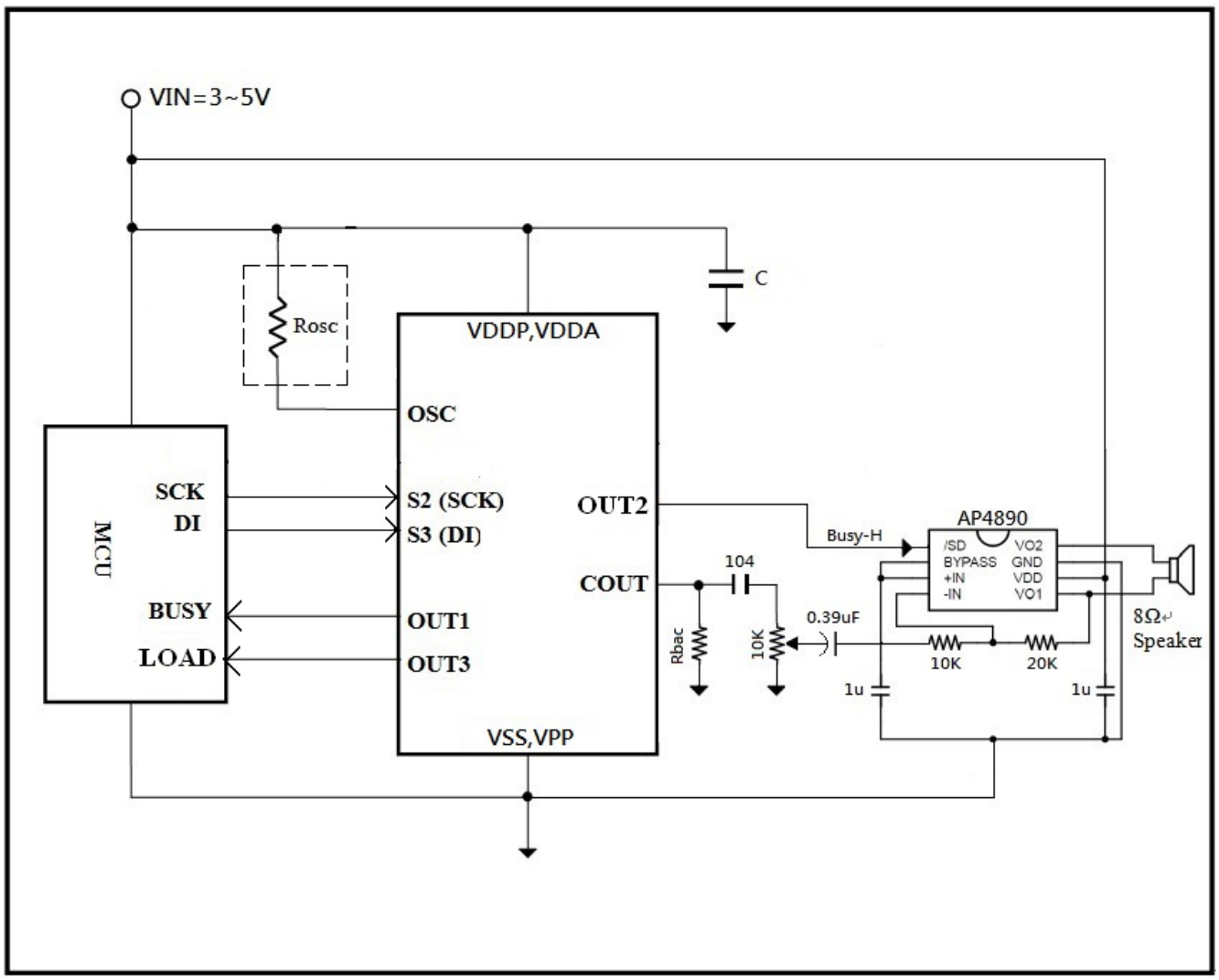


Fig. 19

MP3 Mode

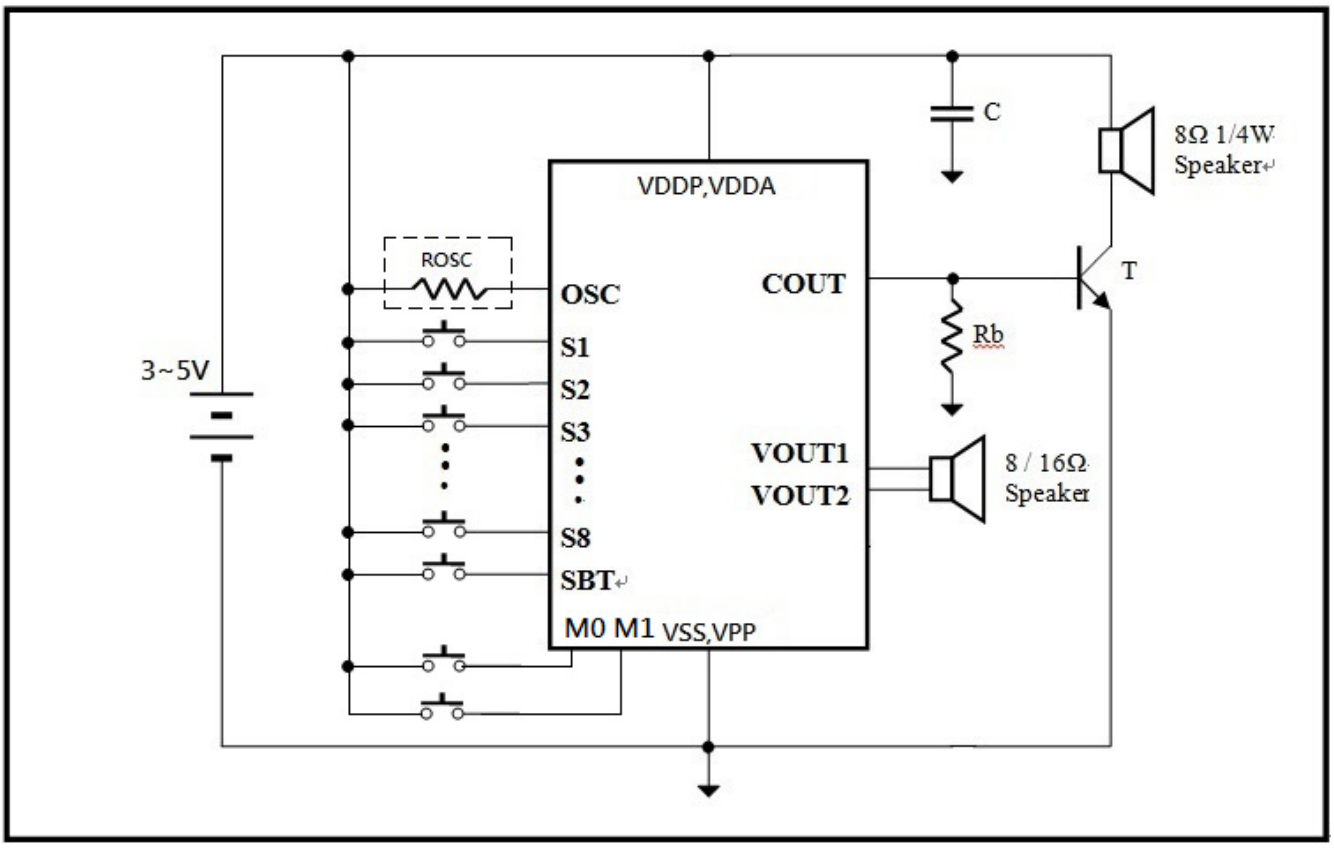
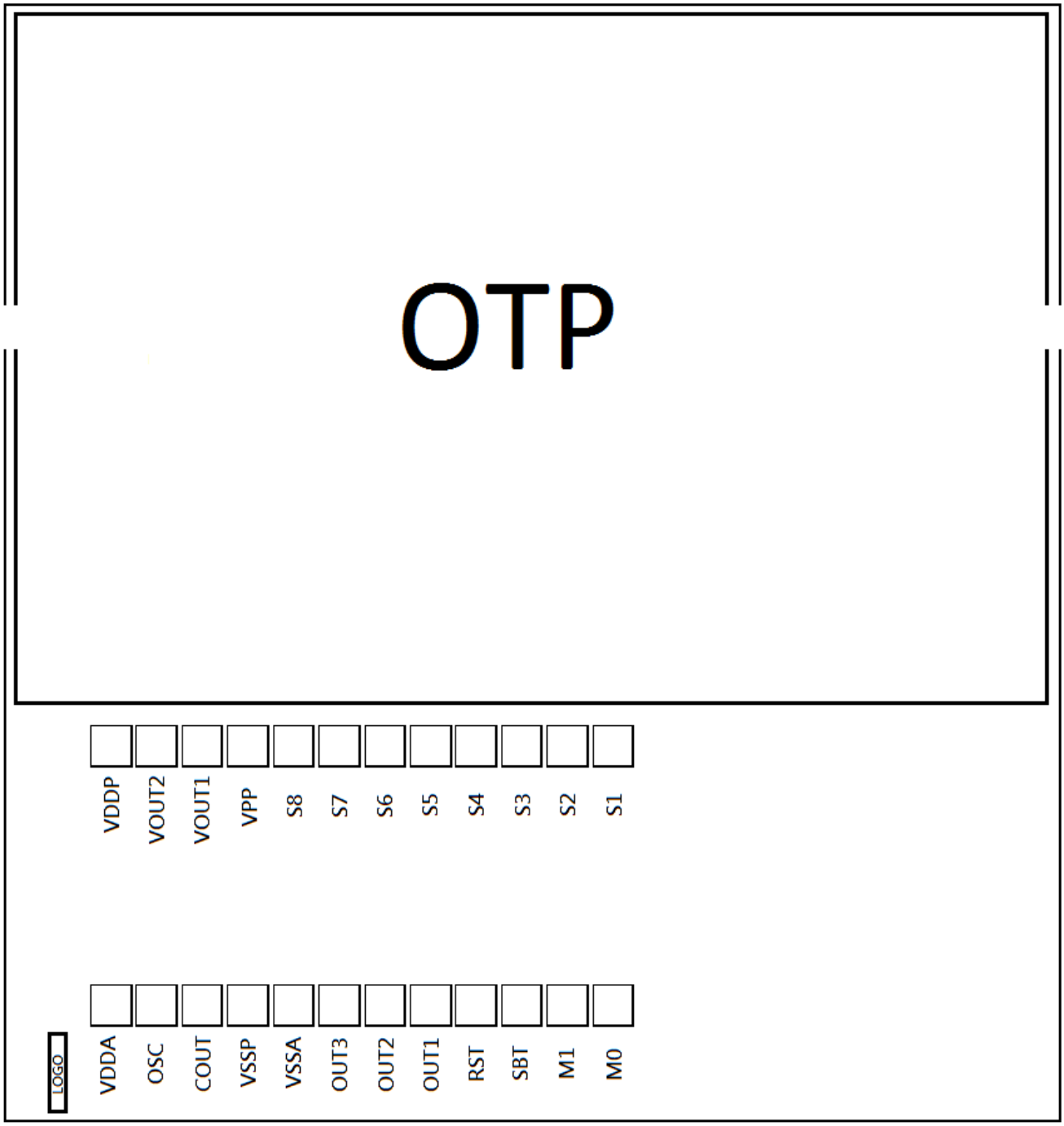


Fig. 20

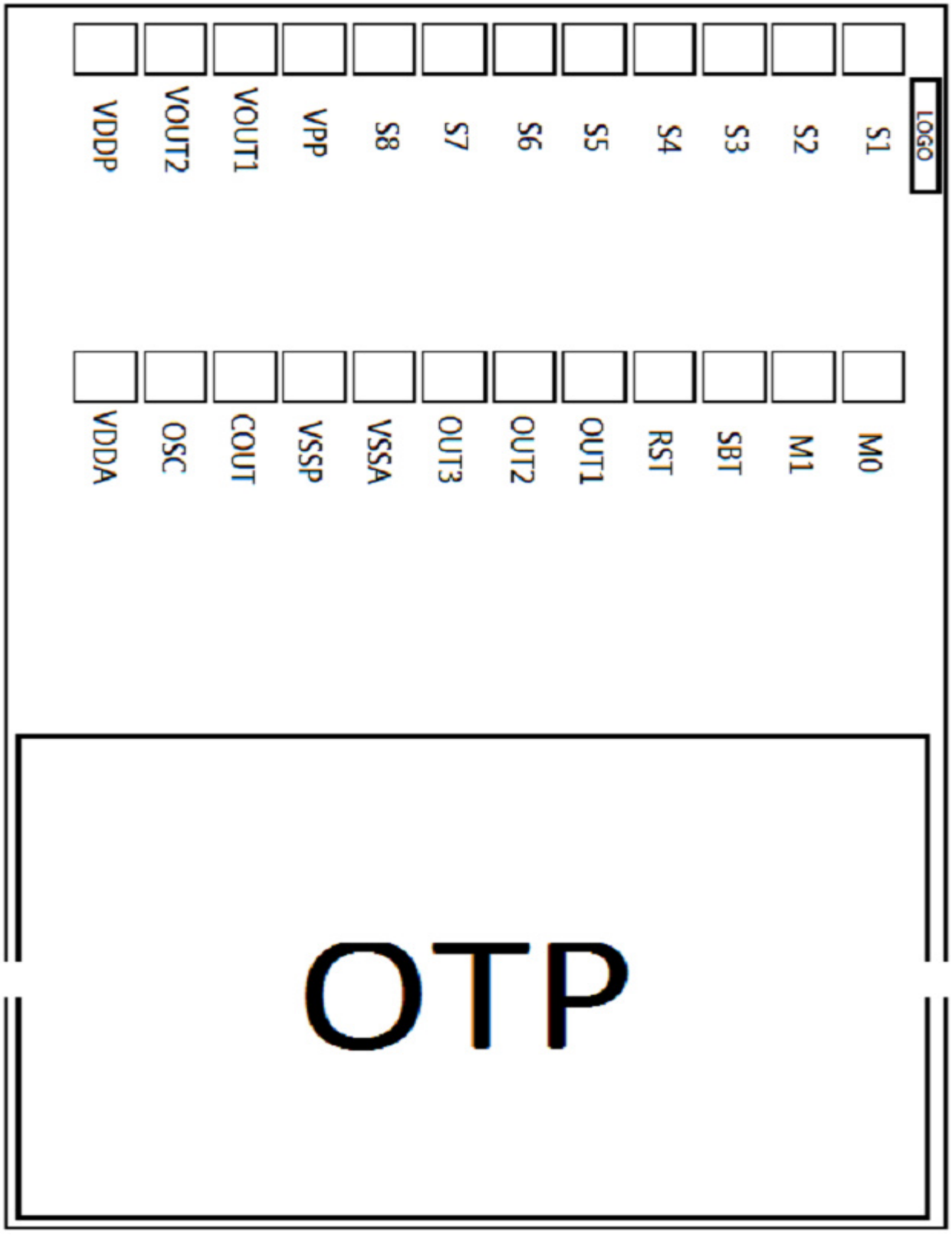
BONDING PAD DIAGRAMS (aP89682K/aP89341K)



Notes:

1. Between VPP and GND should add 10KΩ.
2. VDDA and VDDP should be connected to the Positive Power Supply.
3. VSSA and VSSP should be connected to the Power GND.
4. Substrate should be connected to the Power GND.

BONDING PAD DIAGRAMS (aP89170K/aP89085K)

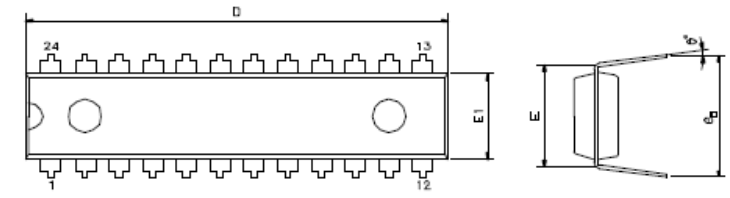


Notes:

1.Between VPP and GND should add 10KΩ.
2.VDDA and VDDP should be connected to the Positive Power Supply.
3.VSSA and VSSP should be connected to the Power GND.
4.Substrate should be connected to the Power GND.

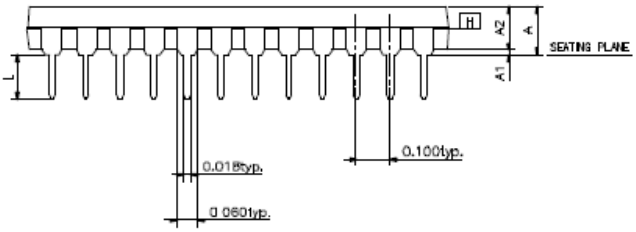
PACKAGES DIMENSION OUTLINES

24-Pin 300mil P-DIP Package



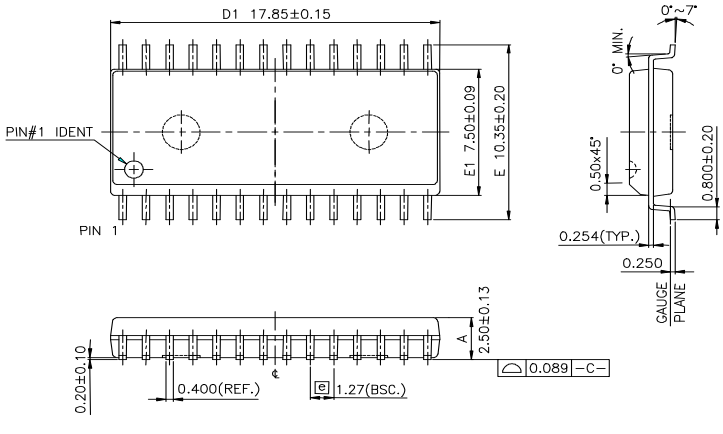
SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	1.230	1.250	1.280
E		0.300 BSC.	
E1	0.253	0.258	0.263
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

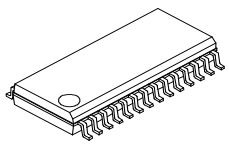
UNIT : INCH



NOTES:
1. JEDEC OUTLINE : MS-001 AF
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE H COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

28-Pin 300mil SOP Package





NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLMETERS (MM).
2. DIMENSION D1 & E1 DOES NOT INCLUDE MOLD PROTRUSION.
3. COPLANARITY OF ALL LEADS SHALL BE (BEFORE TEST) 0.089 MAX. FORM THE SEATING PLANE. UNLESS OTHERWISE SPECIFIED.
4. GENERAL PHYSICAL OUTLINE SPEC IS REFER TO TMC'S FINAL INSPECTION SPEC UNLESS OTHERWISE SPECIFIED.

HISTORY

2015/03/10

aP89682K_341K__170K_085K SPEC.