TEXAS INSTRUMENTS

SN74LVC1G3157

SCES424K – JANUARY 2003 – REVISED JANUARY 2017

# SN74LVC1G3157 Single-Pole Double-Throw Analog Switch

1 Features

- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)
- 1.65-V to 5.5-V V_{CC} Operation
- Useful for Both Analog and Digital Applications
- Qualified For 125°C operation
- Specified Break-Before-Make Switching
- Rail-to-Rail Signal Handling
- Operating Frequency Typically 340 MHz at Room Temperature
- High Degree of Linearity
- High Speed, Typically 0.5 ns
  (V_{CC} = 3 V, C_L = 50 pF)
- Low ON-State Resistance, Typically ≠6 Ω
  (V_{CC} = 4.5 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

2 Applications

- Wearables and Mobile Devices
- Portable Computing
- Internet of Things (IoT)
- Audio Signal Routing
- Remote Radio Unit
- Portable Medical Equipment
- Surveillance
- Home Automation
- I2C/SPI/UART Bus Multiplexing
- Wireless Charging

3 Description

This single-pole double-throw (SPDT) analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G3157 device can handle both analog and digital signals. The SN74LVC1G3157 device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1G3157DBV	SOT-23 (6)	2.90 mm × 1.60 mm
SN74LVC1G3157DCK	SC70 (6)	2.00 mm × 1.25 mm
SN74LVC1G3157DRL	SOT (6)	1.60 mm × 1.20 mm
SN74LVC1G3157DRY	SON (6)	1.45 mm × 1.00 mm
SN74LVC1G3157YZP	DSBGA (6)	1.41 mm × 0.91 mm
SN74LVC1G3157DSF	SON (6)	1.00 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (June 2016) to Revision K   **Page**

- Added new applications to *Applications* section 1
- Added Operating free-air temperature, T_A for BGA and all other packages in *Recommended Operating Conditions* 5
- Added 125°C data to Electrical Characteristics table. 6
- Added 85°C to title to differentiate from new 125°C *Switching Characteristics* section. 7
- Added 125°C *Switching Characteristics* section and data. 8

Changes from Revision I (June 2015) to Revision J   **Page**

- Deleted 200-V Machine Model (A115-A) from *Features* 1
- Changed Operating Frequency from 300 MHz to 340 MHz throughout... 1
- Updated *Device Information* table 1
- Updated pinout images for all packages 4
- Added temperature ranges for Storage temperature, T_{stg} and Junction temperature, T_J in *Absolute Maximum Ratings* 5
- Changed MAX value ±1 to ±0.1 for I_{off} and I_{IN} in *Electrical Characteristics* table.. 6
- Added *Receiving Notification of Documentation Updates* section 18

Changes from Revision H (May 2012) to Revision I   **Page**

- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Updated document to new TI data sheet format. 1
- Updated *Features*. 1

Changes from Revision G (September 2011) to Revision H   **Page**

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View

B2	1	6	S
GND	2	5	V_{CC}
B1	3	4	A

Not to scale

DCK Package
6-Pin SC70
Top View

B2	1	6	S
GND	2	5	V_{CC}
B1	3	4	A

Not to scale

DRY Package
6-Pin SON
Top View

B2	1	6	S
GND	2	5	V_{CC}
B1	3	4	A

Not to scale

DRL Package
6-Pin SOT
Top View

B2	1	6	S
GND	2	5	V_{CC}
B1	3	4	A

Not to scale

DSF Package
6-Pin SON
Top View

B2	1	6	S
GND	2	5	V_{CC}
B1	3	4	A

Not to scale

YZP Package
6-Pin DSBGA
Bottom View

	1	2
C	B1	A
B	GND	V_{CC}
A	B2	S

Not to scale
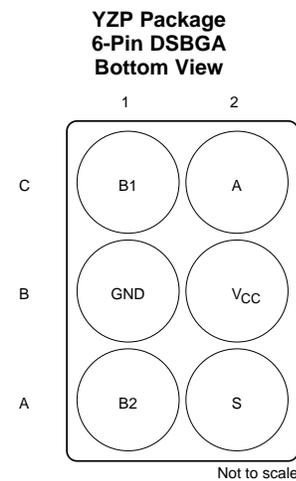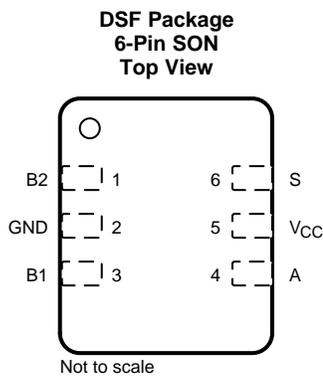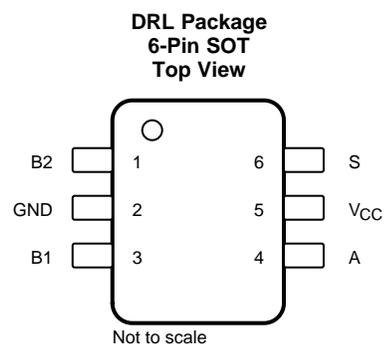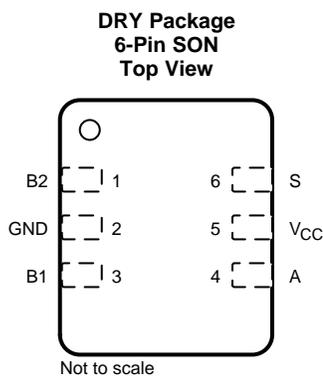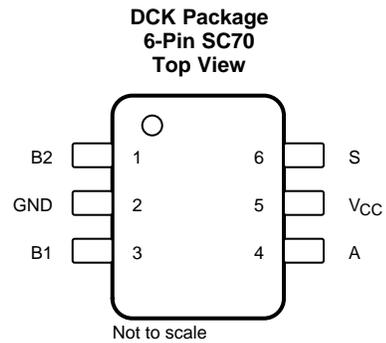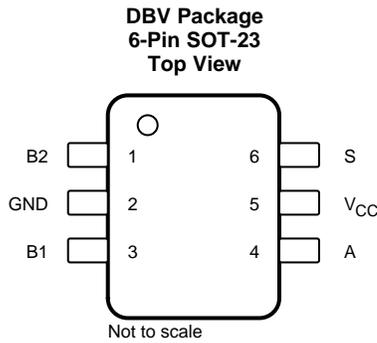
Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23, SC70, SON, or SOT	DSBGA		
B2	1	A1	I/O	Switch I/O. Set S high to enable.
GND	2	B1	—	Ground
B1	3	C1	I/O	Switch I/O. Set S low to enable.
A	4	C2	I/O	Common terminal
V_{CC}	5	B2	—	Power supply
S	6	A2	I	Select

Product Folder Links: *SN74LVC1G3157*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[2]		−0.5	6.5	V
V_{IN}	Control input voltage[2][3]		−0.5	6.5	V
$V_{I/O}$	Switch I/O voltage[2][3][4][5]		−0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		−50	mA
$I_{I/O}$	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		±50	mA
$I_{I/O}$	On-state switch current[6]	$V_{I/O} = 0$ to V_{CC}		±128	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for $V_{I/O}$.
(6) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	Switch input or output voltage		0	V_{CC}	V
V_{IN}	Control input voltage		0	5.5	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	V_{CC} × 0.75		V
		V_{CC} = 2.3 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		V_{CC} × 0.25	V
		V_{CC} = 2.3 V to 5.5 V		V_{CC} × 0.3	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature	BGA package (YZP)	−40	85	°C
		All other packages (DBV, DCK, DRL, DRY, DSF)	−40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

| THERMAL METRIC[1] | SN74LVC1G3157 | | | | | UNIT |
| | DBV (SOT-23) | DCK (SC70) | DRL (SOT) | DRY (SON) | YZP (DSBGA) | |
	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	165	259	142	234	123	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | V_{CC} | T_A = -40 to 85°C | | | T_A = -40 to 125°C | | | UNIT |
						MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
r_{on}	ON-state switch resistance[2]	See Figure 1 and Figure 2	V_I = 0 V	I_O = 4 mA	1.65 V		11	20		11	20	Ω
			V_I = 1.65 V	I_O = −4 mA			15	50		15	50	
			V_I = 0 V	I_O = 8 mA	2.3 V		8	12		8	12	
			V_I = 2.3 V	I_O = −8 mA			11	30		11	30	
			V_I = 0 V	I_O = 24 mA	3 V		7	9		7	9	
			V_I = 3 V	I_O = −24 mA			9	20		9	20	
			V_I = 0 V	I_O = 30 mA	4.5 V		6	7		6	7	
			V_I = 2.4 V	I_O = −30 mA			7	12		7	12	
			V_I = 4.5 V	I_O = −30 mA			7	15		7	15	
r_{range}	ON-state switch resistance over signal range[2][3]	$0 ≤ V_{Bn} ≤ V_{CC}$ (see Figure 1 and Figure 2)	I_A = −4 mA		1.65 V			140			140	Ω
			I_A = −8 mA		2.3 V			45			45	
			I_A = −24 mA		3 V			18			18	
			I_A = −30 mA		4.5 V			10			10	
Δr_{on}	Difference of ON-state resistance between switches[2][4][5]	See Figure 2	V_{Bn} = 1.15 V	I_A = −4 mA	1.65 V			0.5			0.5	Ω
			V_{Bn} = 1.6 V	I_A = −8 mA	2.3 V			0.1			0.3	
			V_{Bn} = 2.1 V	I_A = −24 mA	3 V			0.1			0.3	
			V_{Bn} = 3.15 V	I_A = −30 mA	4.5 V			0.1			0.2	
$r_{on(flat)}$	ON resistance flatness[2][4][6]	$0 ≤ V_{Bn} ≤ V_{CC}$	I_A = −4 mA		1.65 V			110			110	Ω
			I_A = −8 mA		2.3 V			26			40	
			I_A = −24 mA		3 V			9			10	
			I_A = −30 mA		4.5 V			4			5	
I_{off}[7]	OFF-state switch leakage current	$0 ≤ V_I, V_O ≤ V_{CC}$ (see Figure 3)			1.65 V to 5.5 V			±1			±1	μA
							±0.05	±0.1[1]		±0.05	±0.1	
$I_{S(on)}$	ON-state switch leakage current	$V_I = V_{CC}$ or GND, V_O = Open (see Figure 4)			5.5 V			±1			±1	μA
							±0.1[1]				±0.1[1]	

(1) T_A = 25°C
(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages on the two (A or B) ports.
(3) Specified by design
(4) $\Delta r_{on} = r_{on(max)} − r_{on(min)}$ measured at identical V_{CC}, temperature, and voltage levels
(5) This parameter is characterized, but not production tested.
(6) Flatness is defined as the difference between the maximum and minimum values of on-state resistance over the specified range of conditions.
(7) I_{off} is the same as $I_{S(off)}$ (off-state switch leakage current).

Product Folder Links: *SN74LVC1G3157*

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = -40 to 85°C MIN	TYP[1]	MAX	T_A = -40 to 125°C MIN	TYP[1]	MAX	UNIT
I_{IN}	Control input current	$0 \leq V_{IN} \leq V_{CC}$	0 V to 5.5 V			±1			±1	μA
					±0.05	±0.1[1]		±0.05	±0.1	
I_{CC}	Supply current	S = V_{CC} or GND	5.5 V		1	10			35	μA
ΔI_{CC}	Supply-current change	S = V_{CC} – 0.6 V	5.5 V			500			500	μA
C_i	Control input capacitance	S	5 V		2.7			2.7		pF
$C_{io(off)}$	Switch input/output capacitance	Bn	5 V		5.2			5.2		pF
$C_{io(on)}$	Switch input/output capacitance	Bn	5 V		17.3			17.3		pF
		A			17.3			17.3		

6.6 Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response[1] (switch on)	A or Bn	Bn or A	R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	1.65 V	340	MHz
				2.3 V	340	
				3 V	340	
				4.5 V	340	
Crosstalk[2] (between switches)	B1 or B2	B2 or B1	R_L = 50 Ω, f_{in} = 10 MHz (sine wave) (see Figure 7)	1.65 V	−54	dB
				2.3 V	−54	
				3 V	−54	
				4.5 V	−54	
Feed through attenuation[2] (switch off)	A or Bn	Bn or A	C_L = 5 pF, R_L = 50 Ω, f_{in} = 10 MHz (sine wave) (see Figure 8)	1.65 V	−57	dB
				2.3 V	−57	
				3 V	−57	
				4.5 V	−57	
Charge injection[3]	S	A	C_L = 0.1 nF, R_L = 1 MΩ (see Figure 9)	3.3 V	3	pC
				5 V	7	
Total harmonic distortion	A or Bn	Bn or A	V_I = 0.5 V_{p-p}, R_L = 600 Ω, f_{in} = 600 Hz to 20 kHz (sine wave) (see Figure 10)	1.65 V	0.1%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads −3 dB.
(2) Adjust f_{in} voltage to obtain 0 dBm at input.
(3) Specified by design

6.7 Switching Characteristics 85°C

T_A = −40 to +85°C (see Figure 5 and Figure 11)

| PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V MIN	MAX	V_{CC} = 2.5 V ± 0.2 V MIN	MAX	V_{CC} = 3.3 V ± 0.3 V MIN	MAX	V_{CC} = 5 V ± 0.5 V MIN	MAX	UNIT
t_{pd}[1]	A or Bn	Bn or A		2		1.2		0.8		0.3	ns

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. The propagation delay is calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

Switching Characteristics 85°C (continued)

T_A = −40 to +85°C (see Figure 5 and Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{en}[2]	S	Bn	7	24	3.5	14	2.5	7.6	1.7	5.7	ns
t_{dis}[3]			3	13	2	7.5	1.5	5.3	0.8	3.8	
t_{B-M}[4]			0.5		0.5		0.5		0.5		ns

(2) t_{en} is the slower of t_{PZL} or t_{PZH}.
(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ}.
(4) Specified by design.

6.8 Switching Characteristics 125°C

T_A = −40 to +125°C (see Figure 5 and Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}[1]	A or Bn	Bn or A		2.0		1.2		0.8		0.5	ns
t_{en}[2]	S	Bn	1.0	24.5	1.0	14.5	2.5	8.0	1.7	6.0	ns
t_{dis}[3]			2.5	13.5	2.0	8.0	1.5	5.5	0.8	4.0	
t_{B-M}[4]			0.5		0.5		0.5		0.5		ns

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. The propagation delay is calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) t_{en} is the slower of t_{PZL} or t_{PZH}.
(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ}.
(4) Specified by design.

6.9 Typical Characteristics
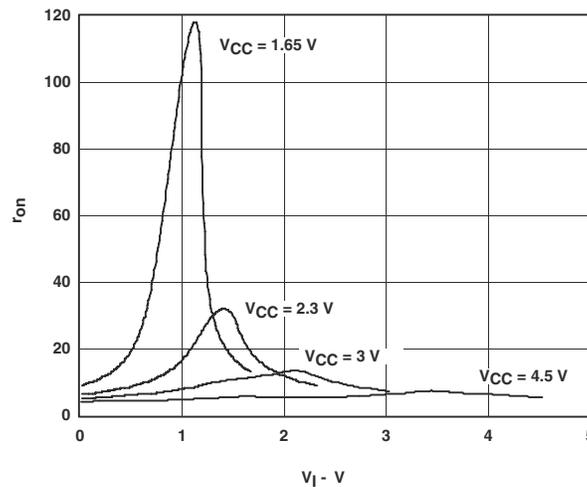
Figure 1. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

7 Parameter Measurement Information

SW	S
1	V_{IL}
2	V_{IH}

$$r_{on} = \left| \frac{V_I - V_O}{I_O} \right| \Omega$$
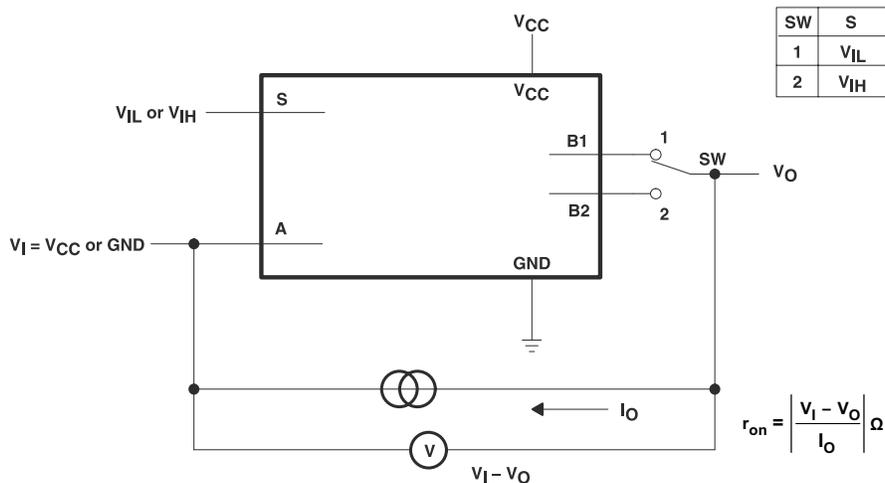
Figure 2. ON-State Resistance Test Circuit

SW	S
1	V_{IL}
2	V_{IH}
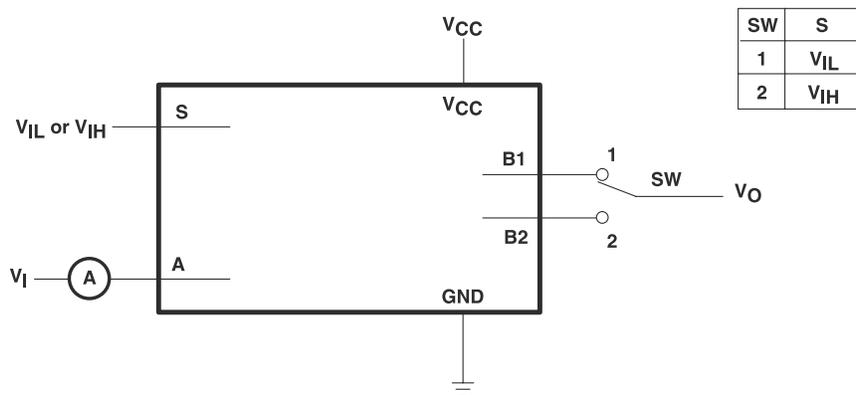
Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. OFF-State Switch Leakage-Current Test Circuit

SW	S
1	V_{IL}
2	V_{IH}

V_O = Open
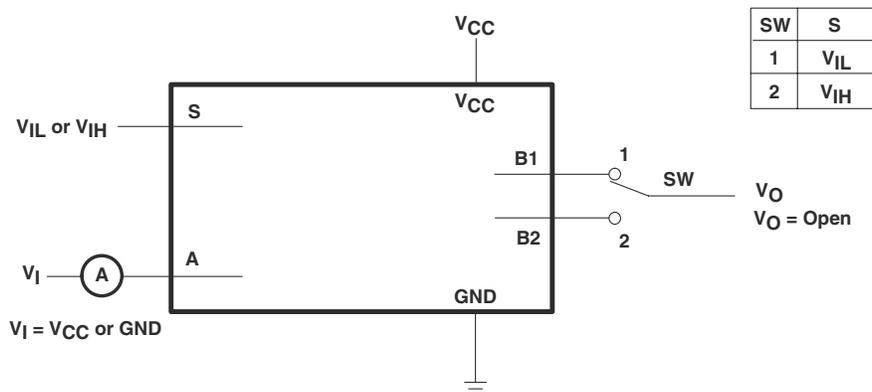
Figure 4. ON-State Switch Leakage-Current Test Circuit

Parameter Measurement Information (continued)
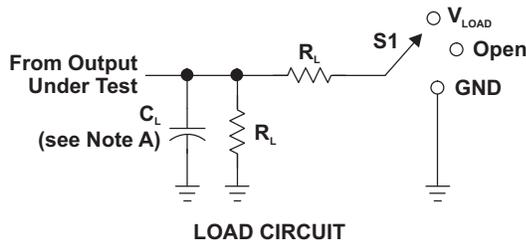
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS PULSE DURATION

VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING
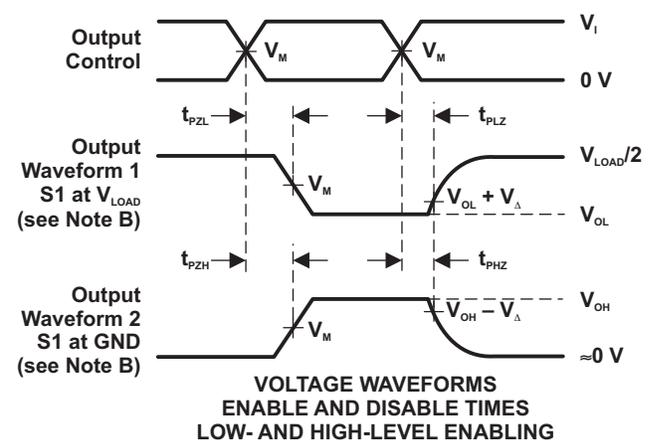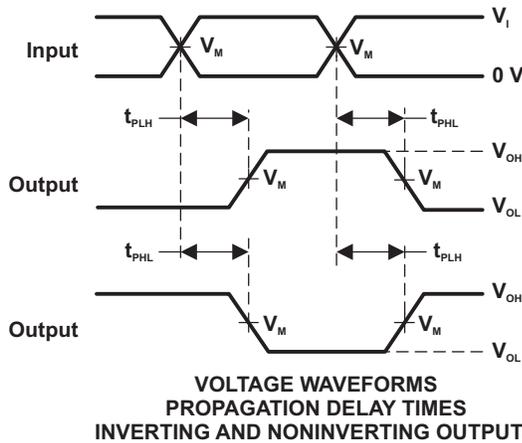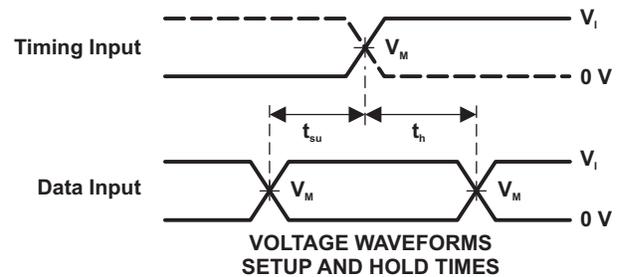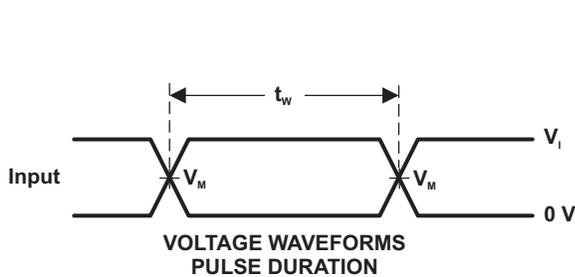
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

Product Folder Links: SN74LVC1G3157

Parameter Measurement Information (continued)

SW	S
1	V_{IL}
2	V_{IH}
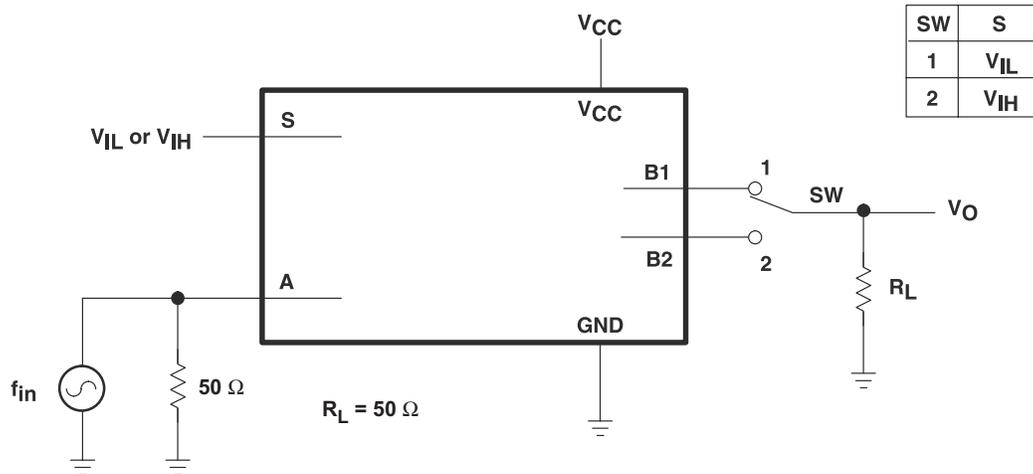
Figure 6. Frequency Response (Switch On)

S	TEST CONDITION
V_{IL}	$20\log_{10}(V_{O2}/V_I)$
V_{IH}	$20\log_{10}(V_{O1}/V_I)$
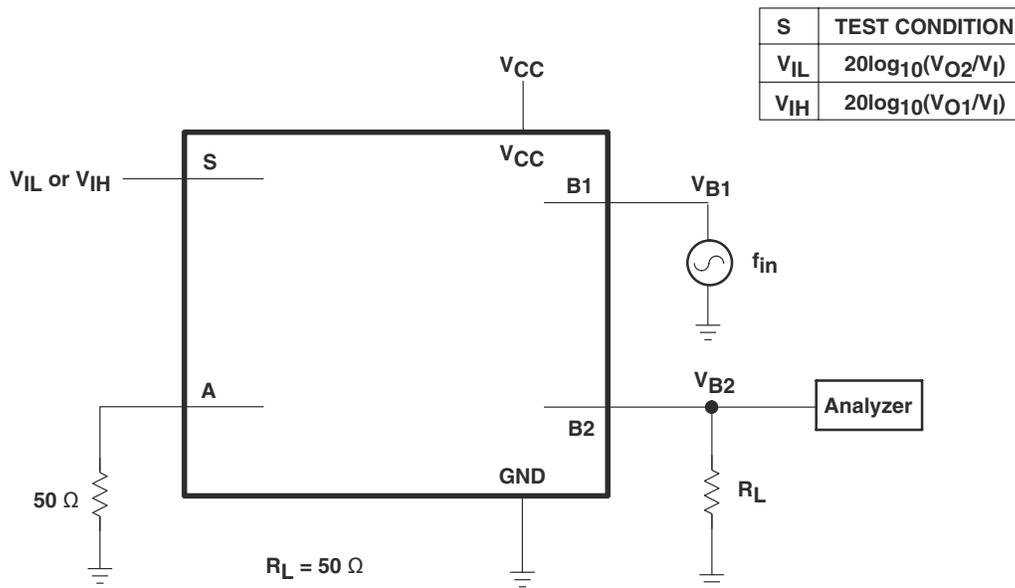
Figure 7. Crosstalk (Between Switches)

Product Folder Links: *SN74LVC1G3157*

Parameter Measurement Information (continued)

SW	S
1	V_{IL}
2	V_{IH}
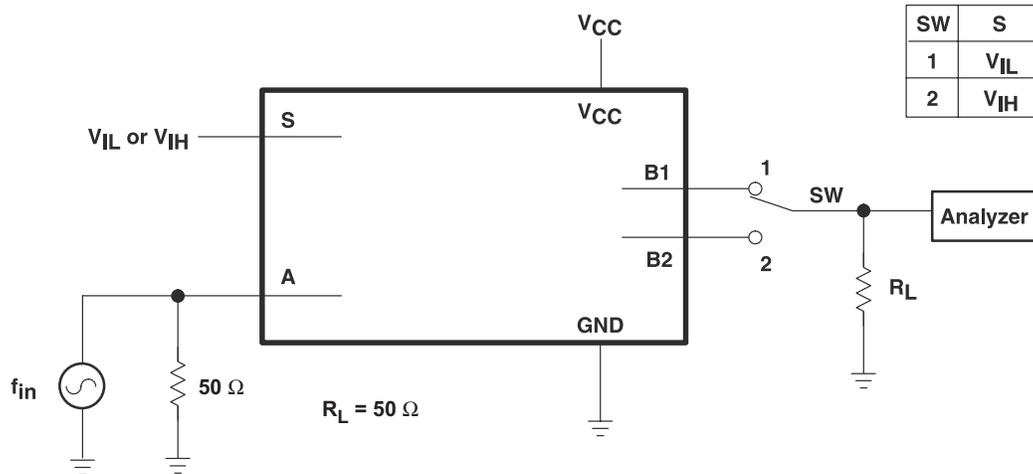
Figure 8. Feed Through

Figure 9. Charge-Injection Test

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Product Folder Links: *SN74LVC1G3157*

Parameter Measurement Information (continued)
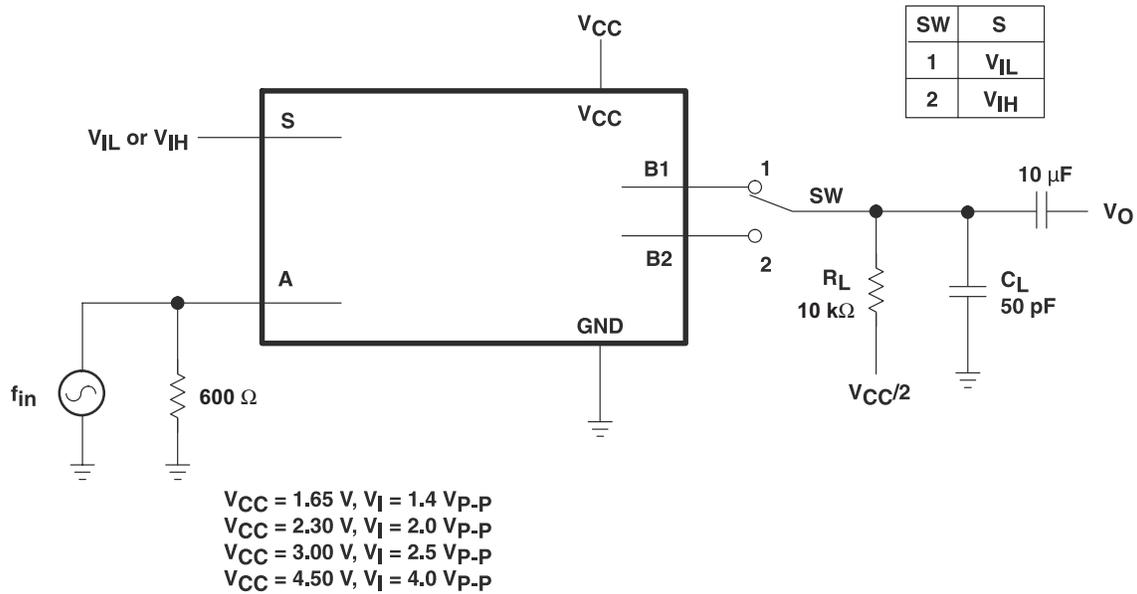
Figure 10. Total Harmonic Distortion
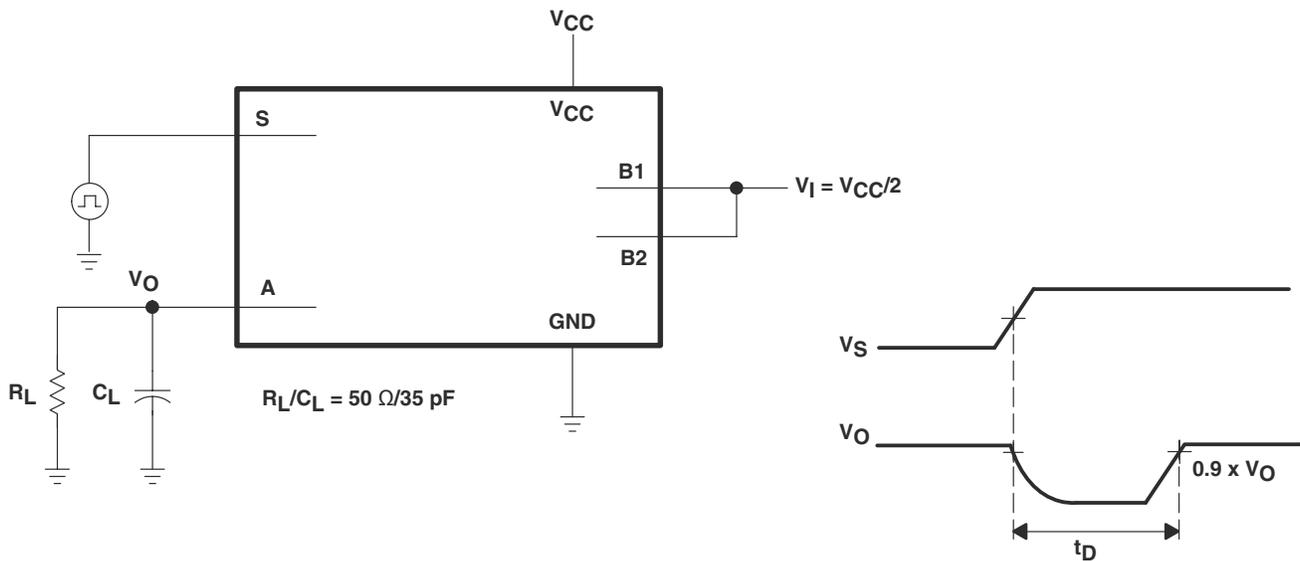
Figure 11. Break-Before-Make Internal Timing

Product Folder Links: *SN74LVC1G3157*

8 Detailed Description

8.1 Overview

The SN74LVC1G3157 device is a single-pole double-throw (SPDT) analog switch designed for 1.65-V to 5.5-V V_{CC} operation. The SN74LVC1G3157 device can handle analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

8.2 Functional Block Diagram
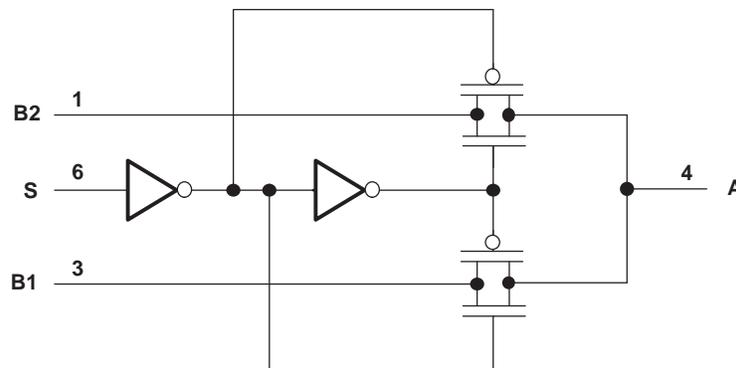
Figure 12. Logic Diagram (Positive Logic)

8.3 Feature Description

The 1.65-V to 5.5-V supply operation allows the device to function in many different systems comprised of different logic levels, allowing rail-to-rail signal switching. Either the B1 channel or the B2 channel is activated depending upon the control input. If the control input is low, B1 channel is selected. If the control input is high, B2 channel is selected.

8.4 Device Functional Modes

Table 1 lists the ON channel when one of the control inputs is selected.

Table 1. Function Table

CONTROL INPUTS	ON CHANNEL
L	B1
H	B2

Product Folder Links: *SN74LVC1G3157*

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G3157 SPDT analog switch is flexible enough for use in a variety of circuits such as analog audio routing, power-up monitor, memory sharing, and so on. For details on the applications, see SCYB014.

9.2 Typical Application
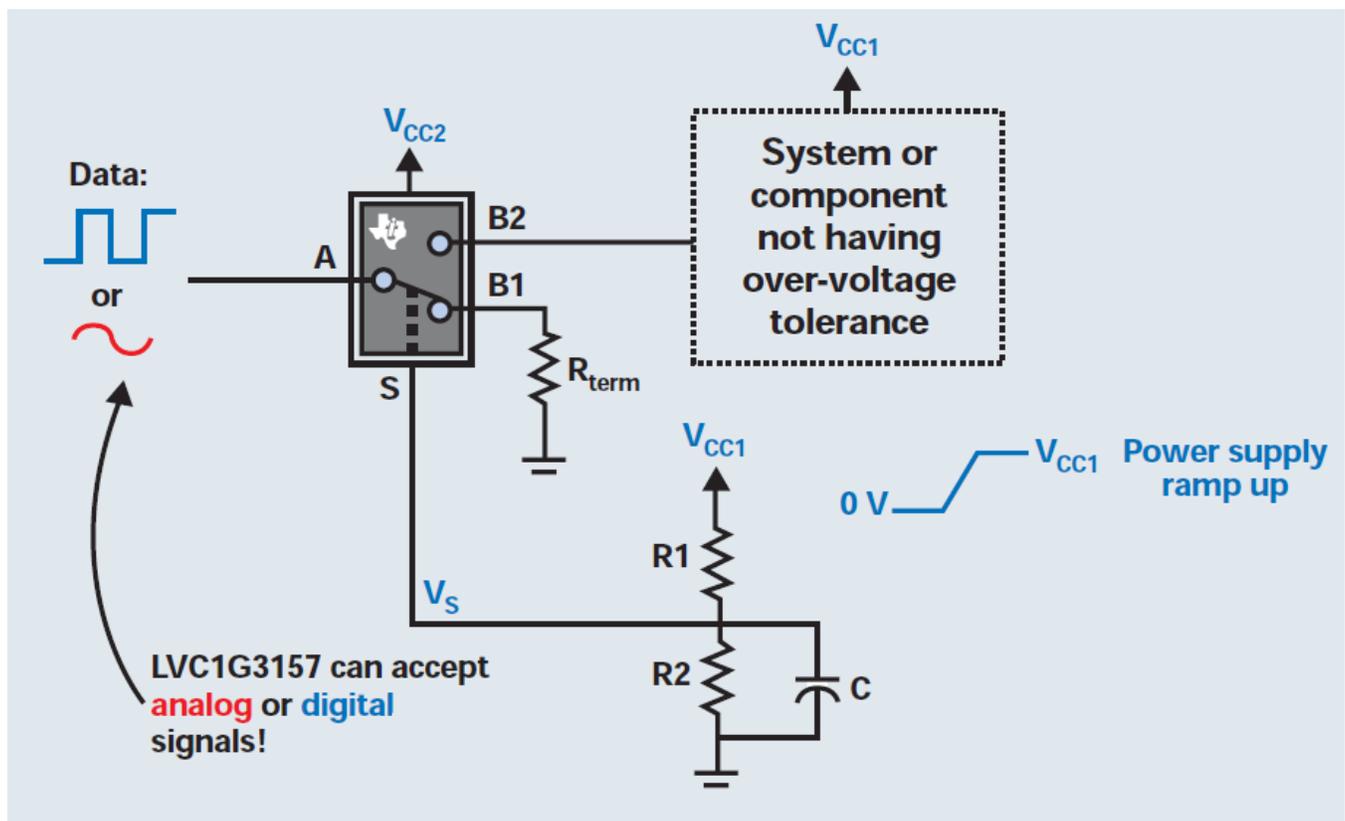
Figure 13. Typical Application Schematic

9.2.1 Design Requirements

The inputs can be analog or digital, but TI recommends waiting until V_{CC} has ramped to a level in *Recommended Operating Conditions* before applying any signals. Appropriate termination resistors should be used depending on the type of signal and specification. The Select pin should not be left floating; either pull up or pull down with a resistor that can be overdriven by a GPIO.

Typical Application (continued)

9.2.2 Detailed Design Procedure

Using this circuit idea, a system designer can ensure a component or subsystem power has ramped up before allowing signals to be applied to its input. This is useful for integrated circuits that do not have overvoltage tolerant inputs. The basic idea uses a resistor divider on the VCC1 power rail, which is ramping up. The RC time constant of the resistor divider further delays the voltage ramp on the select pin of the SPDT bus switch. By carefully selecting values for R1, R2, and C, it is possible to ensure that VCC1 will reach its nominal value before the path from A to B2 is established, thus preventing a signal being present on an I/O before the device/system is powered up. To ensure the minimum desired delay is achieved, the designer should use Equation 1 to calculate the time required from a transition from ground (0 V) to half the supply voltage (VCC1/2).

$$\text{Set} \left(\frac{R2}{R1 \; R2} \times V_{CC1} > V_{IH} \right) \text{of the select pin}$$

(1)

Choose Rs and C to achieve the desired delay.

When V_S goes high, the signal will be passed.

9.2.3 Application Curve
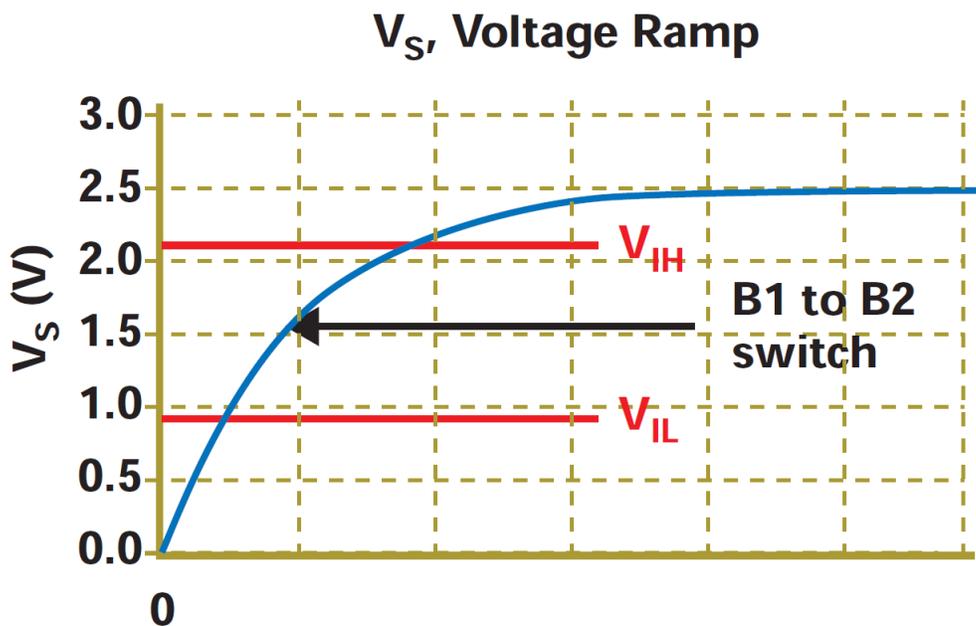
Figure 14. V_S Voltage Ramp

Product Folder Links: *SN74LVC1G3157*

10 Power Supply Recommendations

Most systems have a common 3.3-V or 5-V rail that can supply the V_{CC} pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can be used to provide supply to this device from another voltage rail.

11 Layout

11.1 Layout Guidelines

TI recommends keeping signal lines as short as possible. TI also recommends incorporating microstrip or stripline techniques when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Do not place this device too close to high-voltage switching components, as they may interfere with the device.

11.2 Layout Example
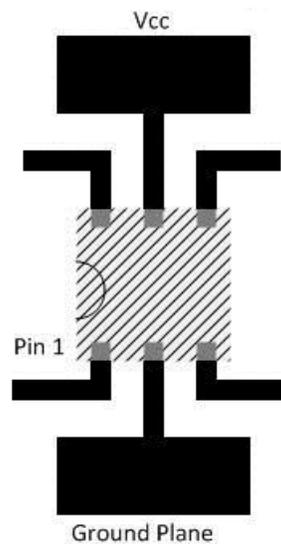
Figure 15. Recommended Layout Example

Product Folder Links: *SN74LVC1G3157*

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:
- *Implications of Slow or Floating CMOS Inputs*, SCBA004.
- *SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches*, SCYB014

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVC1G3157DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC5F	Samples
74LVC1G3157DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CC5F	Samples
74LVC1G3157DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55 ~ C5F ~ C5K ~ C5R)	Samples
74LVC1G3157DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55 ~ C5F ~ C5K ~ C5R)	Samples
74LVC1G3157DRLRG4	ACTIVE	SOT-OTHER	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C57 ~ C5R)	Samples
74LVC1G3157DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(CC55 ~ CC5F ~ CC5K ~ CC5R)	Samples
SN74LVC1G3157DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55 ~ C5F ~ C5K ~ C5R)	Samples
SN74LVC1G3157DRLR	ACTIVE	SOT-OTHER	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C57 ~ C5R)	Samples
SN74LVC1G3157DRY2	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C5	Samples
SN74LVC1G3157YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G3157 :

• Automotive: SN74LVC1G3157-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
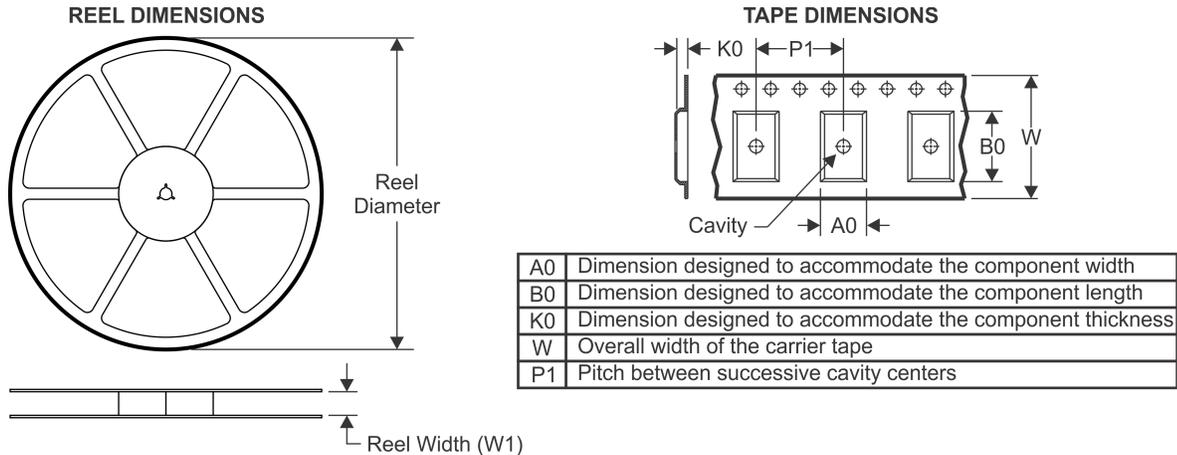
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G3157DBVRG4	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT-OTHER	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT-OTHER	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G3157DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74LVC1G3157DRY2	SON	DRY	6	5000	180.0	8.4	1.65	1.2	0.7	4.0	8.0	Q3
SN74LVC1G3157DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G3157DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS
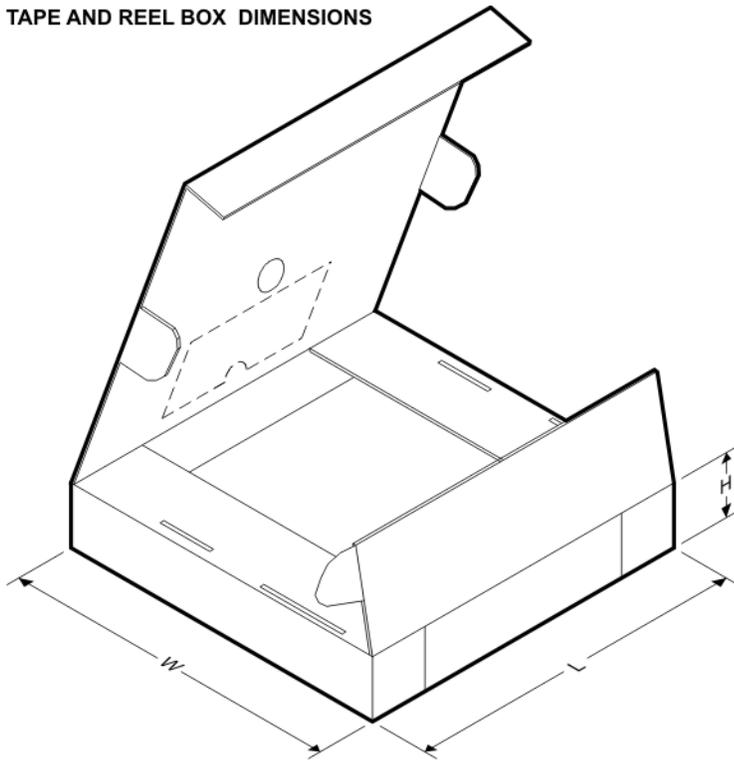
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G3157DBVRG4	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	205.0	200.0	33.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G3157DRLR	SOT-OTHER	DRL	6	4000	184.0	184.0	19.0
SN74LVC1G3157DRLR	SOT-OTHER	DRL	6	4000	202.0	201.0	28.0
SN74LVC1G3157DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G3157DRY2	SON	DRY	6	5000	202.0	201.0	28.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	203.0	203.0	35.0
SN74LVC1G3157DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

A

$\dfrac{1,70}{1,50}$

6X $\dfrac{0,27}{0,13}$

B

6   5   4

△C

$\dfrac{1,30}{1,10}$

$\dfrac{1,70}{1,50}$

Pin 1 Index Area

1   2   3

0,50

6X $\dfrac{0,25}{0,15}$

⊕	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		

$\dfrac{0,60}{0,50}$

0,05 C

Seating Plane

$\dfrac{0,05}{0,00}$

C

$\dfrac{0,18}{0,08}$

1   2   3

6X $\dfrac{0,40}{0,20}$

6   5   4

Bottom View

4205622−3/D   08/2007

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
      △C Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.
          Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
         D. JEDEC package registration is pending.

TEXAS
INSTRUMENTS
www.ti.com

DRL (R−PDSO−N6)   PLASTIC SMALL OUTLINE

Example Board Layout

1,00

0,45

1,80   0,90

0,30

0,50

Example
Non−Soldermask Defined Pad

Example
Pad Geometry

Example
Non−Soldermask Opening

0,05
All Around

Example Stencil Design
(Note E)

1,00

0,55

1,90   0,80

0,40

0,50

4208207−3/E 06/12

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate designs.
         D.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
         E.   Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
         F.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         G.   Side aperture dimensions over−print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
              if stencil manufacturing process allows for sufficient release at smaller opening.

TEXAS
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www.ti.com

DBV (R−PDSO−G6)   PLASTIC SMALL−OUTLINE PACKAGE

DETAIL:
OPTIONAL ORIENTATION
MARKING

Pin 1
Index Area

Pin 1
Index Area
(See Detail)

Gage Plane

Seating Plane

1,45 MAX

4073253-5/N 12/14

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
        D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
        E. Falls within JEDEC MO−178 Variation AB, except minimum lead width.

DBV (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593−4/C 08/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC−7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

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DCK (R−PDSO−G6)　　　　　　　PLASTIC SMALL−OUTLINE PACKAGE

4093553−4/G　01/2007

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
　　　　　D.　Falls within JEDEC MO−203 variation AB.
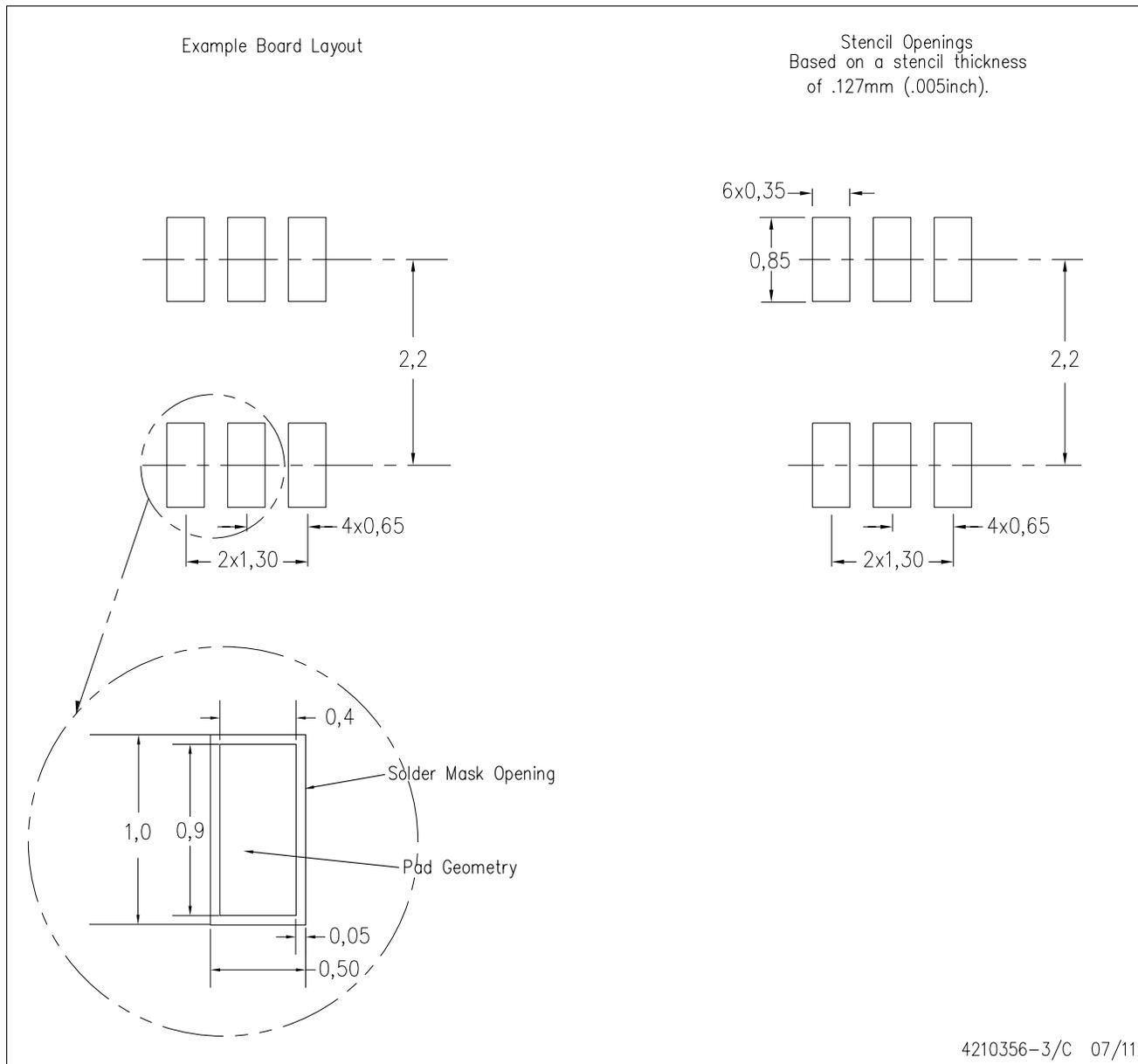
TEXAS
INSTRUMENTS
www.ti.com

DCK (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

4x0,65

2x1,30

4x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−3/C 07/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D.   Publication IPC−7351 is recommended for alternate designs.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
              metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

DRY (R−PUSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

$\dfrac{1,50}{1,40}$ [A]

[B]

6   5   4

$\dfrac{1,05}{0,95}$

1   2   3

Pin 1 Index Area

$\dfrac{0,60}{0,51}$

// | 0,05 | C

0,15 Nominal
Lead Frame [D]

Seating Plane

△ | 0,05 | C

$\dfrac{0,05}{0,00}$
Seating Height

[C]

1,00

0,50

1   2   3

6X $\dfrac{0,10}{0,00}$

5X $\dfrac{0,45}{0,25}$

[F] Pin 1 Identifier
Pin shape will be
modified per device.

5X $\dfrac{0,35}{0,25}$

6   5   4

6X $\dfrac{0,25}{0,15}$

⊕	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		

Bottom View
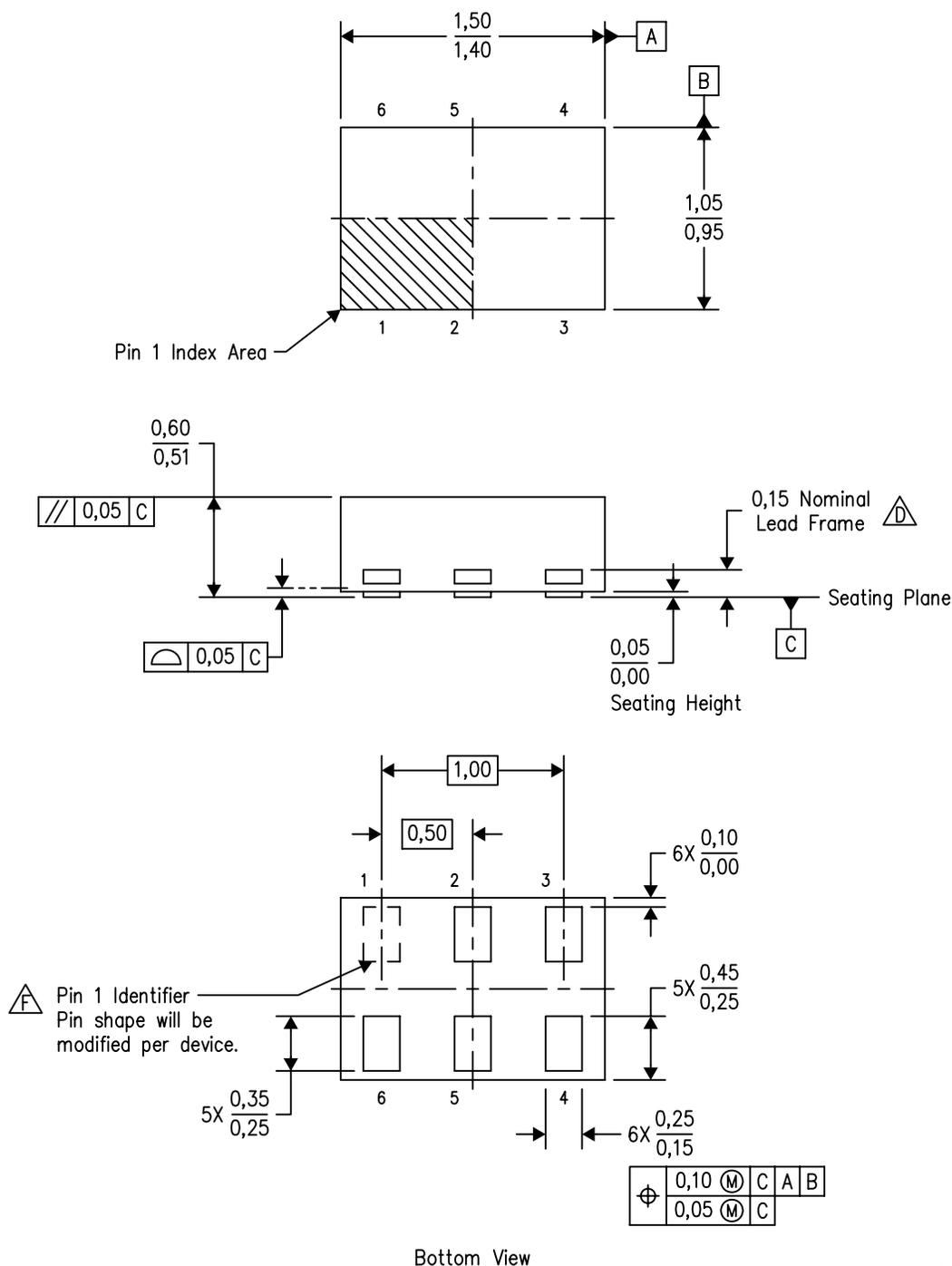
4207181/F   12/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   SON (Small Outline No−Lead) package configuration.
   [D]   The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
         E.   This package complies to JEDEC MO−287 variation UFAD.
   [F]   See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R−PUSON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

Example Board Layout

Example Stencil Design
(Note E, F, G)

Example Solder Mask Clearance
(Note D)

Example Pad Geometry
(Note C)

4208310/E 02/13

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over−print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
if stencil manufacturing process allows for sufficient release at smaller opening.

DSF (S-PX2SON-N6)   PLASTIC SMALL OUTLINE NO-LEAD

A |→| 1.05 |←| B
         0.95

PIN 1 INDEX AREA

1.05
0.95

0.4 MAX

C

SEATING PLANE

⌒ | 0.05 Ⓜ | C

(0.11) TYP

0.05
0.00

SYMM
₵

3 ▭   ▭ 4

2X
0.7

SYMM
₵

4X
0.35

6

1 ▭   ▭

6X 0.22
    0.12

(0.1)
PIN 1 ID

6X 0.45
    0.35

⊕ | 0.07 Ⓜ | C | AⓈ | BⓈ
   | 0.05 Ⓜ | C

4208186/F   10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

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DSF (S−PX2SON−N6)   PLASTIC SMALL OUTLINE NO−LEAD

Land Pattern

Stencil Pattern

0.20

0.35

0.53

0.15 1.20

0.70

Contact your PCB vendor for
allowable Solder Mask clearance (Notes C, D.)

0.53

0.20

0.165

0.35

0.53

0.15 1.20

0.70

4210277/D 05/12

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
            If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
        E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
        F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
        H. Component placement force should be minimized to prevent excessive paste block deformation.

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B ◄── E ──► A

BALL A1
CORNER

D

0.5 MAX

C

SEATING PLANE

0.19
0.15

BALL TYP

⌒ 0.05 C

0.5 TYP

C

SYMM
₵
B

1
TYP

0.5
TYP
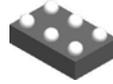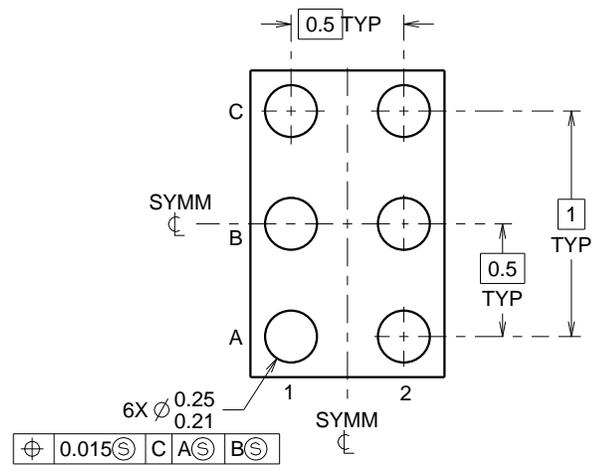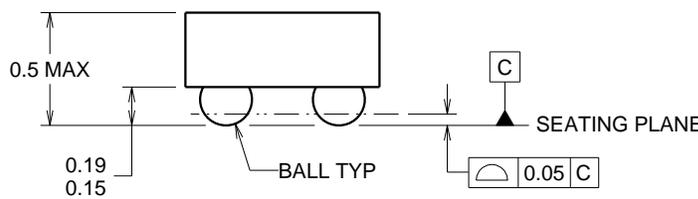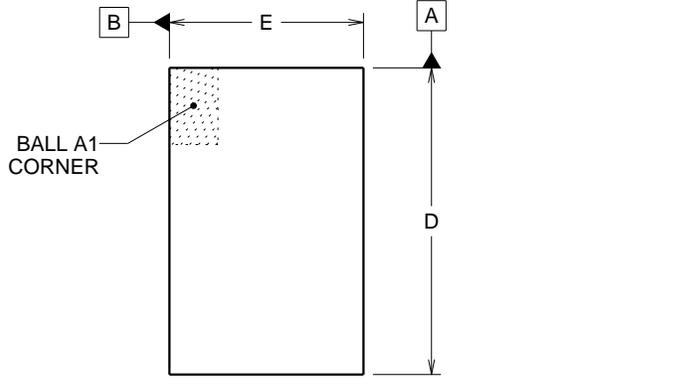
D: Max = 1.418 mm, Min =1.357 mm

E: Max = 0.918 mm, Min =0.857 mm

A

6X ∅ 0.25
0.21

1   2

SYMM
₵

⊕ 0.015Ⓢ C AⓈ BⓈ

4219524/A   06/2014

NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

6X (⌀ 0.225)

(0.5) TYP

(0.5) TYP

1   2

A

B   SYMM ℄

C

SYMM ℄
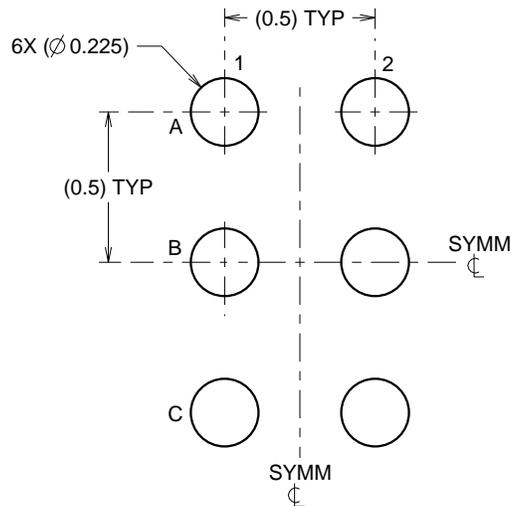
LAND PATTERN EXAMPLE
SCALE:40X

(⌀ 0.225) METAL

0.05 MAX

SOLDER MASK OPENING

NON-SOLDER MASK DEFINED (PREFERRED)

0.05 MIN

METAL UNDER MASK

(⌀ 0.225) SOLDER MASK OPENING

SOLDER MASK DEFINED
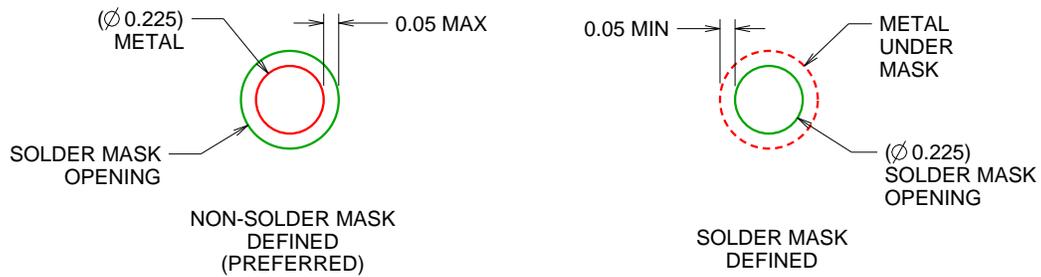
SOLDER MASK DETAILS
NOT TO SCALE

4219524/A   06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

(0.5) TYP

6X (□ 0.25)

(R0.05) TYP

1　2

A

(0.5) TYP

B　SYMM ℄

METAL TYP

C

SYMM ℄
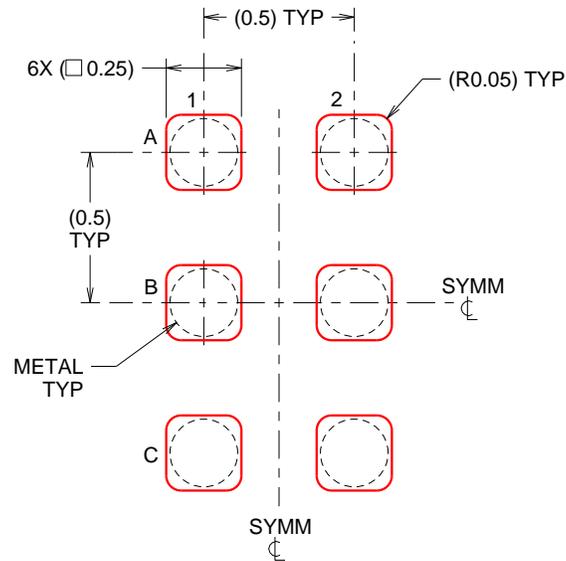
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A   06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.