PalmMicro
Communications, Inc.

AR1688

Datasheet(Version 2.0)

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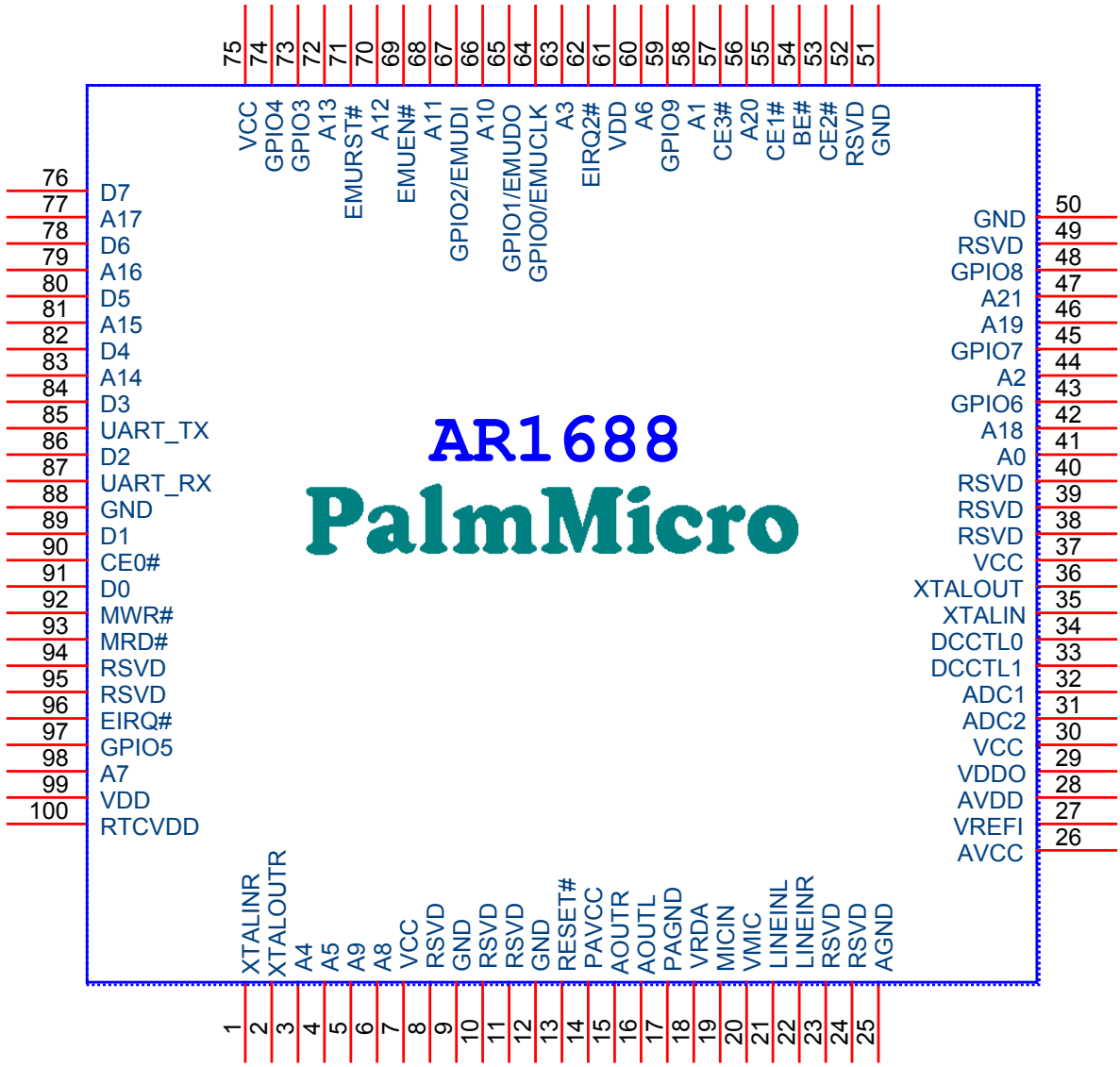
1. Features

- Integrated MCU, the instruction set is compatible with Z80
- MCU run at 24MHz(typical), F/W can program from DC up to 60MHz
- Internal 120 Kbytes RAM, no external SDRAM needed for most application
- Up to 4 chip selection for external SRAM, EEPROM or FLASH, each can support 2MB at maximum
- 24 bits DSP Core
- 2181-instruction-set compatible DSP co-processor
- DSP Speed up to 84MIPS
- Support 24MHz OSC with on-chip PLL for DSP
- Up to 10 general purpose I/O pins
- High quality 18bits CODEC on chip.
- One UART port
- Support real time clock
- Maximum voice output: 11mW@16 ohm
- Internal DC/DC converter to produce CORE voltage, eliminate external LDO
- Operating Voltage: IO: 3.3v, Core: 1.8v
- Low Power consumption: <90mW at typical
- LQFP-100(14x14mm) package

2. Pin Description

2.1. Pin configuration



2.2. Pin function, sorted by pin number

Pin Number	PinName	Type	Reset Value	Description
1	**XTALINR**	**AI**	**/**	**RTC crystal input**
2	**XTALOUTR**	**AO**	**/**	**RTC crystal output**
3	**A4**	**BI**	**Z**	**Bit4 of address bus**
4	**A5**	**BI**	**Z**	**Bit5 of address bus**
5	**A9**	**BI**	**Z**	**Bit9 of address bus**
6	**A8**	**BI**	**Z**	**Bit8 of address bus**
7	**VCC**	**PWR**	**/**	**Power input(3.3V)**
8	**RSVD**	**AO**	**/**	**Reserved, should be left open**
9	**GND**	**PWR**	**/**	**Ground**
10	**RSVD**	**A**	**H**	**Reserved, should be left open**
11	**RSVD**	**A**	**H**	**Reserved, should be left open**
12	**GND**	**/**	**L**	**Ground**
13	**RESET#**	**I**	**H**	**System reset input (active low)**
14	**PAVCC**	**PWR**	**/**	**Bypass capacitor for power amplifier**
15	**AOUTR**	**AO**	**/**	**Audio out right channel**
16	**AOUTL**	**AO**	**/**	**Audio out left channel**
17	**PAGND**	**PWR**	**/**	**Power amplifier ground**
18	**VRDA**	**AO**	**/**	**Bypass capacitor for CODEC Reference voltage**
19	**MICIN**	**AI**	**/**	**Microphone input**
20	**VMIC**	**PWR**	**/**	**Power supply for microphone**
21	**LINEINL**	**AI**	**/**	**Line Input Left Channel**
22	**LINEINR**	**AI**	**/**	**Line Input Right Channel**
23	**RSVD**	**AI**	**/**	**Reserved, should be left open**
24	**RSVD**	**AI**	**/**	**Reserved, should be left open**
25	**AGND**	**PWR**	**/**	**Analog ground**
26	**AVCC**	**PWR**	**/**	**Analog Power supply**
27	**VREFI**	**AI**	**/**	**Reference Voltage input**
28	**AVDD**	**PWR**	**/**	**Analog Core power pin**
29	**VDDO**	**PWR**	**/**	**Core power output**
30	**VCC**	**PWR**	**/**	**Power input(3.3V)**
31	**ADC2**	**AI**	**/**	**ADC2 input**
32	**ADC1**	**AI**	**/**	**ADC1 input**
33	**PWRM1**	**AI**	**/**	**Internal DC/DC Control1**

Pin Number	PinName	Type	Reset Value	Description
34	**PWRM0**	**AI**	**/**	**Internal DC/DC Control2**
35	**XTALIN**	**AI**	**/**	**System crystal input**
36	**XTALOUT**	**AO**	**/**	**System crystal output**
37	**VCC**	**PWR**	**/**	**Power input(3.3V)**
38	**RSVD**	**AI**	**/**	**Reserved, should be left open**
39	**RSVD**	**AI**	**/**	**Reserved, should be left open**
40	**RSVD**	**I**	**/**	**Reserved, should be left open**
41	**A0**	**BI**	**Z**	**Bit0 of address bus**
42	**A18**	**O**	**/**	**Bit18 of address bus**
43	**GPIO6**	**BI**	**Z**	**General purpose Input/Output6**
44	**A2**	**O**		**Bit2 of address bus**
45	**GPIO7**	**BI**	**/**	**General purpose Input/Output7**
46	**A19**	**O**		**Bit19 of address bus**
47	**A21**	**O**		**Bit21 of address bus**
48	**GPIO8**	**BI**	**Z**	**General purpose Input/Output8**
49	**RSVD**	**PWR**	**/**	**Reserved, should be left open**
50	**GND**	**PWR**	**/**	**Ground**
51	**GND**	**PWR**	**/**	**Ground**
52	**RSVD**	**PWR**	**/**	**Reserved, should be left open**
53	**CE2#**	**O**	**H**	**External memory chip enable 2**
54	**BE#**	**I**	**H**	**Boot Enable, Should be low for CE0# boot**
55	**CE1#**	**O**	**H**	**External memory chip enable 1**
56	**A20**	**O**		**Bit20 of address bus**
57	**CE3#**	**O**	**H**	**External memory chip enable 3**
58	**A1**	**O**		**Bit1 of address bus**
59	**GPIO9**	**BI**	**Z**	**General purpose Input/Output9**
60	**A6**	**O**		**Bit6 of address bus**
61	**VDD**	**PWR**	**/**	**Digital Core power**
62	**EIRQ2#**	**I**	**OD**	**External interrupt request input 2**
63	**A3**	**O**		**Bit3 of address bus**
64	**GPIO0**	**O**	**L**	**GPIO0/Emulation clock in**
65	**GPIO1**	**O**	**L**	**GPIO1/Emulation data out**
66	**A10**	**O**		**Bit10 of address bus**
67	**GPIO2**	**O**	**0**	**GPIO2/Emulation data in**
68	**A11**	**O**		**Bit11 of address bus**

Pin Number	PinName	Type	Reset Value	Description
69	**EMUEN#**	**I**	**/**	**Emulation enable(active low)**
70	**A12**	**O**		**Bit12 of address bus**
71	**EMURST#**	**I**	**/**	**Emulation reset(active low)**
72	**A13**	**O**		**Bit13 of address bus**
73	**GPIO3**	**BI**	**Z**	**General purpose Input/Output3**
74	**GPIO4**	**BI**	**Z**	**General purpose Input/Output4**
75	**VCC**	**PWR**	**/**	**Power input(3.3V)**
76	**D7**	**BI**	**L**	**Bit7 of external memory data bus**
77	**A17**	**O**		**Bit17 of address bus**
78	**D6**	**BI**	**L**	**Bit6 of external memory data bus**
79	**A16**	**O**		**Bit16 of address bus**
80	**D5**	**BI**	**L**	**Bit5 of external memory data bus**
81	**A15**	**O**		**Bit15 of address bus**
82	**D4**	**BI**	**L**	**Bit4 of external memory data bus**
83	**A14**	**O**		**Bit15 of address bus**
84	**D3**	**BI**	**L**	**Bit3 of external memory data bus**
85	**UART_TX**	**BI**	**Z**	**UART transmit data out**
86	**D2**	**BI**	**L**	**Bit2 of external memory data bus**
87	**UART_RX**	**BI**	**Z**	**UART receive data in**
88	**GND**	**PWR**	**/**	**Ground**
89	**D1**	**BI**	**L**	**Bit1 of external memory data bus**
90	**CE0#**	**O**		**External memory chip enable 0**
91	**D0**	**BI**	**L**	**Bit0 of external memory data bus**
92	**MWR#**	**O**	**H**	**Memory write strobe**
93	**MRD#**	**O**	**H**	**Memory read strobe**
94	**RSVD**	**O**	**L**	**Reserved, should be left open**
95	**RSVD**	**O**	**L**	**Reserved, should be left open**
96	**EIRQ#**	**BI**	**OD**	**External interrupt request input**
97	**GPIO5**	**BI**	**OD**	**General purpose Input/Output5**
98	**A7**	**O**		**Bit7 of address bus**
99	**VDD**	**PWR**	**/**	**Digital Core power**
100	**RTCVDD**	**PWR**	**/**	**RTC power pin**

2.3. Pin function, Sorted by function group

Pin Number	Pin Name	Type	Reset Value	Description
	CODEC pins			
14	PAVCC	PWR	/	Bypass capacitor for power amplifier
15	AOUTR	AO	/	Audio out right channel
16	AOUTL	AO	/	Audio out left channel
17	PAGND	PWR	/	Power amplifier ground
18	VRDA	AO	/	Bypass capacitor for CODEC Reference voltage
19	MICIN	AI	/	Microphone input
20	VMIC	PWR	/	Power supply for microphone
21	LINEINL	AI	/	Line Input Left Channel
22	LINEINR	AI	/	Line Input Right Channel
	External memory interface pins			
3	A4	BI	Z	Bit4 of address bus
4	A5	BI	Z	Bit5 of address bus
5	A9	BI	Z	Bit9 of address bus
6	A8	BI	Z	Bit8 of address bus
41	A0	BI	Z	Bit0 of address bus
42	A18	O	/	Bit18 of address bus
44	A2	O		Bit2 of address bus
46	A19	O		Bit19 of address bus
47	A21	O		Bit21 of address bus
53	CE2#	O	H	External memory chip enable 2
55	CE1#	O	H	External memory chip enable 1
56	A20	O		Bit20 of address bus
57	CE3#	O	H	External memory chip enable 3
58	A1	O		Bit1 of address bus
60	A6	O		Bit6 of address bus
63	A3	O		Bit3 of address bus
66	A10	O		Bit10 of address bus
68	A11	O		Bit11 of address bus
70	A12	O		Bit12 of address bus
72	A13	O		Bit13 of address bus
76	D7	BI	L	Bit7 of external memory data bus
77	A17	O		Bit17 of address bus

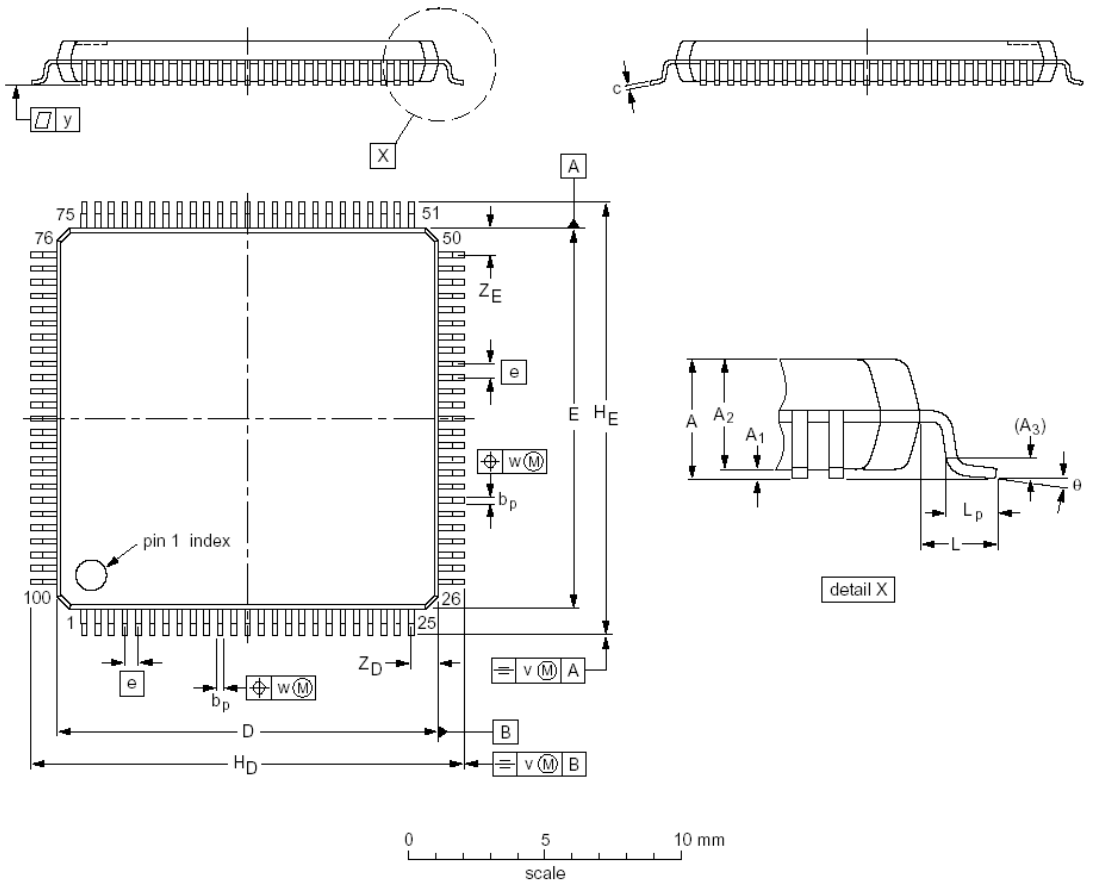
Pin Number	Pin Name	Type	Reset Value	Description
78	D6	BI	L	Bit6 of external memory data bus
79	A16	O		Bit16 of address bus
80	D5	BI	L	Bit5 of external memory data bus
81	A15	O		Bit15 of address bus
82	D4	BI	L	Bit4 of external memory data bus
83	A14	O		Bit15 of address bus
84	D3	BI	L	Bit3 of external memory data bus
86	D2	BI	L	Bit2 of external memory data bus
89	D1	BI	L	Bit1 of external memory data bus
90	CE0#	O		External memory chip enable 0
91	D0	BI	L	Bit0 of external memory data bus
92	MWR#	O	H	Memory write strobe
93	MRD#	O	H	Memory read strobe
98	A7	O		Bit7 of address bus
	GPIO pins			
43	GPIO6	BI	Z	General purpose Input/Output6
45	GPIO7	BI	/	General purpose Input/Output7
48	GPIO8	BI	Z	General purpose Input/Output8
59	GPIO9	BI	Z	General purpose Input/Output9
64	GPIO0	O	L	GPIO0/Emulation clock in
65	GPIO1	O	L	GPIO1/Emulation data out
67	GPIO2	O	0	GPIO2/Emulation data in
73	GPIO3	BI	Z	General purpose Input/Output3
74	GPIO4	BI	Z	General purpose Input/Output4
97	GPIO5	BI	OD	General purpose Input/Output5
	Miscellaneous pins			
1	XTALINR	AI	/	RTC crystal input
2	XTALOUTR	AO	/	RTC crystal output
13	RESET#	I	H	System reset input (active low)
27	VREFI	AI	/	Reference Voltage input
29	VDDO	PWR	/	Core power output
31	ADC2	AI	/	ADC2 input
32	ADC1	AI	/	ADC1 input
33	PWRM1	AI	/	Internal DC/DC Control1
34	PWRM0	AI	/	Internal DC/DC Control2
35	XTALIN	AI	/	System crystal input

Pin Number	Pin Name	Type	Reset Value	Description
36	XTALOUT	AO	/	System crystal output
54	BE#	I	H	Boot Enable, Should be low for CE0# boot
62	EIRQ2#	I	OD	External interrupt request input 2
69	EMUEN#	I	/	Emulation enable(active low)
71	EMURST#	I	/	Emulation reset(active low)
85	UART_TX	BI	Z	UART transmit data out
87	UART_RX	BI	Z	UART receive data in
96	EIRQ#	BI	OD	External interrupt request input
	Power and ground pins			
7	VCC	PWR	/	Power input(3.3V)
9	GND	PWR	/	Ground
12	GND	/	L	Ground
25	AGND	PWR	/	Analog ground
26	AVCC	PWR	/	Analog Power supply
28	AVDD	PWR	/	Analog Core power pin
30	VCC	PWR	/	Power input(3.3V)
37	VCC	PWR	/	Power input(3.3V)
50	GND	PWR	/	Ground
51	GND	PWR	/	Ground
61	VDD	PWR	/	Digital Core power
75	VCC	PWR	/	Power input(3.3V)
88	GND	PWR	/	Ground
99	VDD	PWR	/	Digital Core power
100	RTCVDD	PWR	/	RTC power pin
	Reserved pins			
8	RSVD	AO	/	Reserved, should be left open
10	RSVD	A	H	Reserved, should be left open
11	RSVD	A	H	Reserved, should be left open
23	RSVD	AI	/	Reserved, should be left open
24	RSVD	AI	/	Reserved, should be left open
38	RSVD	AI	/	Reserved, should be left open
39	RSVD	AI	/	Reserved, should be left open
40	RSVD	I	/	Reserved, should be left open
49	RSVD	PWR	/	Reserved, should be left open
52	RSVD	PWR	/	Reserved, should be left open
94	RSVD	O	L	Reserved, should be left open

Pin Number	Pin Name	Type	Reset Value	Description
95	**RSVD**	**O**	**L**	**Reserved, should be left open**

3. Package Outline:

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

LQFP-128: Plastics low profile quad flat package; 128leads, 14x14mm

ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.552 BASIC		
E	16.00 BASIC			0.630 BASIC		
E1	14.00 BASIC			0.552 BASIC		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.13	—	0.23	0.005	—	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
e	0.40 BSC.			0.016 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003