EM78F652N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.4

ELAN MICROELECTRONICS CORP.

December 2007

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Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.2	Changed the document format.	2006/08/01
1.3	1. Modified the General Description, Pin Assignment and Features sections. 2. Added green product information. 3. Modified the Functional Block Diagram. 4. Added Quality Assurance and Reliability 5. Modified the DC Electrical Characteristic 6. Adjusted the Internal RC Oscillator Mode from 16MHz to 12MHz 7. Modified the Operating Voltage.	2007/10/22
1.4	Modified the package type name	2007/12/27

1 General Description

The EM78F652N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology and high noise immunity. It has an on-chip 2K×13-bit Electrical Flash Memory and 256×8-bit in system programmable EEPROM. It provides three protection bits to prevent intrusion of user's Flash memory code. Twelve Code option bits are also available to meet user's requirements.

With its enhanced Flash-ROM feature, the EM78F652N provides a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 2K×13 bits Flash memory
  - 144×8 bits on chip registers (SRAM)
  - 256 bytes in-system programmable EEPROM
    *Endurance: 100,000 write/erase cycles
  - More than 10 years data retention
  - 8-level stacks for subroutine nesting
  - Less than 2 mA at 5V/4MHz
  - Typically 20 μA, at 3V/32kHz
  - Typically 2 μA, during sleep mode
- I/O port configuration
  - 3 bidirectional I/O ports
  - Wake-up port : P6
  - High sink port : P6
  - 12 Programmable pull-down I/O pins
  - 8 programmable pull-high I/O pins
  - 4 programmable open-drain I/O pins
  - External interrupt : P60
- Operating voltage range:
  - Operating voltage: 2.4V~5.5V at -40°C ~85°C (Industrial)
  - Operating voltage: 2.2V~5.5V ay 0°C ~70°C (Commercial)
- Operating frequency range (base on two clocks):
  - Crystal mode:
    DC ~ 16MHz @ 4.5V
    DC ~ 8MHz @ 3V
    DC ~ 4MHz @ 2.2V
  - ERC mode:
    DC ~ 16MHz @ 5V
    DC ~ 8MHz @ 3V
    DC ~ 4MHz @ 2.2V
  - IRC mode:
    DC ~ 12MHz @ 4.5V~5.5V
    DC ~ 4MHz @ 2.2V~5.5V
- Ten available interrupts:
  - Internal interrupt : 6
  - External interrupt : 4
- 4-channels Analog-to-Digital Converter with 12-bit resolution
- One set of 2 orders OP Amplifier
- One 16-bit Timer/Counter
  - TC2 : Timer/Counter/Window
- One 8-bit Timer/Counter
  - TC3 : Timer/Counter/PDO (programmable divider output)/PWM (pulse width modulation)
- Serial transmitter/receiver interface
  - Serial Peripheral Interface (SPI): Three-wire synchronous communication
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Power down (Sleep) mode
  - Four Crystal range in Oscillator Mode
    16MHz ~ 6MHz (HXT)
    6MHz ~ 1MHz (XT)
    1MHz ~ 100KHz (LXT1)
    32.768KHz (LXT2)
  - 4 programmable Level Voltage Detector (LVD)
    *Vdd power monitor and supports low voltage detector interrupt flag
  - Three security registers to prevent intrusion of Flash memory codes
  - One configuration register to accommodate user's requirements
  - 2/4/8/16 clocks per instruction cycle selected by code option
  - High EFT immunity
- Single instruction cycle commands
- Programmable free running watchdog timer
- Package type:
  - 16-pin DIP 300mil : EM78F652ND16J/S
  - 16-pin SOP 300mil : EM78F652NSO16J/S
  - 18-pin DIP 300mil : EM78F652ND18J/S
  - 18-pin SOP 300mil : EM78F652NSO18J/S
  - 20-pin DIP 300mil : EM78F652ND20J/S
  - 20-pin SOP 300mil : EM78F652NSO20J/S

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3 Pin Assignment

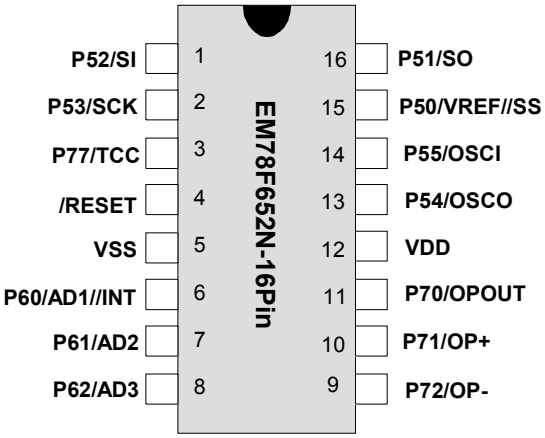


Figure 3-1 EM78F652ND16/SO16

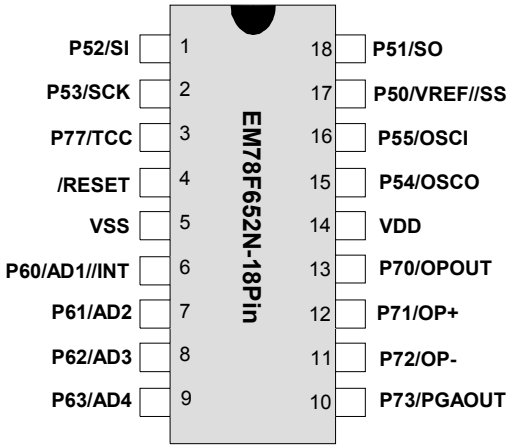


Figure 3-2 EM78F652ND18/SO18

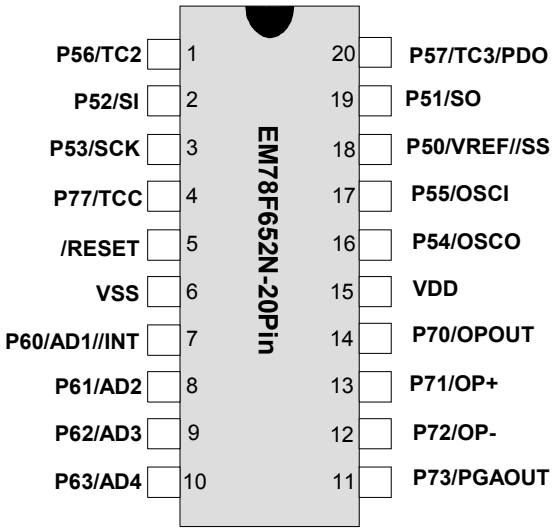


Figure 3-3 EM78F652ND20/SO20

4 Pin Description

4.1 EM78F652ND16/SO16

Symbol	Pin No.	Type	Function
OSCI	14	I	External clock crystal resonator RC oscillator input pin.
OSCO	13	I/O	Clock output from internal oscillator.
TCC	3	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	4	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset.
P50~P51 P52~P53 P54~P55	15, 16 1, 2 13, 14	I/O	Bidirectional 6-bit input/output pins P50~P53 can be used as pull-down pins. P50 can be used as external reference voltage for ADC P51 can be used as SPI serial data output. P52 can be used as SPI serial data input. P53 can be used as SPI serial clock input/output
P60~P62	6~8	I/O	Bidirectional 3-bit input/output ports. These can be pull-high, pull-down or can be open drain by software programming. These can also be used as 3-channel 12-bit resolution A/D converter. P60 can be used as external interrupt.
P70~P72 P77	11~9 3	I/O	P70 ~P72, P77 are bidirectional I/O ports. P70 can be used as OP Amplifier Output. P71 can be used as OP Amplifier non-inverting input. P72 can be used as OP Amplifier inverting input. P77 is an open drain I/O. P70~P72 can be used as pull-high or pull-down pins.
VDD	12	–	Power supply
VSS	5	–	Ground

4.2 EM78F652ND18/SO18

Symbol	Pin No.	Type	Function
OSCI	16	I	External clock crystal resonator RC oscillator input pin.
OSCO	15	I/O	Clock output from internal oscillator.
TCC	3	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	4	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset.
P50~P51 P52~P53 P54~P55	17, 18 1, 2 15, 16	I/O	Bidirectional 6-bit input/output pins P50~P53 can be used as pull-down pins. P50 can be used as external reference voltage for ADC P51 can be used as SPI serial data output. P52 can be used as SPI serial data input. P53 can be used as SPI serial clock input/output
P60~P63	6~9	I/O	Bidirectional 4-bit input/output ports. These can be pull-high, pull-down or can be open drain by software programming. These can also be used as 4-channel 12-bit resolution A/D converter. P60 can be used as external interrupt.
P70~P73 P77	13~10 3	I/O	P70 ~P73, P77 are bidirectional I/O ports. P70 can be used as OP Amplifier Output. P71 can be used as OP Amplifier non-inverting input. P72 can be used as OP Amplifier inverting input. P73 can be used as programmable gain amplifier output. P77 is an open drain I/O. P70~P73 can be used as pull-high or pull-down pins.
VDD	14	-	Power supply
VSS	5	-	Ground

4.3 EM78F652ND20/SO20

Symbol	Pin No.	Type	Function
OSCI	17	I	External clock crystal resonator RC oscillator input pin.
OSCO	16	I/O	Clock output from internal oscillator.
TCC	4	I	Real time clock/counter, Schmitt trigger input pin. Must be tied to VDD or VSS if not in use.
/RESET	5	I	Schmitt trigger input pin. If this pin remains at logic low, the controller is reset.
P50~P51 P52~P53 P54~P55 P56~P57	18, 19 2, 3 16, 17 1, 20	I/O	Bidirectional 8-bit input/output pins P50~P53 can be used as pull-down pins. P50 can be used as external reference voltage for ADC P51 can be used as SPI serial data output. P52 can be used as SPI serial data input. P53 can be used as SPI serial clock input/output P56 can be used as 16-bit timer/counter. P57 can be used as 8-bit timer/counter or programmable divider output (PDO).
P60~P63	7~10	I/O	Bidirectional 4-bit input/output ports. These can be pull-high, pull-down or can be open drain by software programming. These can also be used as 4-channel 12-bit resolution A/D converter. P60 can be used as external interrupt.
P70~P73 P77	14~11 4	I/O	P70 ~P73, P77 are bidirectional I/O ports. P70 can be used as OP Amplifier Output. P71 can be used as OP Amplifier non-inverting input. P72 can be used as OP Amplifier inverting input. P73 can be used as programmable gain amplifier output. P77 is an open drain I/O. P70~P73 can be used as pull-high or pull-down pins.
VDD	15	-	Power supply
VSS	6	-	Ground

5 Block Diagram

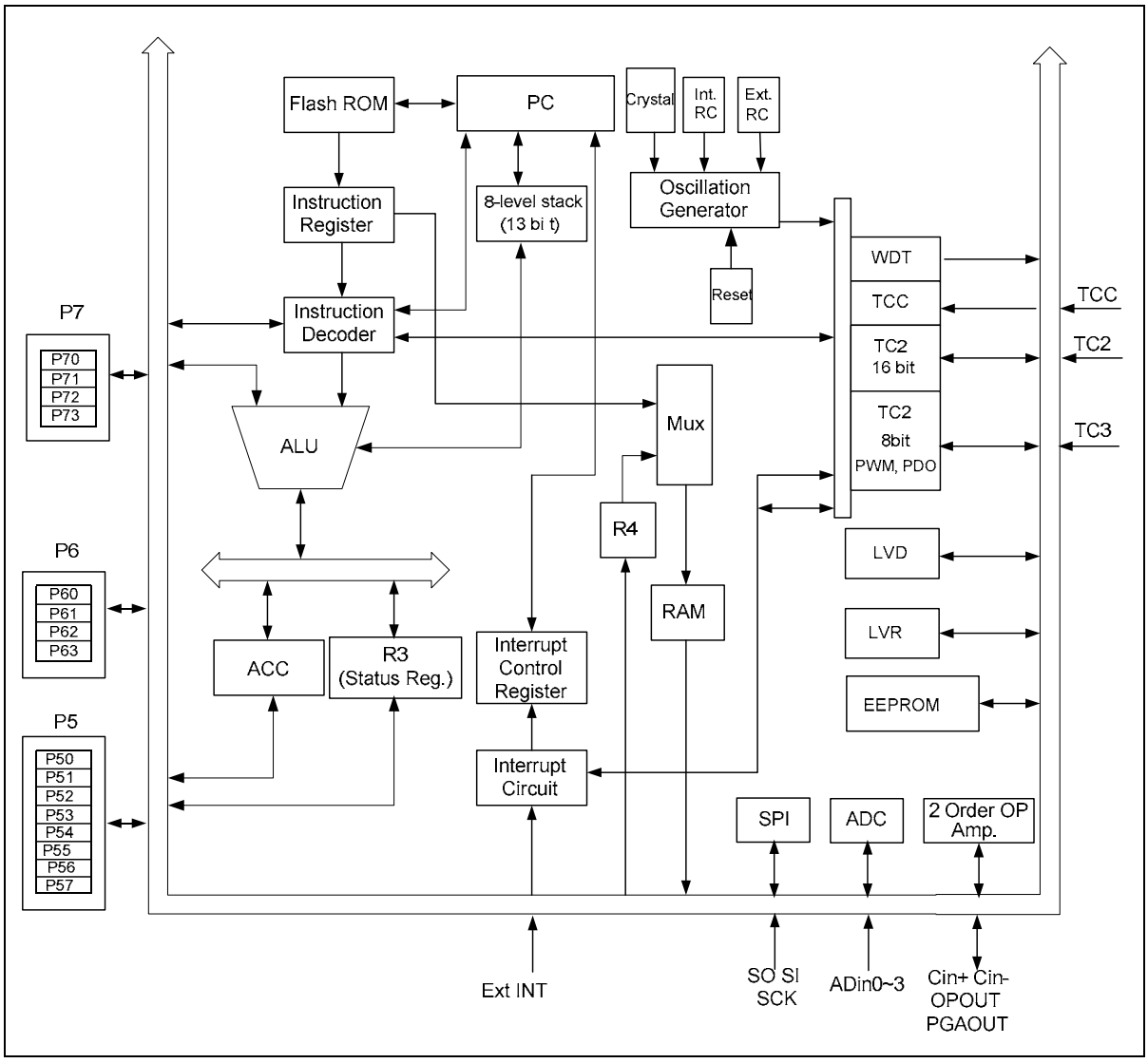


Figure 5 Functional Block Diagram

6 Function Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

R1 is incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC, if the PSTE bit (CONT-3) is reset. The content of the prescaler counter is cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter) and Stack

Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Figure 6-1.

The configuration structure generates 2K×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

R2 is set as all "0"s when under a reset condition.

"JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to go to any location within a page.

"CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top-level stack.

"ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

"MOV R2, A" allows to load an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits of the PC won't be changed.

Any instruction except "ADD R2,A" that is written to R2 (e.g. "MOV R2, A", "BC R2, 6") will cause the ninth bit and the tenth bit (A8~A9) of the PC to remain unchanged.

All instructions are single instruction cycle (fclk/2, fclk/4, fclk/8 or fclk/16) except for the instruction that would change the contents of R2. Such instruction will need one more instruction cycle.

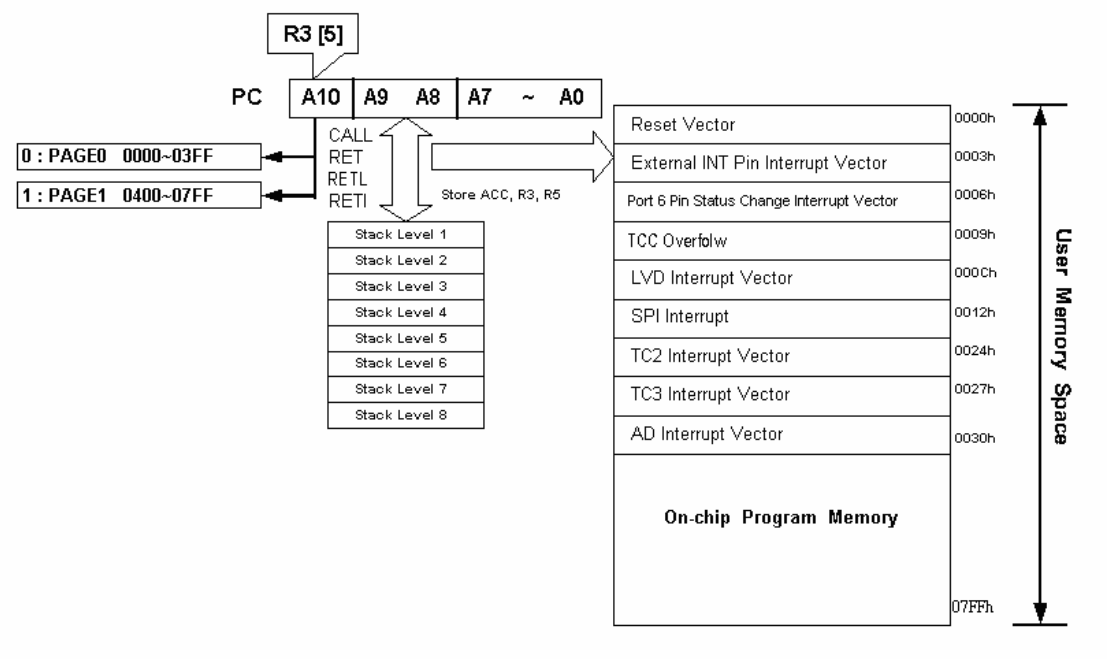


Figure 6-1 Program Counter Organization

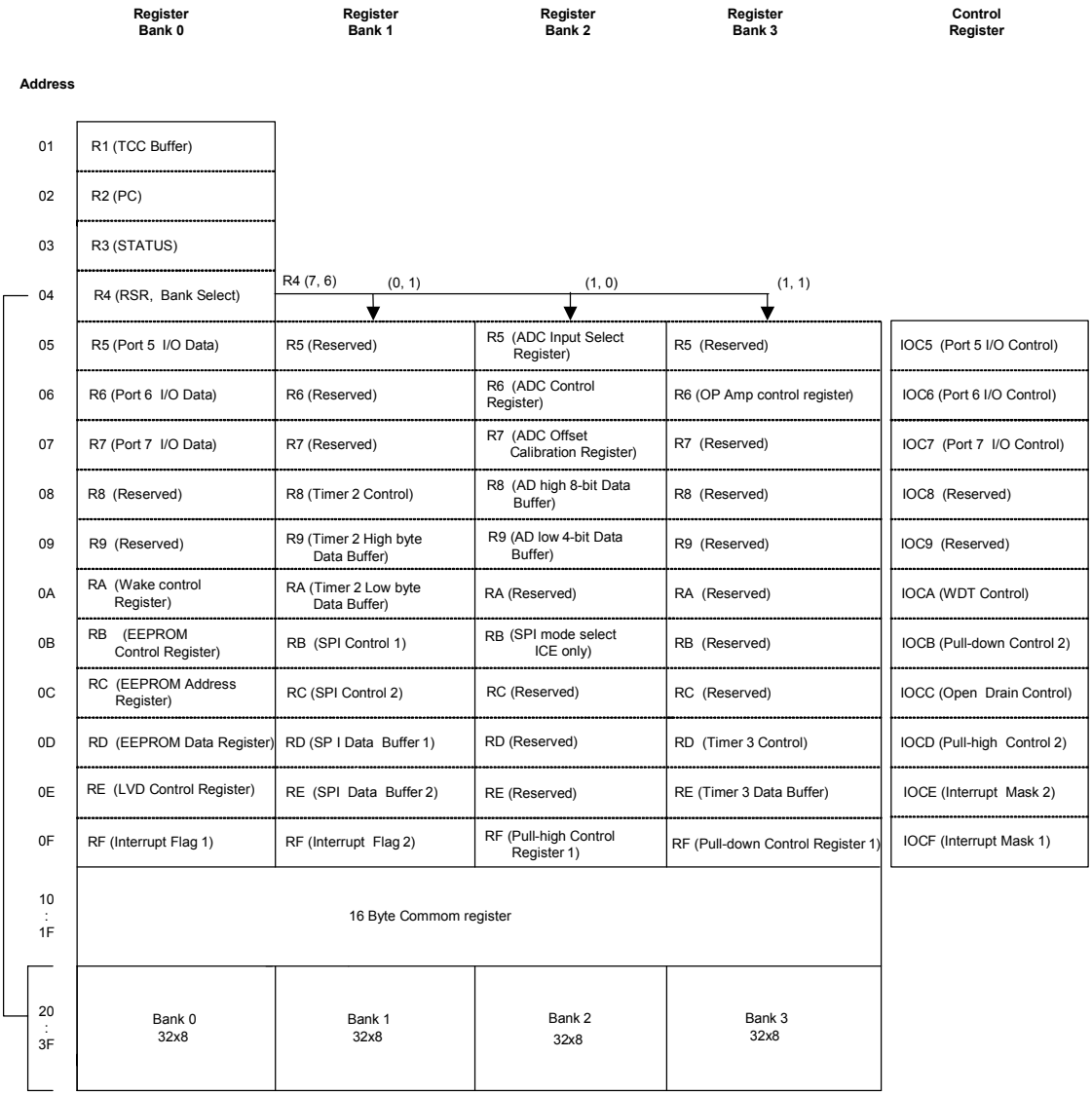


Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GP1	GP0	PS0	T	P	Z	DC	C

Bit 7 ~ Bit 6 (GP1 ~ GP0): General read/write bits

Bit 5 (PS0): Page select bit. PS0 is used to pre-select a program memory page. When executing a "JMP", "CALL", or other instructions which causes the program counter to change (e.g. MOV R2, A), PS0 is loaded into the 11th and 12th bits of the program counter and select one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS0 bit. That is, the return will always be to the page from where the subroutine was called, regardless of the PS0 bit current setting.

PS0	Program Memory Page [Address]
0	Page 0 [0000-03FF]
1	Page 1 [0400-07FF]

Bit 4 (T): Time-out bit

Set to 1 with the "SLEP" and "WDTC" commands, or during power up and reset to 0 by WDT time-out.

Bit 3 (P): Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Used to select Bank 0 ~ Bank 3

Bits 5~0: Used to select registers (Address: 00~3F) in indirect addressing mode.

See the data memory configuration in Figure 6-2.

6.1.6 Bank 0 R5 ~ R7 (Port 5 ~ Port 7)

R5 ~ R7 are I/O registers.

6.1.7 Bank 0 R8 ~ R9

These are reserved registers.

6.1.8 Bank 0 RA (Wake-up Control Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EM78F652N	-	ICWE	ADWE	-	-	-	-	-
ICE652	-	ICWE	ADWE	C4	C3	C2	C1	C0

Bit 7: Not used. Set all "0"

Bit 6 (ICWE): Port 6 input status change wake-up enable bit

0 : Disable Port 6 input status change wake-up

1 : Enable Port 6 input status change wake-up

Bit 5 (ADWE): ADC wake-up enable bit

0 : Disable ADC wake-up

1 : Enable ADC wake-up

When ADC Complete is used to enter the interrupt vector or to wake-up the EM78F652N from sleep with A/D conversion running, the ADWE bit must be set to "Enable".

Bits 4~0 (C4~C0): IRC calibration bits in IRC oscillator mode.

6.1.9 Bank 0 RB (EEPROM Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7 (RD): Read control register

0 : Does not execute EEPROM read

1 : Read EEPROM content, (RD can be set by software, RD is cleared by hardware after Read instruction is completed)

Bit 6 (WR): Write control register

0 : Write cycle to the EEPROM is complete.

1 : Initiate a write cycle, (WR can be set by software, WR is cleared by hardware after Write cycle is completed)

Bit 5 (EEWE): EEPROM Write Enable bit.

0 : Prohibit write to the EEPROM

1 : Allows EEPROM write cycles

Bit 4 (EEDF): EEPROM Detective Flag

0 : Write cycle is completed

1 : Write cycle is unfinished

Bit 3 (EEPC): EEPROM power-down control bit

0 : Switch off the EEPROM

1 : EEPROM is operating

Bits 2 ~ 0: Not used, set to "0" at all time

6.1.10 Bank 0 RC (256 Bytes EEPROM Address)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_A7	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 7 ~ 0: 256 bytes EEPROM address

6.1.11 Bank 0 RD (256 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 256 bytes EEPROM data

6.1.12 Bank 0 RE (LVD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	LVDEN	/LVD	LVD1	LVD0

Bits 7 ~ 4: Not used, set to “0” at all time

Bit 3 (LVDEN): Low Voltage Detect Enable Bit

0 : LVD disable

1 : LVD enable

Bit 2 (/LVD): Low Voltage Detector. This is a read only bit. When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0 : low voltage is detected

1 : low voltage is not detected or LVD function is disabled

Bit 1~Bit 0 (LVD1~LVD0): Low Voltage Detect level select bits

LVD1	LVD0	LVD Voltage Interrupt Level
0	0	2.3
0	1	3.3
1	0	4.0
1	1	4.5

6.1.13 Bank 0 RF (Interrupt Status Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIF	ADIF	SPIF	-	-	EXIF	ICIF	TCIF

Note: " 1 " means with interrupt request **" 0 "** means no interrupt occurs

Bit 7 (LVDIF): Low voltage Detector interrupt flag

When LVD1, LVD0 = "0, 0", Vdd > 2.3V, LVDIF is "0", Vdd ≤ 2.3V, set LVDIF to "1". LVDIF is reset to "0" by software.

When LVD1, LVD0 = "0, 1", Vdd > 3.3V, LVDIF is "0", Vdd ≤ 3.3V, set LVDIF to "1". LVDIF is reset to "0" by software.

When LVD1, LVD0 = "1, 0", Vdd > 4.0V, LVDIF is "0", Vdd ≤ 4.0V, set LVDIF to "1". LVDIF is reset to "0" by software.

When LVD1, LVD0 = "1, 1", Vdd > 4.5V, LVDIF is "0", Vdd ≤ 4.5V, set LVDIF to "1". LVDIF is reset to "0" by software.

Bit 6 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bit 5 (SPIF): SPI mode interrupt flag. Flag is cleared by software.

Bits 4 ~ 3: Not used. Set all to "0" at all time.

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

Note that the result of reading RF is the "logic AND" of RF and IOCF.

6.1.14 R10 ~ R3F

All of these are 8-bit general-purpose registers.

6.1.15 Bank 1 R5 ~R7

Reserved registers.

6.1.16 Bank 1 R8 TC2CR (Timer 2 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0

Bits 7~6: Not used, set to "0" at all time.

Bit 5 (TC2ES): TC2 signal edge

0 : increment if a transition from low to high (rising edge) takes place on the TC2 pin

1 : increment if a transition from high to low (falling edge) takes place on the TC2 pin

Bit 4 (TC2M): Timer/Counter 2 mode select

0 : Timer/counter mode

1 : Window mode

Bit 3 (TC2S): Timer/Counter 2 start control

0 : Stop and counter clear

1 : Start

Bit 2~Bit 0 (TC2CK2~TC2CK0): Timer/Counter 2 clock source select

TC2CK2	TC2CK1	TC2CK0	Clock Source	Resolution	Max. Time
			Normal	Fc=8M	Fc=8M
0	0	0	$Fc/2^{23}$	1.05 sec	19.1 hr
0	0	1	$Fc/2^{13}$	1.02 ms	1.1 min
0	1	0	$Fc/2^{8}$	32 μs	2.1 sec
0	1	1	$Fc/2^{3}$	1 μs	65.5 ms
1	0	0	Fc	125 ns	7.9 ms
1	0	1	–	–	–
1	1	0	–	–	–
1	1	1	External clock (TC2 pin)	–	–

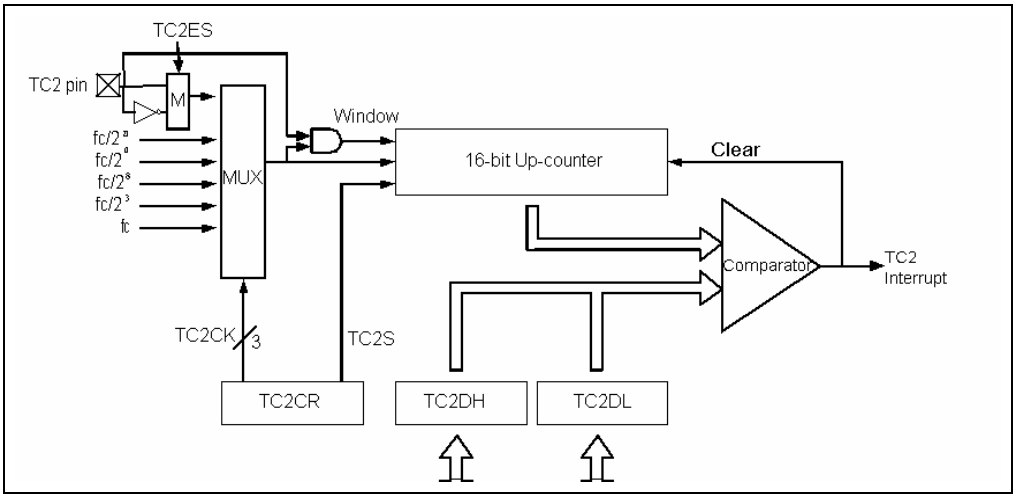


Figure 6-3 Configuration of Timer/Counter 2

In Timer mode, counting up is performed using the internal clock. When the contents of the up-counter matched with TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

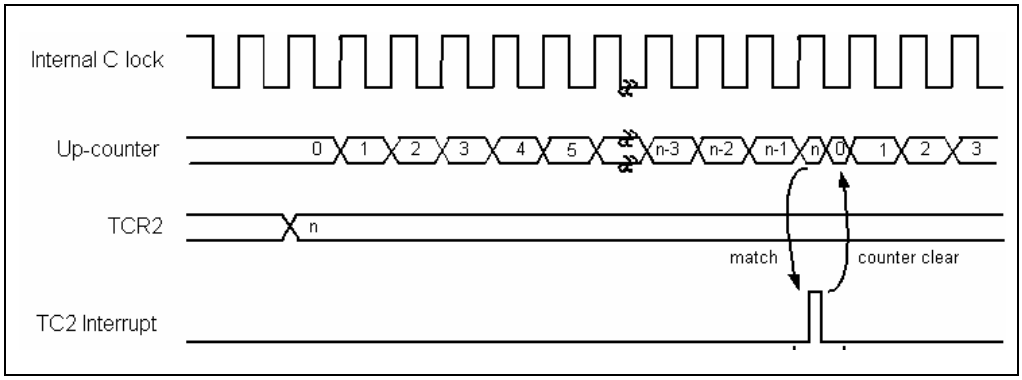


Figure 6-4 Timer Mode Timing Chart

In Counter mode, counting up is performed using the external clock input pin (TC2 pin) and either rising or falling can be selected by setting TC2ES. When the contents of the up-counter matched with TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

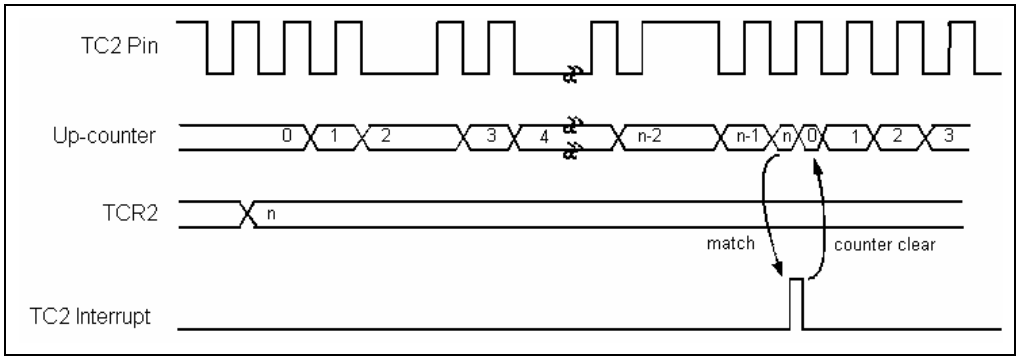


Figure 6-5 Counter Mode Timing Chart (INT2ES = 1)

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of up-counter matched with TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

Writing to the TCR2L, the comparison is inhibited until TCR2H is written.

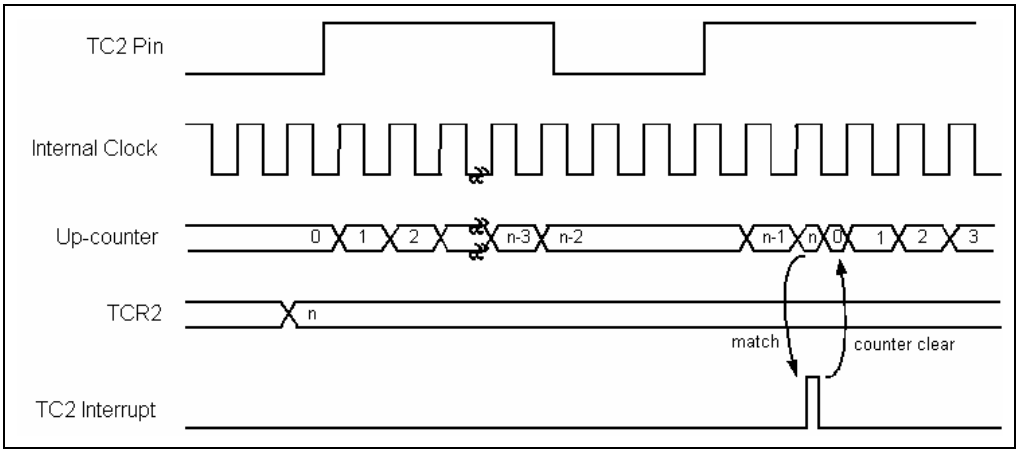


Figure 6-6 Window Mode Timing Chart

6.1.17 Bank 1 R9 TC2DH (Timer 2 High Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8

Bit 7 ~ Bit 0 (TC2D8 ~ TC2D15): High byte data buffer of 16-bit Timer/Counter 2.

6.1.18 Bank 1 RA TC2DL (Timer 2 Low Byte Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0

Bit 7 ~ Bit 0 (TC2D7 ~ TC2D0): Low byte data buffer of 16-bit Timer/Counter 2.

6.1.19 Bank 1 RB SPIS (SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	-	OD3	OD4	-	RBF

Bit 7 (DORD): Data transmission order

0 : Shift left (MSB first)

1 : Shift right (LSB first)

Bit 6~Bit 5 (TD1 ~ TD0): SDO Status output Delay times Options

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: Not used, set to “0” at all time.

Bit 3 (OD3): Open-drain Control bit

0 : Open-drain disable for SDO

1 : Open-drain enable for SDO

Bit 2 (OD4): Open-drain Control bit

0 : Open-drain disable for SCK

1 : Open-drain enable for SCK

Bit 1: Not used and set to “0” at all time

Bit 0 (RBF): Read Buffer Full flag

0 : Receiving not completed, and SPIRB has not fully exchanged

1 : Receiving completed; SPIRB is fully exchanged

6.1.20 Bank 1 RC SPIC (SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0

Bit 7 (CES): Clock Edge Select bit

0 : Data shifts out on rising edge, and shifts in on falling edge. Data is on hold during low-level.

1 : Data shifts out on falling edge, and shifts in on rising edge. Data is on hold during high-level.

Bit 6 (SPIE): SPI Enable bit

0 : Disable SPI mode

1 : Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0 : No overflow

1 : A new data is received while the previous data is still being held in the SPIB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, users are required to read the SPIRB register although only the transmission is implemented.

This can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0 : Reset as soon as the shifting is complete, and the next byte is ready to shift.

1 : Start to shift, and keep at "1" while the current byte is still being transmitted.

This bit will reset to 0 at every one-byte transmission by the hardware.

Bit 3 (SDOC): SDO output status control bit:

0 : After the Serial data output, the SDO remains high

1 : After the Serial data output, the SDO remains low

Bit 2~Bit 0 (SBRS 2 ~ SBRS0): SPI Baud Rate Select bits

SBRS2 (Bit 2)	SBRS1 (Bit 1)	SBRS0 (Bit 0)	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	F osc/4
0	1	0	Master	F osc/8
0	1	1	Master	F osc/16
1	0	0	Master	F osc/32
1	0	1	Master	F osc/64
1	1	0	Slave	/SS enable
1	1	1	Slave	/SS disable

6.1.21 Bank 1 RD SPIRB (SPI Read Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0

Bit 7 ~ Bit 0 (SPID7 ~ SPID0): SPI Read data buffer

6.1.22 Bank 1 RE SPIWB (SPI Write Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

Bit 7 ~ Bit 0 (SWB7 ~ SWB0): SPI Write data buffer

6.1.23 Bank 1 RF (Interrupt Status Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	TCIF3	TCIF2	-	-	-	-

Bits 7~6: Not used, set to ”0” at all time

Bit 5 (TCIF3): 8-bit Timer/Counter 4 interrupt flag. Interrupt flag is cleared by software.

Bit 4 (TCIF2): 16-bit Timer/Counter 2 interrupt flag. Interrupt flag is cleared by software.

Bits 3 ~ 0: Not used, set to “0” at all time.

6.1.24 Bank 2 R5 AISR (ADC Input Select Register)

The AISR register individually defines the Port 6 pins as analog input or as digital I/O.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	ADE3	ADE2	ADE1	ADE0

Bit 3 (ADE3): AD converter enable bit of P63 pin.

0 : Disable ADC3, P63 act as I/O pin

1 : Enable ADC3 act as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin.

0 : Disable ADC2, P62 act as I/O pin

1 : Enable ADC2 act as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

0 : Disable ADC1, P61 functions as I/O pin

1 : Enable ADC1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin

0 : Disable ADC0, P60 act as I/O pin

1 : Enable ADC0 act as analog input pin

The following table shows the priority of P60/ADC0//INT.

P60/ADC1//Int Pin Priority		
High	Medium	Low
/INT	ADC0	P60

6.1.25 Bank 2 R6 ADCON (A/D Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	-	ADIS1	ADIS0

Bit 7 (VREFS): The input source of the Vref of the ADC.

0 : Vref of the ADC is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1 : Vref of the ADC is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler of oscillator clock rate of ADC

00 = 1: 16 (default value)

01 = 1: 4

10 = 1: 64

11 = 1: WDT ring oscillator frequency

CKR1/CKR0	Operation Mode	Max. Operation Frequency
00	$F_{OSC}/16$	4 MHz
01	$F_{OSC}/4$	1 MHz
10	$F_{OSC}/64$	16 MHz
11	Internal RC	1 MHz

Bit 4 (ADRUN): ADC starts to run

0 : reset on completion of AD conversion. This bit cannot be reset by software

1 : A/D conversion is started. This bit can be set by software

Bit 3 (ADPD): ADC Power-down mode

0 : switch off the resistor reference to save power even while the CPU is operating

1 : ADC is operating

Bit 2: Not used, set to "0" at all time.

Bit 1~Bit 0 (ADIS1~ADIS0): Analog Input Select

00 = AN0/P60

01 = AN1/P61

10 = AN2/P62

11 = AN3/P63

The following table shows the priority of P50/VREF//SS pin. They can only be changed when the ADIF bit and the ADRUN bit are both low.

P50/VREF//SS Pin Priority		
High	Medium	Low
/SS	VREF	P50

6.1.26 Bank 2 R7 ADOC (A/D Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	-	-	-

Bit 7 (CALI): Calibration enable bit for A/D offset

0 : Calibration disable

1 : Calibration enable

Bit 6 (SIGN): Polarity bit of offset voltage

0 : Negative voltage

1 : Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

Bits 2 ~ 0: Not used, set to "0" at all time

6.1.27 Bank 2 R8 ADDH (AD High 8-Bits Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

When the A/D conversion is complete, the result of high 8-bit is loaded into the ADDH. The ADRUN bit is cleared, and the ADIF is set. R8 is read only.

6.1.28 Bank 2 R9 ADDL (AD Low 4-Bits Data Buffer)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	-	-	-	AD3	AD2	AD1	AD0

Bits 7 ~ 4: Not used, set to "0" at all time

Bit 3~Bit 0 (AD3~AD0): AD low 4-bit data buffer. R9 is read only.

6.1.29 Bank 2 RA, RC~RE

Reserved Registers

6.1.30 Bank 2 RB (only for ICE652)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	SBIM1	SBIM0	-	-	-	-

Bit 5 ~ Bit 4 (SBIM1 ~ SBIM0): Serial bus interface operating mode select.

SBIM1	SBIM0	Operating Mode
0	0	I/O mode
0	1	SPI mode

6.1.31 Bank 2 RF (Pull-high Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	/PH73	/PH72	/PH71	/PH70

Bits 7 ~ 4: Not used, set to "0" at all time.

Bit 3 (/PH73): Control bit used to enable the P73 pull-high pin

0 : Enable internal pull-high

1 : Disable internal pull-high

Bit 2 (/PH72): Control bit used to enable the P72 pull-high pin

Bit 1 (/PH71): Control bit used to enable the P71 pull-high pin

Bit 0 (/PH70): Control bit used to enable the P70 pull-high pin

The RF Register is both readable and writable.

6.1.32 Bank 3 R5

Reserved Register

6.1.33 Bank 3 R6 OPCON (OP Amplifier Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	PGAADEN	PGAO	POP	PPC	PG2	PG1	PG0

Bit 7: Not used, set to "0" at all time

Bit 6 (PGAADEN): this bit is used to enable if ADC is dedicated as PGA output

0 : ADC is not dedicated to PGA output

1 : ADC is dedicated to PGA output

PGAADEN	ADIS1	ADIS0	Analog Input Select
1	0	0	PGA connects to AN0/P60
1	0	1	PGA connects to AN1/P61
1	1	0	PGA connects to AN2/P62
1	1	1	PGA connects to AN3/P63

Bit 5 (PGAO): PGA output

0 : P73 functions as I/O pin

1 : P73 functions as PGA output

Bit 4 (POP): Power of OP Amplifier

0 : OP Amp disabled

1 : OP Amp enabled

Bit 3 (PPC): Power of PGA Control bit.

0 : PGA disabled

1 : PGA enabled

Bit 2 ~ Bit 0 (PG2 ~ PG0): Gain setting of PGA

PG2	PG1	PG0	Gain (v/v)
0	0	0	10
0	0	1	15
0	1	0	20
0	1	1	30
1	0	0	40
1	0	1	60
1	1	0	80
1	1	1	100

6.1.34 Bank 3 R7~RC

Reserved Registers

6.1.35 Bank 3 RD TC3CR (Timer 3 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bit 7 ~ Bit 6 (TC3FF1 ~ TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0 : Stop and clear the counter

1 : Start

Bit 4 ~ Bit 2 (TC3CK2 ~ TC3CK0): Timer/Counter 3 clock source select

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution	Max. Time
			Normal	Fc=8M	Fc=8M
0	0	0	$Fc/2^{11}$	250μs	64ms
0	0	1	$Fc/2^{7}$	16μs	4ms
0	1	0	$Fc/2^{5}$	4μs	1ms
0	1	1	$Fc/2^{3}$	1μs	255μs
1	0	0	$Fc/2^{2}$	500ns	127.5μs
1	0	1	$Fc/2^{1}$	250ns	63.8μs
1	1	0	Fc	125ns	31.9μs
1	1	1	External clock (TC3 pin)	-	-

Bit 1 ~ Bit 0 (TC3M1 ~ TC3M0): Timer/Counter 3 operating mode select

TC3M1	TC3M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider output
1	1	Pulse Width Modulation output

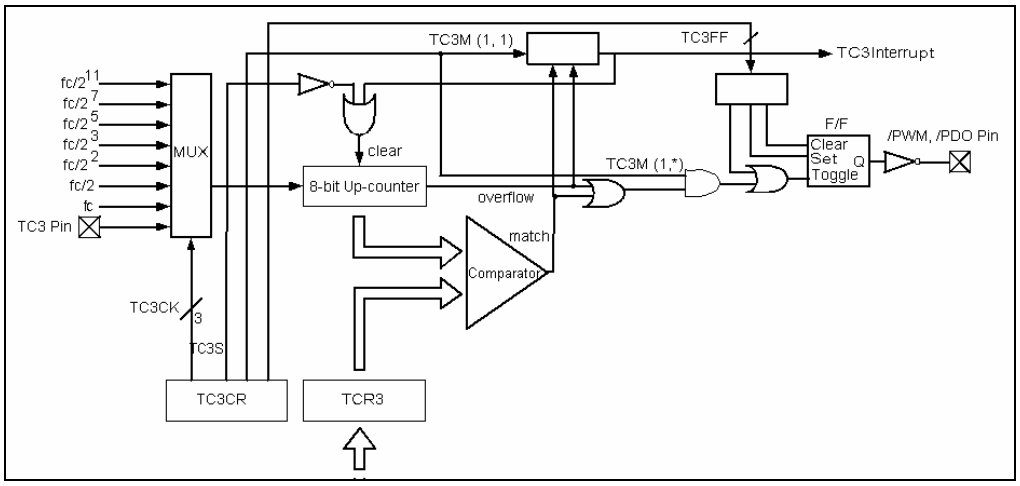


Figure 6-7 Timer/Counter 3 Configuration

In Timer mode, counting up is performed using internal clock (rising edge trigger). When the contents of the up-counter match with the contents of the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using external clock input pin (TC3 pin). When the contents of the up-counter match with the contents of the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. The F/F can be initialized by the program and it is initialized to “0” during reset. A TC3 interrupt is generated each time the /PDO output is toggled.

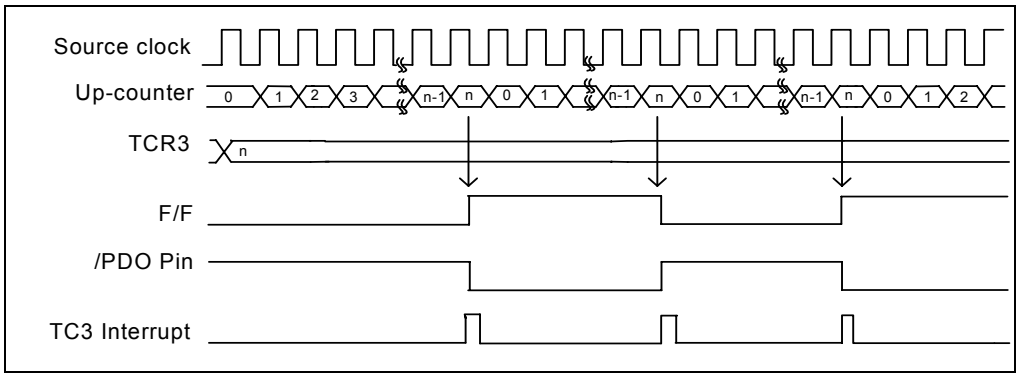


Figure 6-8 PDO Mode Timing Chart

In Pulse Width Modulation (PWM) Output mode, counting up is performed using internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. The counter continues counting, the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. TCR3 is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten. Therefore, the output can be changed continuously. Also, the first time, TRC3 is shifted by setting TC3S to "1" after data is loaded to TCR3.

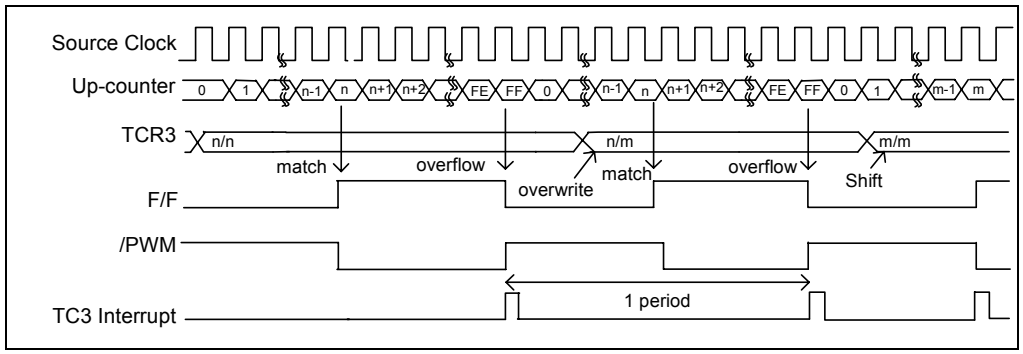


Figure 6-9 PWM Mode Timing Chart

6.1.36 Bank 3 RE TC3D (Timer 3 Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0

Bit 7 ~ Bit 0 (TC3D7 ~ TC3D0): Data Buffer of 8-bit Timer/Counter 3

6.1.37 Bank 3 RF (Pull-down Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	/PD73	/PD72	/PD71	/PD70

Bit 7~ Bit 4: Not used, set to "0" at all time

Bit 3 (/PD73): Control bit used to enable the P73 pull-down pin

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 2 (/PD72): Control bit used to enable the P72 pull-down pin

Bit 1 (/PD71): Control bit used to enable the P71 pull-down pin

Bit 0 (/PD70): Control bit used to enable the P70 pull-down pin

The RF Register is both readable and writable.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	/INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0 = interrupt occurs at the rising edge of the INT pin

1 = interrupt occurs at the falling edge of the INT pin

Bit 6 (/INT): Interrupt enable flag

0 : masked by DISI or hardware interrupt

1 : enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0 : internal instruction cycle clock

1 : transition on the TCC pin

Bit 4 (TE): TCC signal edge

0 : increment if a transition from low to high takes place on the TCC pin

1 : increment if a transition from high to low takes place on the TCC pin

Bit 3 (PSTE): Prescaler enable bit for TCC

0 : prescaler disable bit, TCC rate is 1:1

1 : prescaler enable bit, TCC rate is set as Bit 2~Bit 0

Bit 2 ~ Bit 0 (PST 2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

CONT register is both readable and writable.

6.2.3 IOC5 ~ IOC7 (I/O Port Control Register)

A value of "1" sets the relative I/O pin into high impedance, while "0" defines the relative I/O pin as output.

IOC5, IOC6 and IOC7 registers are both readable and writable.

6.2.4 IOC8~IOC9

Reserved registers

6.2.5 IOCA (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0

Bit 7 (WDTE): Control bit used to enable the Watchdog timer

0 : Disable WDT

1 : Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS): Control bit used to define the function of P60 (/INT) pin

0 : P60, bidirectional I/O pin

1 : /INT, external interrupt pin. In this case, the I/O control bit of P60 (Bit 0 of IOC6) must be set to "1".

When EIS is "0", the path of /INT is masked. When EIS is "1", the status of /INT pin can also be read by way of reading Port 6 (R6).

EIS is both readable and writable.

Bits 5~4: Not used, set to “0” at all time

Bit 3 (PSWE): Prescaler enable bit for WDT

0 : prescaler disable bit, WDT rate is 1:1

1 : prescaler enable bit, WDT rate is set as Bit 0~Bit 2

Bit 2 ~ Bit 0 (PSW2 ~ PSW0): WDT prescaler bits

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.2.6 IOCB (Pull-down Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0

Bit 7 (/PD7): Control bit used to enable the of P63 pull-down pin

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 6 (/PD6): Control bit used to enable the P62 pull-down pin

Bit 5 (/PD5): Control bit used to enable the P61 pull-down pin

Bit 4 (/PD4): Control bit used to enable the P60 pull-down pin

Bit 3 (/PD3): Control bit used to enable the P53 pull-down pin

Bit 2 (/PD2): Control bit used to enable the P52 pull-down pin

Bit 1 (/PD1): Control bit used to enable the P51 pull-down pin

Bit 0 (/PD0): Control bit used to enable the P50 pull-down pin

The IOCB Register is both readable and writable.

6.2.7 IOCC (Open-drain Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	OD3	OD2	OD1	OD0

Bits 7 ~ 4: Not used, set to “0” at all time

Bit 3 (OD3): Control bit used to enable the open-drain output of the P63 pin

0 : Disable open-drain output

1 : Enable open-drain output

Bit 2 (OD2): Control bit used to enable the open-drain output of the P62 pin

Bit 1 (OD1): Control bit used to enable the open-drain output of the P61 pin

Bit 0 (OD0): Control bit used to enable the open-drain output of the P60 pin

The IOCC Register is both readable and writable.

6.2.8 IOCD (Pull-high Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	–	/PH3	/PH2	/PH1	/PH0

Bits 7~4: Not used, set to "0" at all time

Bit 3 (/PH3): Control bit used to enable the P63 pull-high pin.

0 : Enable internal pull-high

1 : Disable internal pull-high

Bit 2 (/PH2): Control bit used to enable the P62 pull-high pin

Bit 1 (/PH1): Control bit used to enable the P61 pull-high pin

Bit 0 (/PH0): Control bit used to enable the P60 pull-high pin

The IOCD Register is both readable and writable.

6.2.9 IOCE (Interrupt Mask Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	TCIE3	TCIE2	–	–	–	–

Bits 7 ~ 6: Not used, set to "0" at all time

Bit 5 (TCIE3): Interrupt enable bit

0 : Disable TCIF3 interrupt

1 : Enable TCIF3 interrupt

Bit 4 (TCIE2): Interrupt enable bit

0 : Disable TCIF2 interrupt

1 : Enable TCIF2 interrupt

Bits 3 ~ 0: Not used, set to "0" at all time

6.2.10 IOCF (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDIE	ADIE	SPIE	-	-	EXIE	ICIE	TCIE

Bit 7 (LVDIE): LVDIF interrupt enable bit

0 : Disable LVDIF interrupt

1 : Enable LVDIF interrupt

Bit 6 (ADIE): ADIF interrupt enable bit

0 : Disable ADIF interrupt

1 : Enable ADIF interrupt

When the ADC Complete is used to enter interrupt vector or enter next instruction, the ADIE bit must be set to "Enable".

Bit 5 (SPIE): Interrupt enable bit.

0 : Disable SPIF interrupt

1 : Enable SPIF interrupt

Bits 4~3: Not used, set to “0” at all time

Bit 2 (EXIE): EXIF interrupt enable bit

0 : Disable EXIF interrupt

1 : Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0 : Disable ICIF interrupt

1 : Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0 : Disable TCIF interrupt

1 : Enable TCIF interrupt

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. The IOCF register is both readable and writable.

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the CONT register are used to determine the ratio of the prescaler of TCC. Likewise, the PSW0~PSW2 bits of the IOCE0 register are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the “WDTC” and “SLEP” instructions. Figure 6-10 depicts the circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be internal clock or external signal input (edge selectable from the TCC pin). If TCC signal source is from the internal clock, TCC will be incremented by 1 at every instruction cycle (without prescaler). As illustrated in Figure 6-10, selection of CLK=Fosc/2, CLK=Fosc/4, CLK=Fosc/8 or CLK=Fosc/16 depends on the Code Option bit <CLKS1, CLKS0>.

If TCC signal source is from external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept in high or low level) must be greater than 1CLK. The TCC will stop running when sleep mode occurs.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode or by software programming. Refer to WDTE bit of IOCE0 register. With no prescaler, the WDT time-out period is approximately 18 ms[1] (one oscillator start-up timer period).

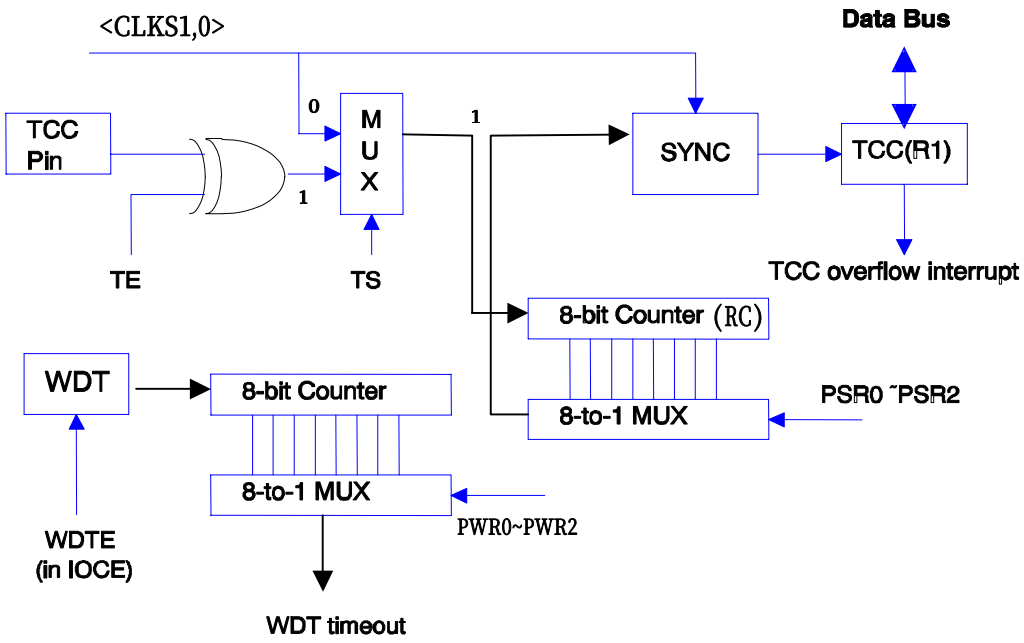


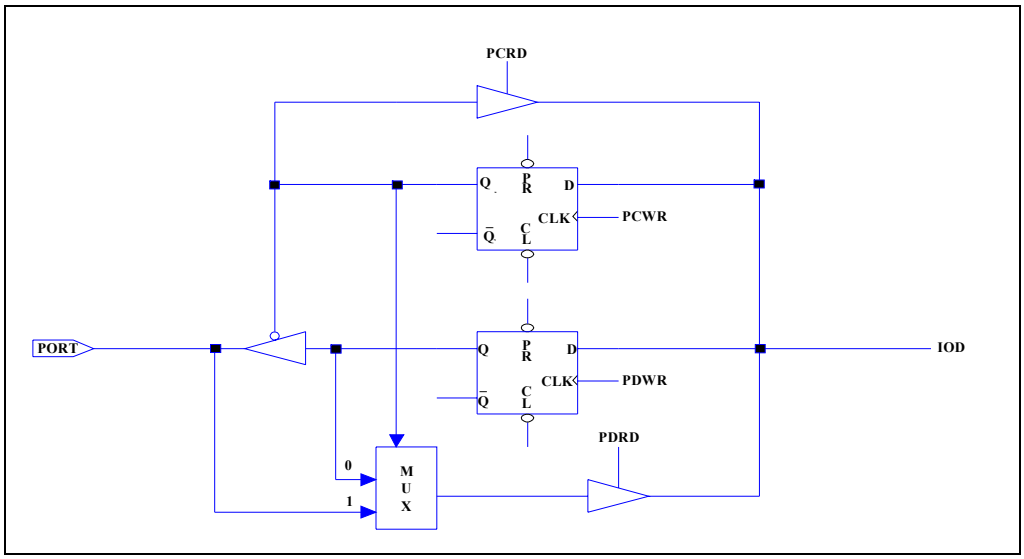
Figure 6-10 Block Diagram of TCC and WDT

[1] **Note:** VDD=5V, WDT time-out period = 16.5ms ± 8% VDD=3V
WDT time-out period = 18ms ± 8%.

6.4 I/O Ports

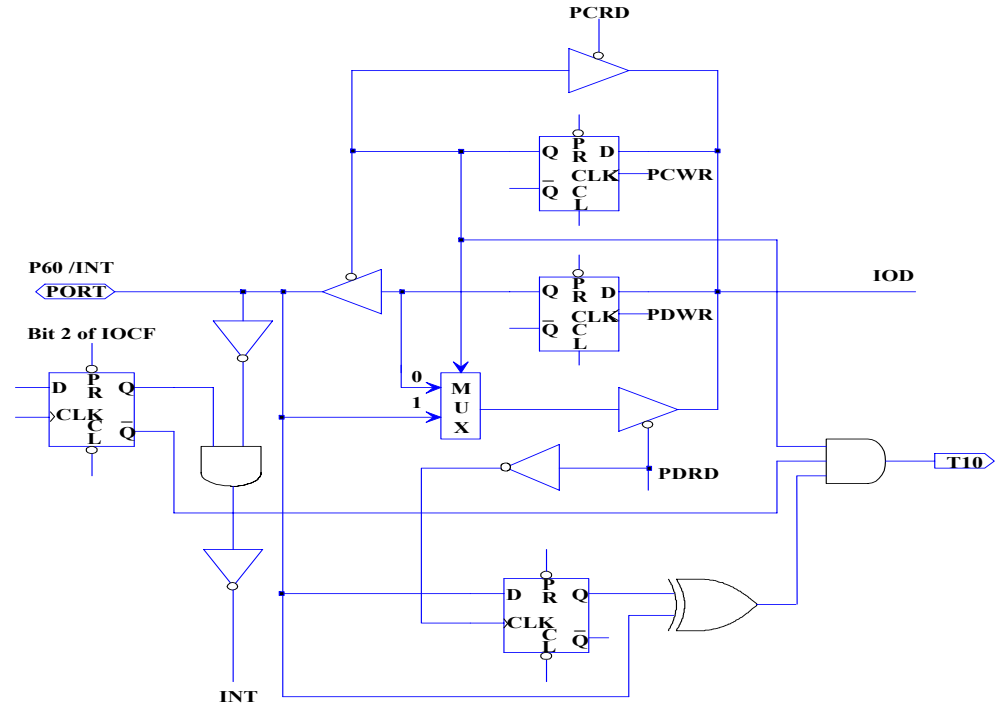
The I/O registers, Ports 5, 6 and 7, are bidirectional tri-state I/O ports. Port 6 / 7 can be pulled high internally by software. In addition, Port 6 can also have open-drain output by software. Input status change interrupt (or wake-up) function on Port 6 P50 ~ P53 and P60 ~ P63 and Port 7 pins can be pulled down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC7).

The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6 and Port 7 are shown in the following Figures 6-11, 6-12 (a), 6-12 (b), and Figure 6-13.



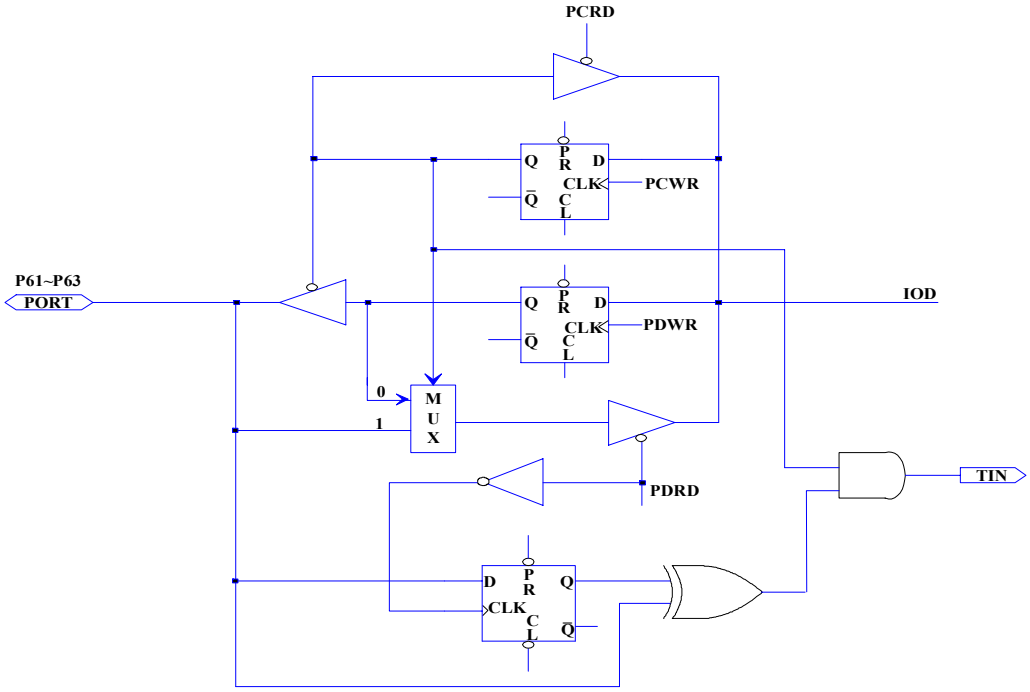
Note: Pull-down is not shown in the figure.

Figure 6-11 I/O Port and I/O Control Register Circuit for Ports 5, 6, 7



Note: Pull-high (down) and **Note:** Open-drain are not shown in the figure.

Figure 6-12 (a) I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: Pull-high (down) and Open-drain are not shown in the figure.

Figure 6-12 (b) I/O Port and I/O Control Register Circuit for P61~P63, P70~P73

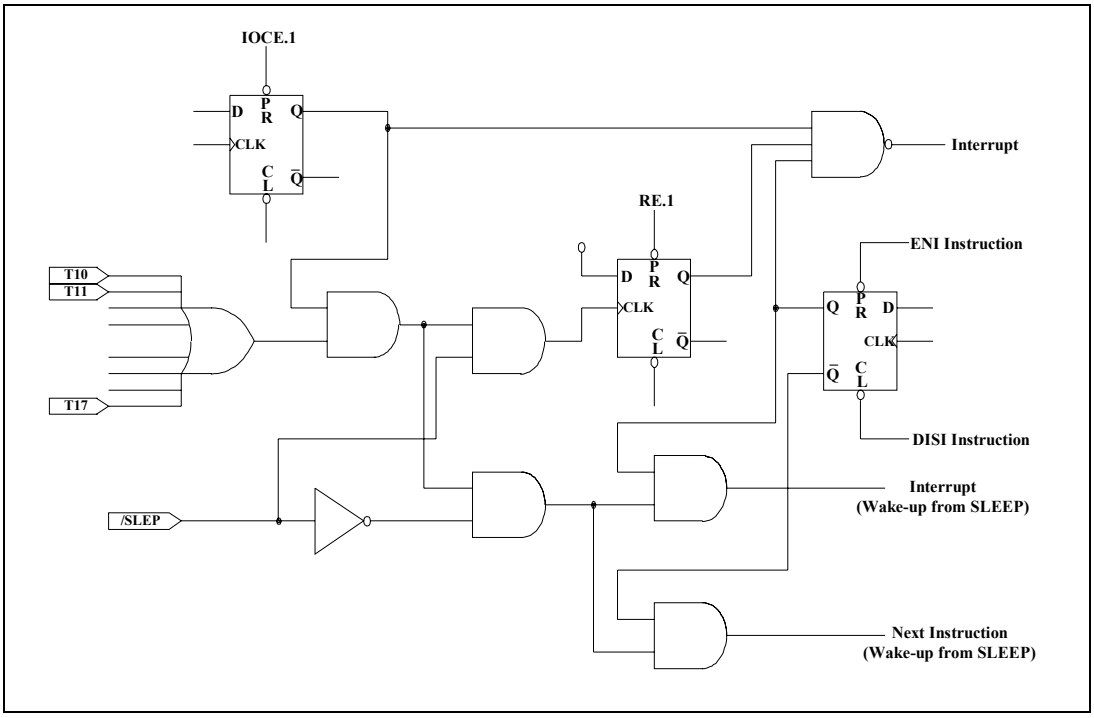


Figure 6-13 Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up

Table 6 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before Sleep 1. Disable WDT[2] (use this very carefully) 2. Read I/O Port 6 (MOV R6,R6) 3 a. Enable interrupt (Set IOCF.1), after wake-up if “ENI” switch to interrupt vector (006H), if “DISI” excute next instruction 3 b. Disable interrupt (Set IOCF.1), always execute next instruction 4. Enable wake-up enable bit (Set RA.6) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (006H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt vector (006H)

[2] **Note:** Software disables WDT (watchdog timer) but hardware must be enabled before applying Port 6 Change Wake-up function. (Code Option Register and Bit 6 (ENWDTB) are set to “1”).

6.5 Reset and Wake-up

6.5.1 Reset

A reset is initiated by one of the following events:

(1) Power-on reset

(2) /RESET pin input "low"

(3) WDT time-out (if enabled)

The device is kept in a reset condition for a period of approx. 18ms[3] (one oscillator start-up timer period) after the reset is detected. The oscillator is running, or will be started.

- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper three bits of R3 are cleared.
- The bits of the RB, RC, RD, RD, RE registers are set to their previous status.
- The bits of the CONT register are set to all "0" except for Bit 6 (INT flag).
- The bits of the Pull-high, Pull-down and LVD registers are set to all "1".
- Bank 0 RF, Bank 1 RF, IOCE and IOCF registers are cleared.

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering sleep mode, WDT (if enabled) is cleared but keeps on running. After a wake-up, in RC mode the wake-up time is 34 clocks. High crystal mode wake-up time is 2 ms and 32 clocks. In low Crystal 2 mode, wake-up time is 500 ms.

[3] **Note:** Vdd = 5V, set up time period = 16.8ms ± 8%
Vdd = 3V, set up time period = 18ms ± 8%

The controller can be awakened by:

(1) External reset input on /RESET pin

(2) WDT time-out (if enabled)

(3) Port 6 input status changes (if enabled)

(4) A/D conversion completed (if ADWE is enabled)

The first two cases will cause the EM78F652N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, and 5 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) determines whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from address 0x6, 0xF or 0X15, 0X30 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction right next to SLEP after wake-up. All throughout the sleep mode, wake up time is150μs, no matter what oscillation mode (except low Crystal mode). In low Crystal 2 mode, wake up time is 500ms.

One or more of Cases 2 to 5 can be enabled before entering into sleep mode. That is,

[a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78F652N can be awakened only by Case 1 or 2. Refer to the Interrupt section for further details.

[b] If Port 6 Input Status Change is used to wake up the EM78F652N and the ICWE bit of the RA register is enabled before SLEP, WDT must be disabled. Hence, the EM78F652N can be awakened only by Case 3.

[c] If AD conversion completed is used to wake-up EM78F652N and ADWE bit of RA register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM78F652N can be awakened only by Case 5.

If Port 6 Input Status Change Interrupt is used to wake-up the EM78F652N, (as in Case [a] above), the following instructions must be executed before SLEP:

```
BC              R3, 7           ; Select Segment 0
MOV             A, @001110xxb   ; Select WDT prescaler and
                                ; Disable the WDT
IOW             IOCA
WDTC                            ; Clear WDT and prescaler
MOV             R6, R6          ; Read Port 6
ENI (or DISI)                   ; Enable (or disable) global
                                ; interrupt
MOV             A, @010xxxxxb   ; Enable Port 6 input change
                                ; wake-up bit
MOV             RA,A
MOV             A, @00000x1xb   ; Enable Port 6 input change
                                ; interrupt
IOW             IOCF
SLEP                            ; Sleep
```

Similarly, if the Comparator 1 Interrupt is used to wake up the EM78F652N (as in Case [c] above), the following instructions must be executed before SLEP:

```
BS              R4, 7           ; Select Bank 3
BS              R4, 6
MOV             A, @x10xxxxxb   ; Select a comparator and P70
                                ; act as CO pin
MOV             R7,A
MOV             A, @001110xxb   ; Select WDT prescaler and
                                ; Disable the WDT
IOW             IOCA
WDTC                            ; Clear WDT and prescaler
ENI (or DISI)                   ; Enable (or disable) global
                                ; interrupt
MOV             A, @100xxxxxb   ; Enable comparator output status
                                ; change wake-up bit
MOV             RA,A
MOV             A, @10000000b   ; Enable comparator output status
                                ; change interrupt
IOW             IOCE
SLEP                            ; Sleep
```

All kinds of wake-up mode and interrupt mode are shown below:

Signal	Sleep Mode	Normal Mode
TCC Over Flow	X	DISI + IOCF (TCIE) Bit 0 = 1
		Next Instruction+ Set RF (TCIF) = 1
		ENI + IOCF0 (TCIE) Bit 0 = 1
		Interrupt Vector (0x09)+ Set RF (TCIF) = 1
Port 6 Input Status Change	RA (ICWE) Bit 6 = 0, IOCF (ICIE) Bit 1 = 0	IOCF0 (ICIE) Bit 1=0
	Oscillator, TCC and TIMERX are stopped. Port 6 input status changed wake-up is invalid.	Port 6 input status change interrupt is invalid
	RA (ICWE) Bit 6 = 0 (IOCFICIE) Bit 1 = 1	
	Set RF (ICIF) = 1, Oscillator, TCC and TIMERX are stopped. Port 6 input status changed wake-up is invalid.	
	RA (ICWE) Bit 6 = 1, IOCF (ICIE) Bit 1 = 0	
	Wake-up+ Next Instruction Oscillator, TCC and TIMERX are stopped.	
	RA (ICWE) Bit 6 = 1, DISI + IOCF (ICIE) Bit 1 = 1	DISI + IOCF (ICIE) Bit 1 = 1
	Wake-up+ Next Instruction+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	Next Instruction+ Set RF (ICIF) = 1
	RA (ICWE) Bit 6 = 1, ENI + IOCF (ICIE) Bit 1 = 1	ENI + IOCF0 (ICIE) Bit 1 = 1
	Wake-up+ Interrupt Vector (0x06)+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	Interrupt Vector (0x06)+ Set RF (ICIF) = 1

Signal	Sleep Mode	Normal Mode
INT Pin	X	DISI + IOCF (EXIE) Bit 2 = 1
		Next Instruction+ Set RF (EXIF) = 1
		ENI + IOCF (EXIE) Bit 2=1
		Interrupt Vector (0x03)+ Set RF (EXIF) = 1
AD Conversion	RA (ADWE) Bit 5 = 0, IOCF (ADIE) Bit 6 = 0	IOCF (ADIE) Bit 6 = 0
	Clear R6 (Bank 2) (ADRUN)=0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	AD conversion interrupt is invalid
	RA (ADWE) Bit 5 = 0, IOCF0 (ADIE) Bit 6 = 1	
	Set RF (ADIF) = 1, R6 (Bank 2) (ADRUN) = 0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	
	RA (ADWE) Bit 5=1, IOCF0 (ADIE) Bit 6=0	
	Wake-up+ Next Instruction, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC is completed.	
	RA (ADWE) Bit 5 = 1, DISI + IOCF0 (ADIE) Bit 6 = 1	DISI + IOCF (ADIE) Bit 6 = 1
	Wake-up+ Next Instruction+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	Next Instruction+ RF (ADIF) = 1
	RA (ADWE) Bit 5 = 1, ENI + IOCF0 (ADIE) Bit 6 = 1	ENI + IOCF0 (ADIE) Bit 6 = 1
	Wake-up+ Interrupt Vector (0x30)+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	Interrupt Vector (0x30)+ Set RF (ADIF) = 1
WDT Time Out IOCE (WDTE) Bit 7 = 1	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)

Table 7. Summary of Registers Initialized Values

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	–	–	–	–	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	C77	–	–	–	C73	C72	C71	C70
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	/INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x01	R1 (TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x02	R2 (PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	**0/P	**0/P	**0/P	**0/P	**1/P	**0/P	**0/P	**0/P
0x03	R3 (SR)	Bit Name	GP1	GP0	PS0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET and WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin Change	P	P	P	t	t	P	P	P
0x04	R4 (RSR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	P5 (Bank 0)	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	P6 (Bank 0)	Bit Name	×	×	×	×	P63	P62	P61	P60
		Power-on	–	–	–	–	1	1	1	1
		/RESET and WDT	–	–	–	–	1	1	1	1
		Wake-up from Pin Change	–	–	–	–	P	P	P	P
0x07	P7 (Bank 0)	Bit Name	P77	×	×	×	P73	P72	P71	P70
		Power-on	U	–	–	–	U	U	U	U
		/RESET and WDT	P	–	–	–	P	P	P	P
		Wake-up from Pin Change	P	–	–	–	P	P	P	P
0x0A	RA (Bank 0)	Bit Name	–	ICWE	ADWE	–	–	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0X0B	RB (ECR) (Bank 0)	Bit Name	RD	WR	EEWE	EEDF	EEPC	–	–	–
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	0	0
0X0C	RC (Bank 0)	Bit Name	EE_A7	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	P	P	P	P	P	P	P
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0X0D	RD (Bank 0)	Bit Name	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0E	RE (Bank 0)	Bit Name	–	–	–	–	LVDEN	/LVD	LVD1	LVD0
		Power-on	0	0	0	0	0	1	0	0
		/RESET and WDT	0	0	0	0	0	1	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x0F	RF (ISR) (Bank 0)	Bit Name	LVDIF	ADIF	SPIF	–	–	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	0	0	P	P	P
0x8	R8 (Bank 1)	Bit Name	-	-	TC2ES	TC2M	TC2S	TC2CK2	TC2CK1	TC2CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	P	P	P	P	P
0x9	R9 (Bank 1)	Bit Name	TC2D15	TC2D14	TC2D13	TC2D12	TC2D11	TC2D10	TC2D9	TC2D8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0XA	RA (Bank 1)	Bit Name	TC2D7	TC2D6	TC2D5	TC2D4	TC2D3	TC2D2	TC2D1	TC2D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XB	RB (Bank 1)	Bit Name	DORD	TD1	TD0	-	OD3	OD4	-	RBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XC	RC (Bank 1)	Bit Name	CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SSBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XD	RD (Bank 1)	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XE	RE (Bank 1)	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XF	RF (Bank 1)	Bit Name	-	-	TCIF3	TCIF2	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	R5 (Bank 2)	Bit Name	-	-	-	-	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x06	R6 (Bank 1)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	-	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x7	R7 (Bank 2)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	ADCPO	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	0	0
0x8	R8 (Bank 2)	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x9	R9 (Bank 2)	Bit Name	-	-	-	-	AD3	AD2	AD1	AD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x0F	RF (Bank 2)	Bit Name	-	-	-	-	/PH73	/PH72	/PH71	/PH70
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x06	R6 (Bank 3)	Bit Name	-	PGAADEN	PGA0	POP	PPC	PG2	PG1	PG0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0XD	RD (Bank 3)	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XE	RE (Bank 3)	Bit Name	TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XF	RF (Bank 3)	Bit Name	-	-	-	-	/PD73	/PD72	/PD71	/PD70
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x0A	IOCA	Bit Name	WDTE	EIS	-	-	PSWE	PSW2	PSW1	PSW0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	0	0	P	P	P	P
0x0B	IOCB	Bit Name	/PD7	/PD6	/PD5	/PD4	/PD3	/PD2	/PD1	/PD0
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0C	IOCC	Bit Name	–	–	–	–	OD3	OD2	OD1	OD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x0D	IOCD	Bit Name	-	-	-	-	/PH3	/PH2	/PH1	/PH0
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0E	IOCE	Bit Name	-	-	TCIE3	TCIE2	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	P	0	0	0	0
0x0F	IOCF	Bit Name	LVDIE	ADIE	SPIE	-	-	EXIE	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	0	0	P	P	P
0x10~ 0x2F	R10~ R2F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Legend: **"x"** = not used **"P"** = previous value before reset
"u" = unknown or don't care **"t"** = check Table 9

* To jump to Address 0x08, or to execute the instruction which is next to the "SLEP" instruction.

6.5.2 Status of RST, T, and P of the Status Register

A reset condition is initiated by the following events:

1. Power-on condition

2. High-low-high pulse on /RESET pin

3. Watchdog timer time-out

The values of T and P, listed in Table 8 are used to check how the processor wakes up. Table 9 shows the events that may affect the status of T and P.

Table 8. Values of RST, T and P after Reset

Reset Type	T	P
Power on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

* P: Previous status before reset

Table 9 Status of T and P Being Affected by Events.

Event	T	P
Power on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin change during Sleep mode	1	0

* P: Previous value before reset

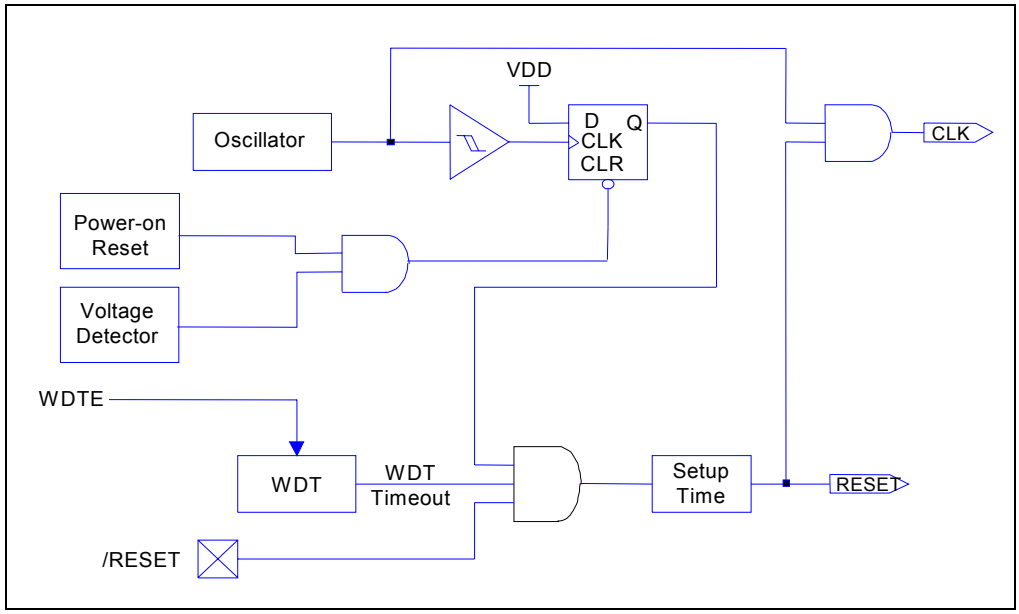


Figure 6-14 Block Diagram of Controller Reset

6.6 Interrupt

The EM78F652N has 8 interrupts (4 external, 4 internal) listed below:

Interrupt Source		Enable Condition	Int. Flag	Int. Vector	Priority
Internal / External	Reset	-	-	0000	High 0
External	INT	ENI + EXIE=1	EXIF	0003	1
External	Port 6 pin change	ENI +ICIE=1	ICIF	0006	2
Internal	TCC	ENI + TCIE=1	TCIF	0009	3
External	LVD	ENI + LVDIE=1	LVDIF	000C	4
External	SPI	ENI + SPIE=1	SPIF	0012	5
Internal	TC2	ENI + TCIE2=1	TCIF2	0024	6
Internal	TC3	ENI + TCIE3=1	TCIF3	0027	7
Internal	AD	ENI + ADIE=1	ADIF	0030	8

RE and RF are the interrupt status registers that record the interrupt requests in the relative flags/bits. IOCE and IOCF are the interrupt mask registers. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the enabled interrupts occurs, the next instruction will be fetched from their individual address. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF & RE) is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

The external interrupt has an on-chip digital noise rejection circuit (input pulse less than **8 system clock time** is eliminated as noise), **but in Low Crystal oscillator (LXT) mode, the noise rejection circuit will be disabled.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register will be saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3 and R4 will be pushed back.

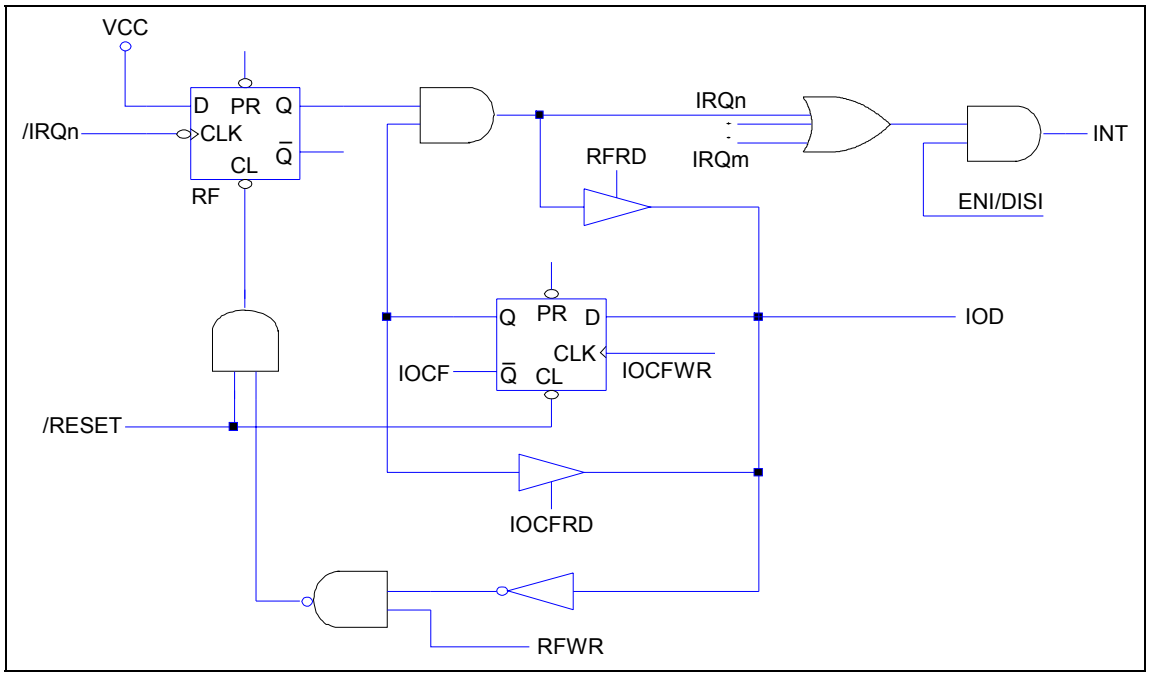


Figure 6-15 Interrupt Input Circuit

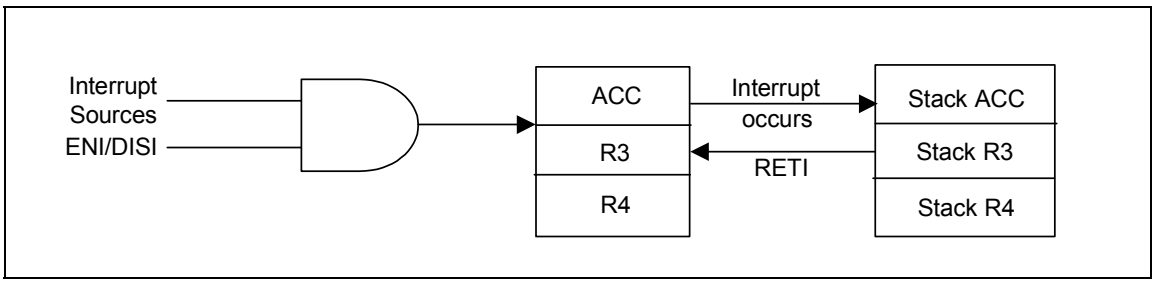


Figure 6-16 Interrupt Back-up Diagram

6.7 LVD (Low Voltage Detector)

During power source unstable situations, such as external power noise interference or EMS test condition, it will cause the power to vibrate fiercely. At the time Vdd is unsettled, it is probably below the working voltage. When the system supply voltage, Vdd, is below the working voltage, the IC kernel must keep all register status automatically.

LVD property is set at Register RE, Bit 1, 0 detailed operation mode is as follows:

Bits 1~Bit 0 (LVD1~LVD0): Low Voltage Detect level control Bits.

LVD1	LVD0	LVD Voltage Interrupt Level
0	0	2.3
0	1	3.3
1	0	4.0
1	1	4.5

The LVD status and interrupt flag is referred to as RF

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RF	LVDIF	ADIF	SPIF	-	-	EXIF	ICIF	TCIF

Bit 7 (LVDIF): Low voltage Detector interrupt flag.

When LVD1, LVD0 = “0, 0”, Vdd > 2.5V, LVDIF is “0”, Vdd ≤ 2.3V, set LVDIF to “1”. LVDIF is reset to “0” by software.

When LVD1, LVD0 = “0, 1”, Vdd > 3.5V, LVDIF is “0”, Vdd ≤ 3.3V, set LVDIF to “1”. LVDIF is reset to “0” by software.

When LVD1, LVD0 = “1, 0”, Vdd > 4.2V, LVDIF is “0”, Vdd ≤ 4.0V, set LVDIF to “1”. LVDIF is reset to “0” by software.

When LVD1, LVD0 = “1, 1”, Vdd > 4.7V, LVDIF is “0”, Vdd ≤ 4.5V, set LVDIF to “1”. LVDIF is reset to “0” by software.

The following steps are needed to setup the LVD function:

Set the LVDEN of Register RE to “1”, then use Bit 1, 0 (LVD1, LVD0) of Register RE to set LVD interrupt level

Wait for LVD interrupt to occur.

Clear LVD interrupt flag

The internal LVD module uses internal circuit to fit. When the LVDEN is set to enable the LVD module, the current consumption will increase to about 10μA.

During sleep mode, the LVD module continues to operate. If the device voltage drops slowly and crosses the detect point, the LVDIF bit will be set and the device won’t wake-up from Sleep mode. Until the other wake-up sources wake up the device, the LVD interrupt flag is still set at the prior status. When the system resets, the LVD flag will be cleared.

Figure 6-17 shows the LVD module to detect the external voltage situation.

When Vdd drops not below V_{LVD}, LVDIF remains at “0”.

When Vdd drops below V_{LVD}, LVDIF is set to “1”. If global ENI enable, LVDIF will be set to “1”, the next instruction will branch to interrupt vector. The LVD interrupt flag is cleared to “0” by software.

When Vdd drops below V_{RESET} and is less than 80μs, the system will all maintain the register status and system halt but oscillation is active. When Vdd drops below V_{RESET} and is more than 80μs, a system reset will occur, and for the following waveform situation, refer to Section 6.5.1 *Reset Description*.

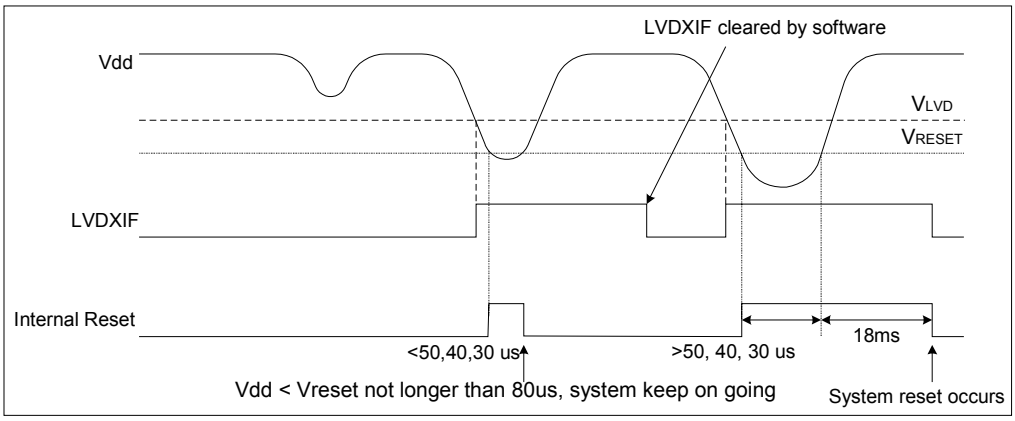


Figure 6-17 LVD Waveform Situation

6.8 Data EEPROM

The Data EEPROM is readable and writable during normal operation over the whole Vdd range. The operation for Data EEPROM is base on a single byte. A write operation makes an erase-then-write cycle to take place on the allocated byte.

The Data EEPROM memory provides high erase and write cycles. A byte write automatically erases the location and writes the new value.

6.8.1 Data EEPROM Control Register

6.8.1.1 RB (EEPROM Control Register)

The EECR (EEPROM Control Register) is the control register for configuring and initiating the control register status.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RD	WR	EEWE	EEDF	EEPC	-	-	-

Bit 7：Read control register

0 : Does not execute EEPROM read

1 : Read EEPROM content, (RD can be set by software, RD is cleared by hardware after Read instruction is completed)

Bit 6：Write control register

0 : Write cycle to the EEPROM is complete.

1 : Initiate a write cycle, (WR can be set by software, WR is cleared by hardware after Write cycle is completed)

Bit 5：EEPROM Write Enable bit

0 : Prohibit write to the EEPROM

1 : Allows EEPROM write cycles.

Bit 4：EEPROM Detect Flag

0 : Write cycle is completed

1 : Write cycle is unfinished

Bit 3：EEPROM power-down control bit

0 : Switch off the EEPROM

1 : EEPROM is operating

Bits 2 ~ 0: Not used, set to "0" at all time

6.8.1.2 RC (256 Bytes EEPROM Address)

When accessing the EEPROM data memory, the RC (256 bytes EEPROM address register) holds the address to be accessed. According the operation, the RD (256 bytes EEPROM Data register) holds the data to written, or the data read, at the address in RC.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_A7	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0

Bits 7 ~ 0: 256 bytes EEPROM address

6.8.1.3 RD (256 Bytes EEPROM Data)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0

Bits 7 ~ 0: 256 bytes EEPROM data

6.8.2 Programming Step / Example Demonstration

6.8.2.1 Programming Step

Follow these steps to write or read data from the EEPROM:

(1) Set the RB.EEPC bit to 1 for enable EEPROM power.

(2) Write the address to RC (256 bytes EEPROM address).

a.1. Set the RB.EEWE bit to 1, if the write function is employed.

a.2. Write the 8-bit data value to be programmed in the RD (256 bytes EEPROM data)

a.3. Set the RB.WR bit to 1, then execute write function

b. Set the RB.READ bit to 1, after which, execute read function

(3) a. Wait for the RB.EEDF or RB.WR to be cleared

b. Wait for the RB.EEDF to be cleared

(4) For the next conversion, go to Step 2 as required.

(5) If user wants to save power and to make sure the EEPROM data is not used, clear the RB.EEPC.

6.8.2.2 Example Demonstration Programs

```
;To define the control register
;Write data to EEPROM
RC == 0x0C
RB == 0x0B
RD == 0x0D
Read == 0x07
WR == 0x06
EEWE == 0x05
EEDF == 0x04
EEPC == 0x03

BS RB, EEPC       ; Set the EEPROM power on
MOV A,@0x0A
MOV RC,A          ; Assign the address from EEPROM
BS RB, EEWE       ; Enable the EEPROM write function
MOV A,@0x55
MOV RD,A          ; Set the data for EEPROM
BS RB,WR          ; Write value to EEPROM
JBC RB,EEDF       ; To check the EEPROM bit complete or not
JMP $-1
```

6.9 Analog-To-Digital Converter (ADC)

The analog-to-digital circuitry consists of a 12-bit analog multiplexer, three control registers (AISR/R5 (Bank 2), ADCON/R6 (Bank 2), ADOC/R7 (Bank 2)), two data registers (ADDH, ADDL/R8, R9) and an ADC with 12-bit resolution. The functional block diagram of the ADC is shown in Figure 6-18. The analog reference voltage (Vref) and analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDH and ADDL. Input channels are selected by the analog input multiplexer via the ADCON register Bits ADIS0 and ADIS1.

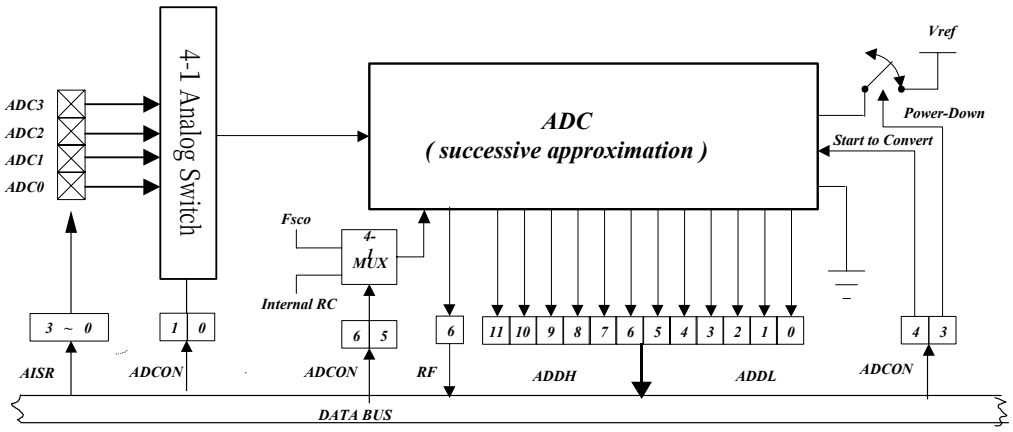


Figure 6-18 Functional Block Diagram of Analog-to-Digital Conversion

6.9.1 ADC Control Register (AISR/R5, ADCON/R6, ADOC/R7)

6.9.1.1 Bank 2 R5 AISR (ADC Input Select Register)

The AISR register individually defines the Port 6 pins as analog inputs or as digital I/O.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	-	-	-	-	ADE3	ADE2	ADE1	ADE0
*Init_Value	0	0	0	0	0	0	0	0

Bits 7 ~ 4: Not used, set to "0" at all time

Bit 3 (ADE3): AD converter enable bit of P63 pin.

0 : Disable ADC3, P63 act as I/O pin

1 : Enable ADC3 act as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin

0 : Disable ADC2, P62 functions as I/O pin

1 : Enable ADC2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

0 : Disable ADC1, P61 functions as I/O pin

1 : Enable ADC1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin.

0 : Disable ADC0, P60 functions as I/O pin

1 : Enable ADC0 to function as analog input pin

6.9.1.2 Bank 2 R6 ADCON (A/D Control Register)

The ADCON register controls the operation of the A/D conversion and decides which pin should be currently active.

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	VREFS	CKR1	CKR0	ADRUN	ADPD	-	ADIS1	ADIS0
*Init_Value	0	0	0	0	0	0	0	0

*Init_Value: Initial value during power-on reset

Bit 7 (VREFS): ADC's Vref input source

0 : ADC's Vref is connected to Vdd (default value), and the P50/VREF pin carries out the function of P50

1 : ADC's Vref is connected to P50/VREF

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler of oscillator clock rate of ADC

00 = 1: 16 (default value)

01 = 1: 4

10 = 1: 64

11 = 1: WDT ring oscillator frequency

CKR1/CKR0	Operation Mode	Max. Operation Frequency
00	Fosc/16	4 MHz
01	Fosc/4	1 MHz
10	Fosc/64	16 MHz
11	Internal RC	1 MHz

Bit 4 (ADRUN): ADC starts to run

0 : reset on completion of the conversion. This bit cannot be reset by software

1 : an A/D conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode

0 : switch off the resistor reference to save power even while the CPU is operating

1 : ADC is operating

Bit 2: Not used, set to "0" at all time

Bit 1 ~ Bit 0 (ADIS1 ~ ADIS0): Analog Input Select

000 = AN0/P60

001 = AN1/P61

010 = AN2/P62

011 = AN3/P63

They can only be changed when the ADIF bit and the ADRUN bit are both LOW.

6.9.1.3 Bank 2 R7 ADOC (A/D Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	-	-	-

Bit 7 (CALI): Calibration enable bit for A/D offset

0 : Calibration disable

1 : Calibration enable

Bit 6 (SIGN): Polarity bit of offset voltage

0 : Negative voltage

1 : Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

Bits 2 ~ 0: Not used, set to "0" at all time

6.9.2 ADC Data Buffer (ADDH, ADDL/R8, R9)

When the A/D conversion is complete, the result is loaded to the ADDH, ADDL. The ADRUN bit is cleared, and the ADIF is set.

6.9.3 A/D Sampling Time

The accuracy, linearity, and speed of the successive approximation A/D converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2μs for each KΩ of the analog source impedance and at least 2μs for the low-impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion can be started.

6.9.4 A/D Conversion Time

CKR0 and CKR1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the accuracy of A/D conversion. For the EM78F652N, the conversion time per bit is 4μs. Table 10 shows the relationship between Tct and the maximum operating frequencies.

Table 10. Tct vs. Maximum Operation Frequency

CKR0: CKR1	Operation Mode	Max. Operating Frequency	Max. Conversion Rate Per Bit	Max. Conversion Rate
00	Fosc/16	4 MHz	250kHz (4μs)	14*4μs=56μs (17.9kHz)
01	Fosc/4	1 MHz	250kHz (4μs)	14*4μs=56μs (17.9kHz)
10	Fosc/64	16 MHz	250kHz (4μs)	14*4μs=56μs (17.9kHz)
11	Internal RC	1 MHz	14kHz (71μs)	14*71μs=994μs (1kHz)

NOTE

The pin that is not used as an analog input pin can be used as regular input or output pins.

During conversion, do not perform output instruction to maintain a precision for all of the pins.

6.9.5 A/D Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduced power consumption, the A/D conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, TC2, TC3, and A/D conversion.

The AD Conversion is considered completed when:

1 ADRUN Bit of R6 Register Is Cleared to “0”.

2 Wake-Up from A/D Conversion Remains in Operation during Sleep Mode.

The result is fed to the ADDATA, ADOC when the conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the A/D conversion will be shut off, no matter what the status of ADPD bit is.

6.9.6 Programming Steps/Considerations

6.9.6.1 Programming Steps

Follow the following steps to obtain data from the ADC:

1. Write to the four bits (ADE3 ~ ADE0) on the R5 (AISR) register to define the characteristics of R6: Digital I/O, analog channels, and voltage reference pin.
2. Write to the R6/ADCON register to configure the AD module:
   a. Select A/D input channel (ADIS1 ~ ADIS0).
   b. Define the A/D conversion clock rate (CKR1 ~ CKR0).
   c. Select the input source of the VREFS of the ADC.
   d. Set the ADPD bit to 1 to begin sampling.
3. Set the ADWE bit, if the wake-up function is employed.
4. Set the ADIE bit, if the interrupt function is employed.
5. Put “ENI” instruction, if the interrupt function is employed.
6. Set the ADRUN bit to 1.
7. Wait for wake-up or when ADRUN bit is cleared to “0”.
8. Read ADDATA, ADOC the conversion data register.
9. Clear the interrupt flag bit (ADIF) when A/D interrupt function has occurred.
10. For the next conversion, go to Step 1 or Step 2 as required. At least two Tct is required before the next acquisition starts.

NOTE

To obtain an accurate value, it is necessary to avoid any data transition on the I/O pins during AD conversion.

6.9.6.2 The Demonstration Programs

```
; To define the general registers
R_0 == 0                    ; Indirect addressing register
PSW == 3                    ; Status register
PORT5 == 5
PORT6 == 6
RE== 0XE                    ; wake-up control resister
RF== 0XF                    ; Interrupt status register

; To define the control register
IOC50 == 0X5                ; Control Register of Port 5
IOC60 == 0X6                ; Control Register of Port 6
C_INT== 0XF                 ; Interrupt Control Register
```

```
;ADC Control Registers
ADDATA == 0x8              ; The contents are the results of ADC
AISR == 0x08               ; ADC output select register
ADCON == 0x6               ; 7    6    5    4    3   2   1    0
                             VREFS  CKR1  CKR0  ADRUN  ADPD
                             –    ADIS1 ADIS0
;To define bits
;In ADCON
ADRUN == 0x4               ; ADC is executed as the bit is set
ADPD == 0x3                ; Power Mode of ADC

ORG 0                      ; Initial address
JMP INITIAL
ORG 0x30                   ; Interrupt vector

(User program)
CLR RF                     ; To clear the ADIF bit
BS ADCON  , ADRUN          ; To start to execute the next AD
                           ; conversion if necessary
RETI

INITIAL:
MOV A      , @0B00000001   ; To define P60 as an analog input
MOV AISR   , A
MOV A      , @0B00001000   ; To select P60 as an analog input
                           ; channel, and AD power on
MOV ADCON  , A             ; To define P60 as an input pin and
                           ; set clock rate at fosc/16
En_ADC:
MOV A      , @0BXXXXXXX1   ; To define P60 as an input pin, and
                           ; the others are dependent
IOW PORT6                  ; on applications
MOV A      , @0BXXXX1XXX   ; Enable the ADWE wake-up function
                           ; of ADC, “X” by application
MOV RE     , A
MOV A      , @0BXXXX1XXX   ; Enable the ADIE interrupt function
                           ; of ADC, “X” by application
IOW C_INT

ENI                        ; Enable the interrupt function
BS ADCON   , ADRUN         ; Start to run the ADC
                           ; If the interrupt function is
                           ; employed, the following three lines
                           ; may be ignored
POLLING:
JBC ADCON  , ADRUN         ; To check the ADRUN bit continuously
JMP                        ; ADRUN bit will be reset as the AD
POLLING                    ; conversion is completed
(User program)
```

6.10 Timer/Counter 2

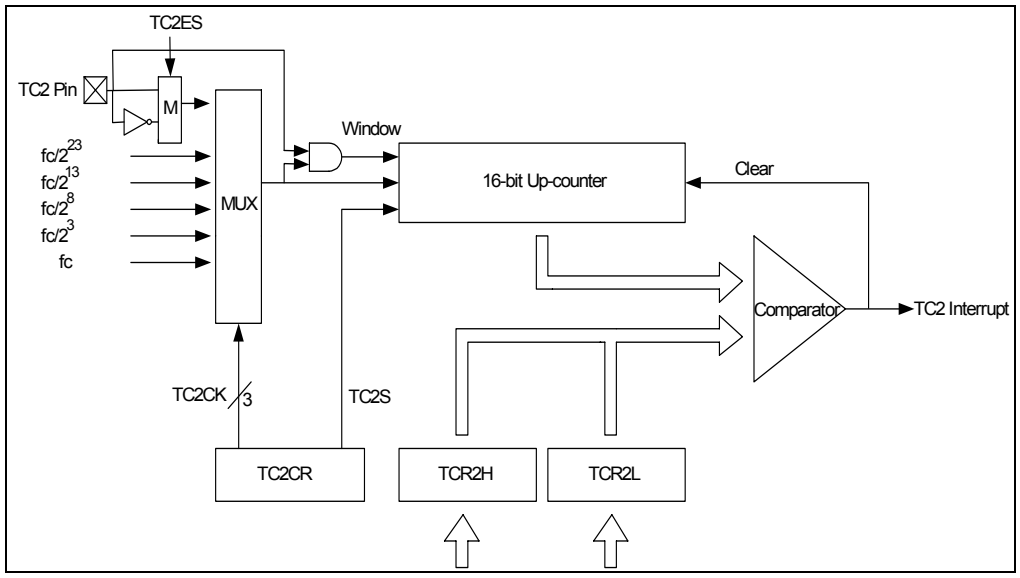


Figure 6-19 Configuration of Timer / Counter 2

In Timer mode, counting up is performed using the internal clock. When the contents of the up-counter matched the TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

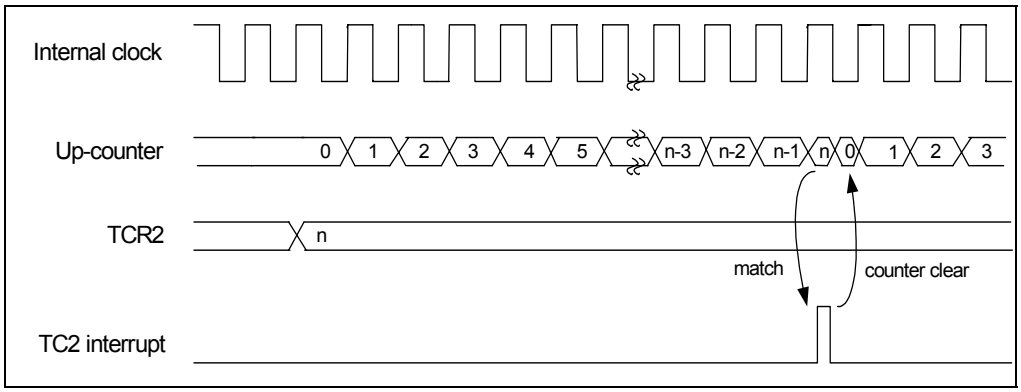


Figure 6-20 Timer Mode Timing Chart

In Counter mode, counting up is performed using external clock input pin (TC2 pin) and either rising or falling can be selected by setting TC2ES. When the contents of the up-counter matched the TCR2 (TCR2H+TCR2L), then interrupt is generated and counter is cleared. Counting up resumes after the counter is cleared.

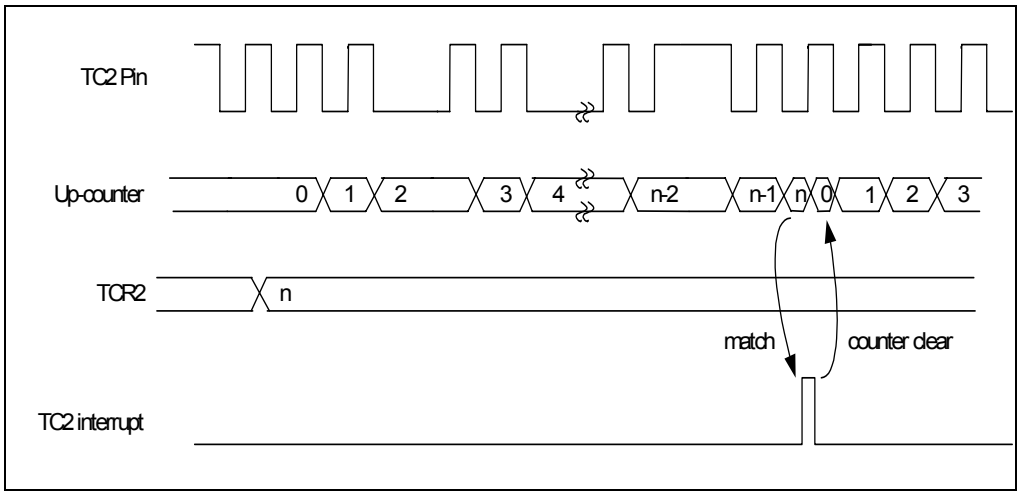


Figure 6-21 Counter Mode Timing Chart (INT2ES = 1)

In Window mode, counting up is performed on a rising edge of the pulse that is logical AND of an internal clock and the TC2 pin (window pulse). When the contents of the up-counter are matched with the TCR2 (TCR2H+TCR2L), then interrupt is generated and the counter is cleared. The frequency (window pulse) must be slower than the selected internal clock.

While writing to the TCR2L, the comparison is inhibited until TCR2H is written.

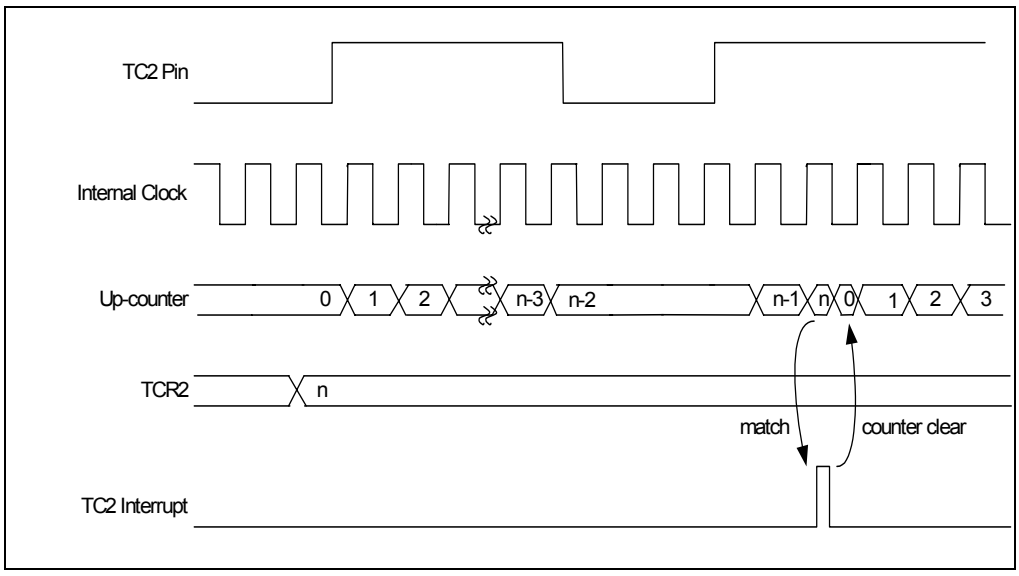


Figure 6-22 Window Mode Timing Chart

6.11 Timer/Counter 3

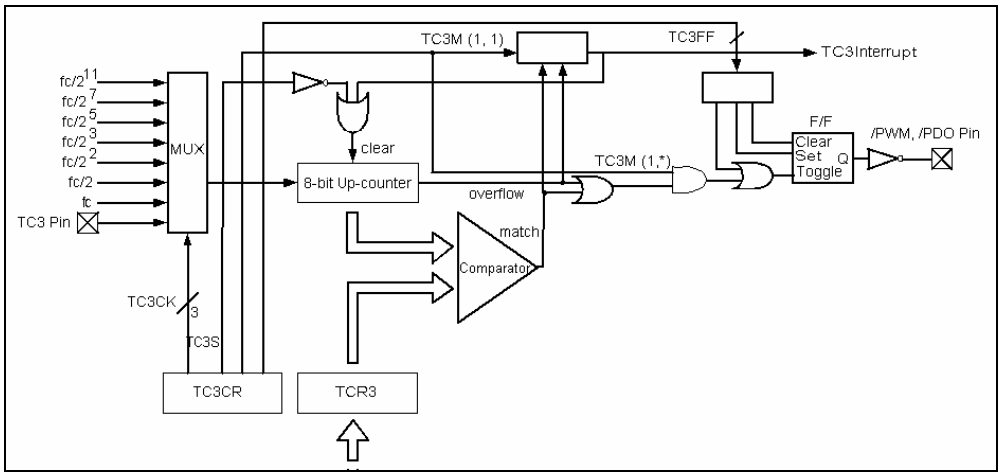


Figure 6-23 Timer / Counter 3 Configuration

In Timer mode, counting up is performed using internal clock (rising edge trigger). When the contents of the up-counter matched with the contents of TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using the external clock input pin (TC3 pin). When the contents of the up-counter matched with the contents of TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

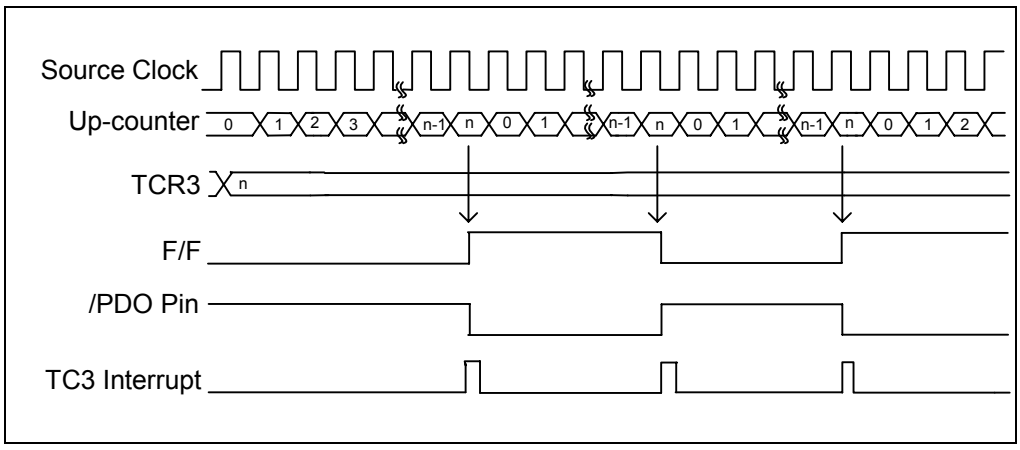


Figure 6-24 PDO Mode Timing Chart

In Pulse Width Modulation (PWM) Output mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. While the counter is counting, the F/F is toggled again when the counter overflows, then the counter is cleared. The F/F output is inverted and output to the /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Hence, the output can be changed continuously. Also, on the first time, TRC3 is shifted by setting TC3S to "1" after data is loaded to TCR3.

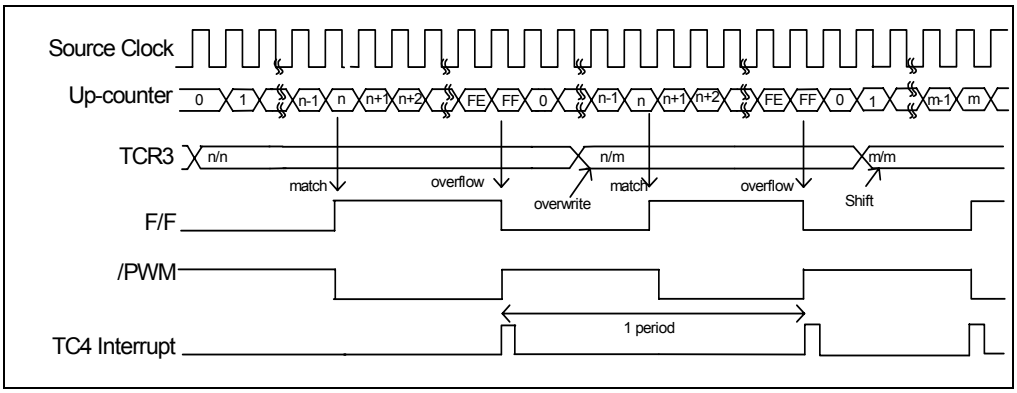


Figure 6-25 PWM Mode Timing Chart

6.12 One Set of 2 Orders OP Amplifier

The EM78F652N has one set of 2 orders OP Amplifier, which has two major components, Operational Amplifier (OP Amp) and Programmable Gain Amplifier (PGA). The signal will be amplified by OP Amp and PGA. User can configure the input and output of the OP Amp by using external resistors and capacitors. The PGA is an inverting configuration of the OP Amp. It is controlled by three digital lines and provides eight different gains.

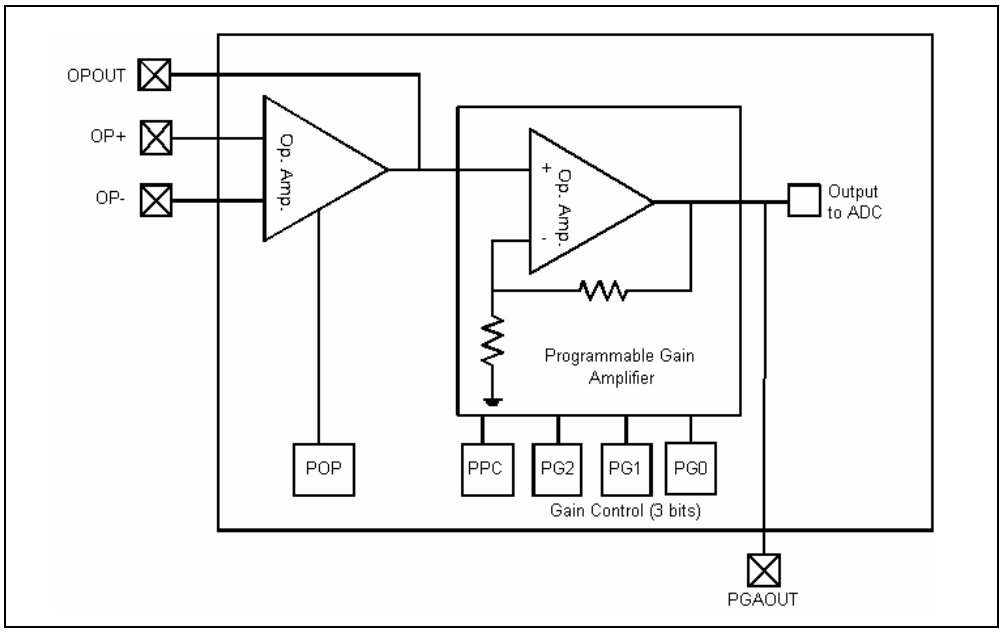


Figure 6-26 Operational Amplifier Block Diagram

6.13 SPI

6.13.1 Overview & Features

Overview:

Figure 6-27, 6-28 and 6-29 shows how the EM78F652N communicates with other devices through SPI module. If EM78F652N is a master controller, it sends clock pulse through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if the EM78F652N is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. You can also set SPIS Bit 7 (DORD) to determine the SPI transmission order, SPIC Bit 3 (SDOC) to control the SO pin after serial data output status and SPIS Bit 6 (TD1), Bit 5 (TD0) determine the SO status output delay times.

Features:

- Operation in either Master mode or Slave mode
- Three-wire or four-wire full duplex synchronous communication
- Programmable baud rates of communication
- Programming clock polarity, (RD Bit 7)
- Interrupt flag available for the read buffer full
- SPI transmission order
- After serial data output SO status select
- SO status output delay times
- SPI handshake pin
- Up to 8 MHz (maximum) bit frequency

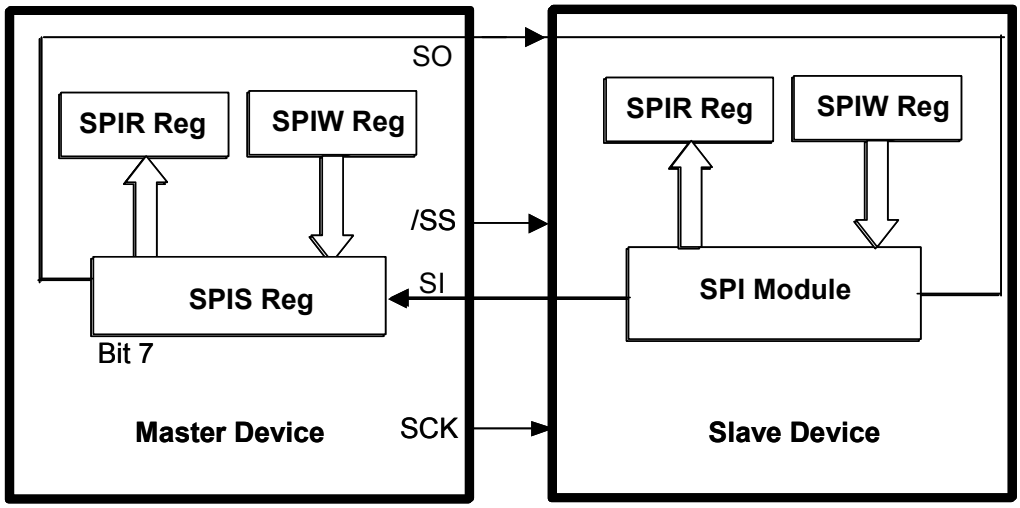


Figure 6-27 SPI Master/Slave Communication

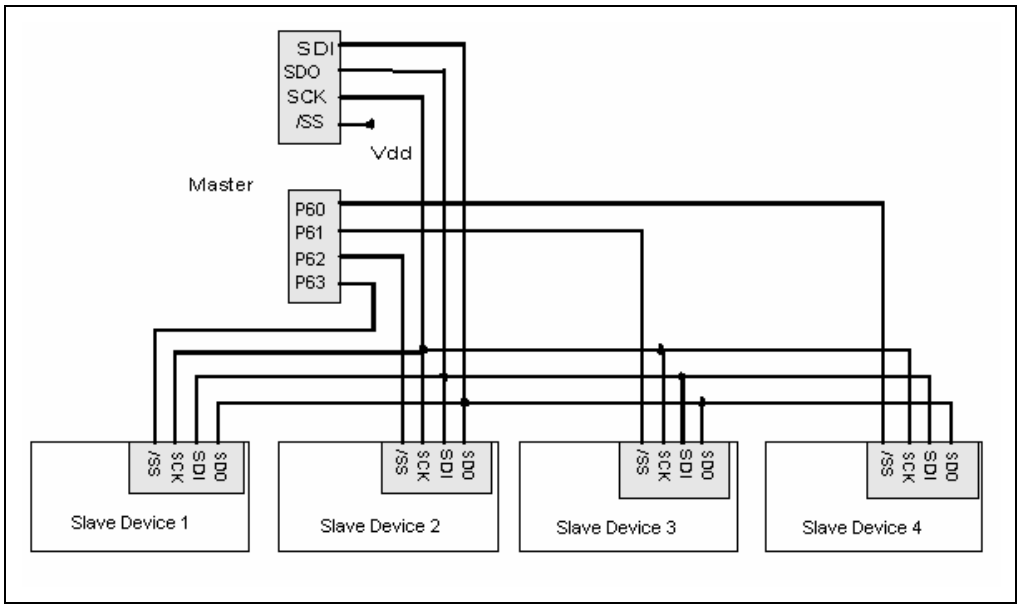


Figure 6-28 SPI Configuration of a Single-Master and Multi-Slave

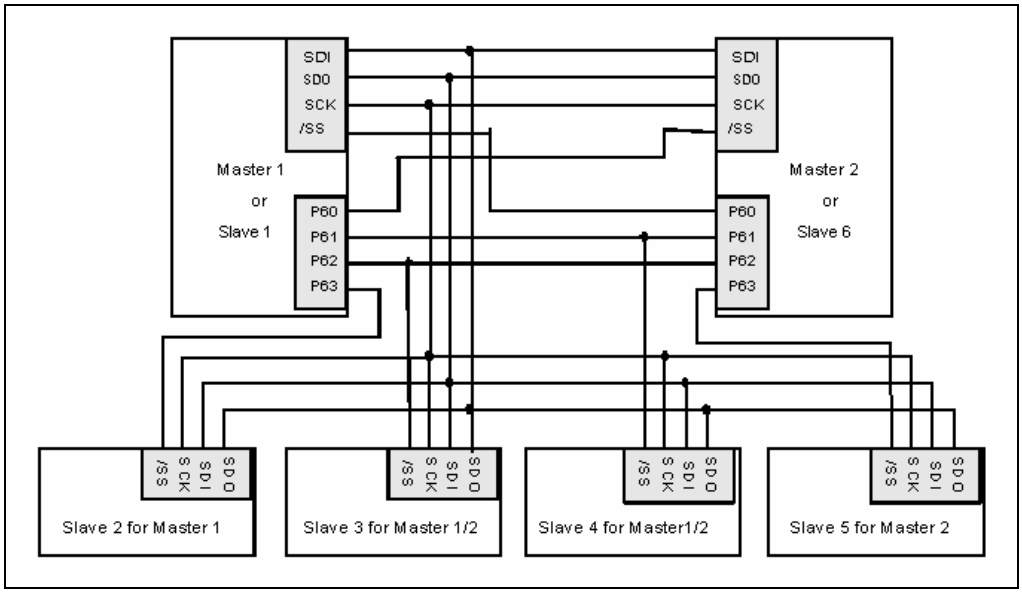


Figure 6-29 SPI Configuration of a Single-Master and Multi-Slave

6.13.2 SPI Function Description

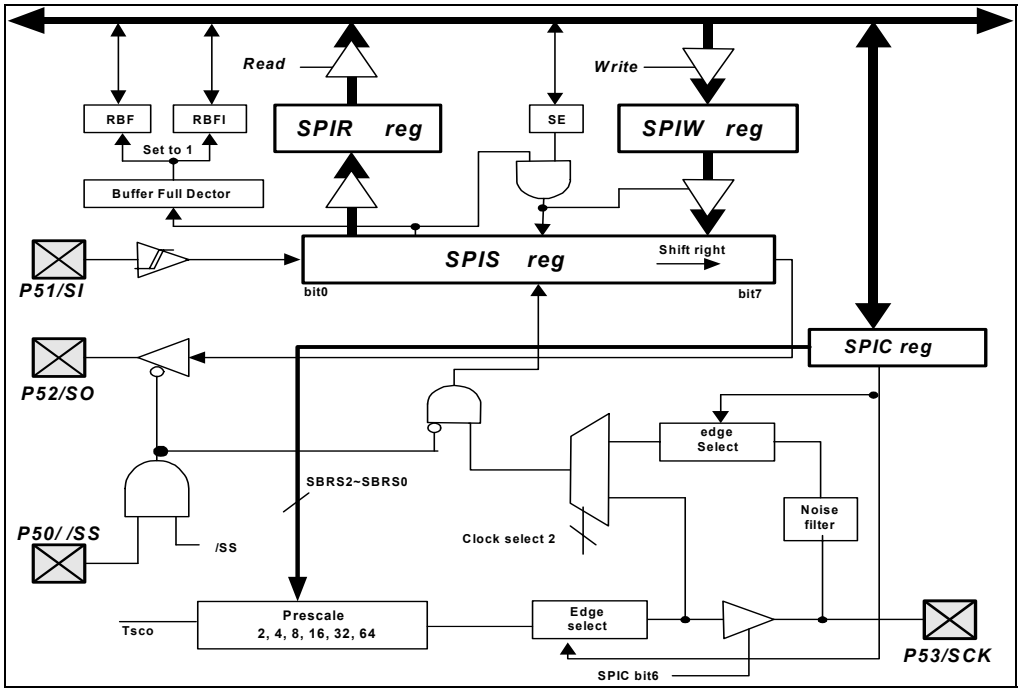


Figure 6-30 SPI Block Diagram

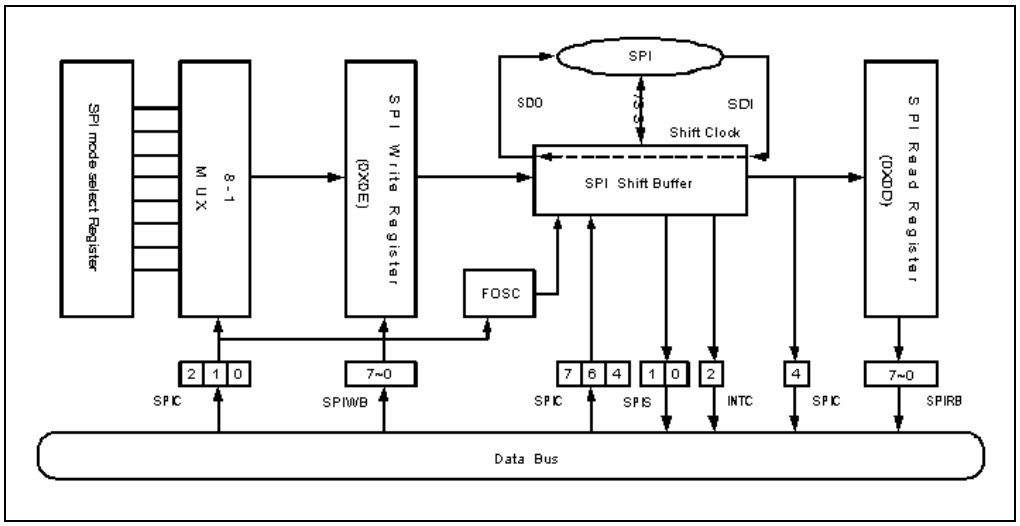


Figure 6-31 Function Block Diagram of SPI Transmission

Below are the functions of each block and explanations on how to carry out the SPI communication with the signals depicted in Figure 6-31 and Figure 6-32:

- P52 / SI : Serial Data In
- P51 / SO : Serial Data Out
- P53 / SCK : Serial Clock
- P50 / /SS : /Slave Select (Option). This pin (/SS) may be required during a slave mode
- RBF: Set by Buffer Full Detector, and reset by software
- Buffer Full Detector: Set to 1 when an 8-bit shifting is completed
- SSE: Loads the data in SPIS register, and begin to shift
- SPIS reg.: Shifting byte in and out. The MSB is shifted first. Both the SPIS and the SPIW registers are loaded at the same time. Once data are written, SPIS starts transmission / reception. The data received are moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the RBFI (Read Buffer Full Interrupt) flags are then set.
- SPIR reg.: Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- SPIW reg.: Write buffer. The buffer will deny any attempts to write until the 8-bit shifting is completed.

The SSE bit will be kept in “1“ if the communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.

- SBRS2~SBRS0 : Programs the clock frequency/rates and sources
- Clock Select : Selects either internal or external clock as the shifting clock
- Edge Select : Selects the appropriate clock edges by programming the CES bit

6.13.3 SPI Signal & Pin Description

The detailed functions of the four pins, SDI, SDO, SCK, and /SS, which are shown in Figure 6-39, are as follows:

SI/P52

- Serial Data In
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Defined as high-impedance, if not selected
- Program the same clock rate and clock edge to latch on both the master and slave devices
- The byte received will update the transmitted byte
- Both the RBF and RBFIF bits (located in Register 0x0C) will be set as the SPI operation is completed.
- Timing is shown in Figure 6-32 and 6-33

SO/P51

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- Program the same clock rate and clock edge to latch on both the master and slave devices
- The received byte will update the transmitted byte
- The CES (located in Register 0x0D) bit will be reset, as the SPI operation is completed
- Timing is shown in Figure 6-32 and 6-33

SCK/P53

- Serial Clock
- Generated by a master device
- Synchronize the data communication on both the SDI and SDO pins
- The CES (located in Register 0x0D) is used to select the edge to communicate
- The SBR0~SBR2 (located in Register 0x0D) is used to determine the baud rate of communication
- The CES, SBR0, SBR1, and SBR2 bits have no effect in the slave mode
- Timing is show in Figure 6-32 and 6-33

/SS/P50

- Slave Select; negative logic
- Generated by a master device to signify the slave(s) to receive data
- Goes low before the first cycle of SCK appears, and remains low until the last (eighth) cycle is completed
- Ignores the data on the SDI and SDO pins while /SS is high, because the SDO is no longer driven
- Timing is shown in Figure 6-32 and 6-33

6.13.4 Program the Related Registers

As the SPI mode is defined, the related registers are shown in Table 2 and Table 3.

Table 1 Related Control Registers of the SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1 0x0C	*SPIC/RC	CES	SPIE	SRO	SSE	SDOC	SBR2	SBR1	SBR0
Bank 0 0x0F	IOCF	LVDIE	ADIE	SPIE	–	–	EXIE	ICIE	TCIE

***SPIC:** SPI control register

Bit 7 (CES): Clock Edge Select bit

0 : Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during a low-level.

1 : Data shifts out on a falling edge, and shifts in on a rising edge. Data is on hold during a high-level.

Bit 6 (SPIE): SPI Enable bit

0 : Disable SPI mode

1 : Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0 : No overflow

1 : A new data is received while the previous data is still being held in the SPIB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, users are required to read the SPIRB register although only the transmission is implemented.

- This can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0 : Reset as soon as the shifting is complete, and the next byte is ready to shift

1 : Start to shift, and keep on “1” while the current byte is still being transmitted

- This bit will reset to 0 at every one-byte transmission by the hardware.

Bit 3 (SDOC): SDO output status control bit

0 : After the Serial data output, the SDO remains high

1 : After the Serial data output, the SDO remains low

Bit 2~Bit 0 (SBRS2 ~ SBRS0): SPI Baud Rate Select bits

SBRS2 (Bit 2)	SBRS1 (Bit 1)	SBRS0 (Bit 0)	Mode	Baud Rate
0	0	0	Master	Fosc/2
0	0	1	Master	Fosc/4
0	1	0	Master	Fosc/8
0	1	1	Master	Fosc/16
1	0	0	Master	Fosc/32
1	0	1	Master	Fosc/64
1	1	0	Slave	/SS disable
1	1	1	Slave	/SS enable

IOCF: Interrupt Mask Register

Bit 7(LVDIE): LVDIF interrupt enable bit

0 : Disable LVDIF interrupt

1 : Enable LVDIF interrupt

Bit 6 (ADIE): ADIF interrupt enable bit.

0 : Disable ADIF interrupt

1 : Enable ADIF interrupt

When the ADC Complete is used to enter an interrupt vector or enter next instruction, the ADIE bit must be set to “Enable“.

Bit 5 (SPIE): Interrupt enable bit

0 : Disable SPIF interrupt

1 : Enable SPIF interrupt

Bits 4 ~ 3: Not used, set to “0” at all time

Bit 2 (EXIE): EXIF interrupt enable bit.

0 : disable EXIF interrupt

1 : enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit.

0 : Disable ICIF interrupt

1 : Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0 : Disable TCIF interrupt

1 : Enable TCIF interrupt

Table 10 Related Status/Data Registers in SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bank 1 0X0B	SPIS/RB	DORD	TD1	TD0	-	OD3	OD4	-	RBF
Bank 1 0x0D	SPIRB/RD	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
Bank 1 0x0E	SPIWB/RE	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

SPIS: SPI Status register

Bit 7 (DORD): Read Buffer Full Interrupt flag

0 : Shift left (MSB first)

1 : Shift right (LSB first)

Bit 6~Bit 5 (TD1 ~ TD0): SDO Status Output Delay Time Options

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4: Not used, set to “0” at all time

Bit 3 (OD3): Open-Drain Control bit (P51)

0 : SO open-drain disable

1 : SO open-drain enable

Bit 2 (OD4): Open Drain-Control bit (P53)

0 : SCK open-drain disable

1 : SCK open-drain enable

Bit 1: Not used, set to “0” at all time

Bit 0 (RBF): Read Buffer Full flag

0 : Receiving is ongoing, SPIB is empty

1 : Receiving is completed, SPIB is full

SPIRB: SPI Read Buffer. Once the serial data is received completely, it will load to SPIRB from SPISR. The RBF bit and the RBFIF bit in the SPIS register will also be set.

SPIWB: SPI Write Buffer. As a transmitted data is loaded, the SPIS register stands by and start to shift the data when sensing SCK edge with SSE set to “1”.

6.13.5 SPI Mode Timing

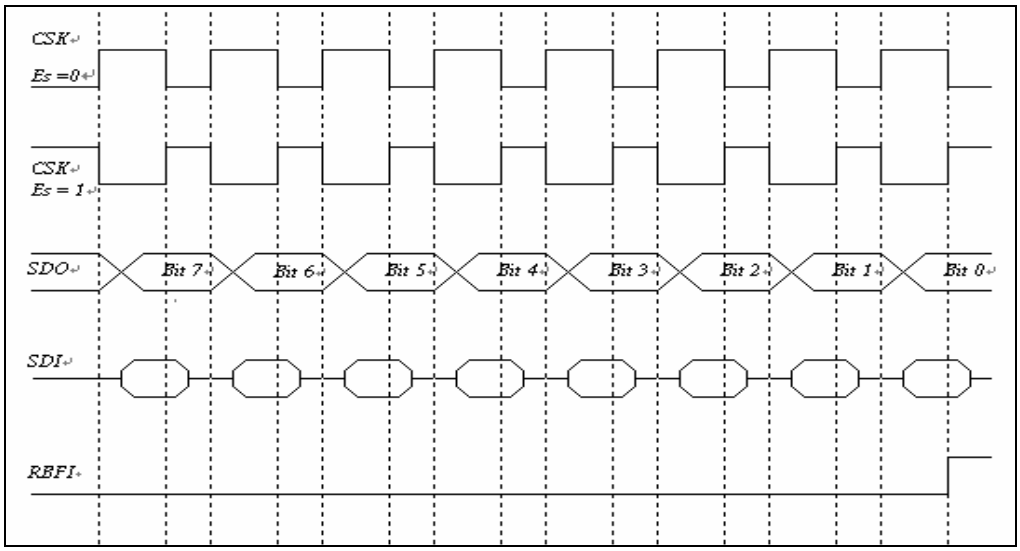


Figure 6-32 SPI Mode with /SS Disable

The SCK edge is selected by programming bit CES. The waveform shown in Figure 6-32 is applicable regardless whether the EM78R652 is in master or slave mode, with /SS disabled. However, the waveform in Figure 6-33 can only be implemented in slave mode, with /SS enabled.

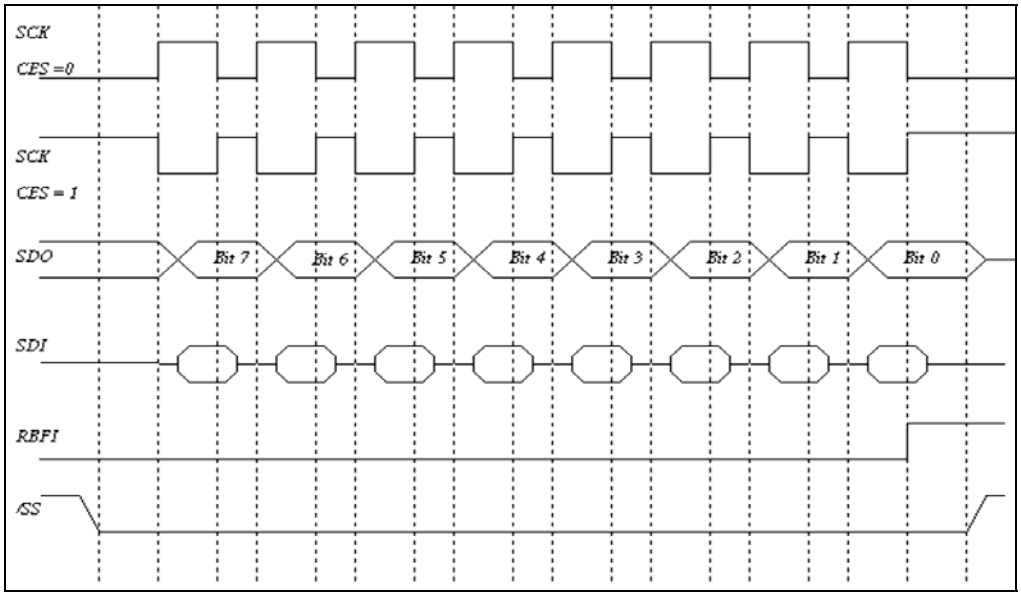


Figure 6-33 SPI Mode with /SS Enable

6.13.6 SPI Software Application

Example for SPI:

For Master

```
ORG 0X0
SETTING:
CLRA
IOW 0X05                        ; Set Port 5 output
IOW 0X06                        ; Set Port 6 output
MOV 0X05        , A
MOV A           , @0B11001111   ; Set WDT prescaler
CONTW
MOV A           , @0B00010001   ; Disable wakeup function
IOW 0X0E
MOV A           , @0B00000000   ; Disable interrupt
IOW 0X0F
MOV A           , @0x07         ; SDI input and SDO, SCK
                                ; output
IOW 0x09
MOV A           , @0B10000000   ; Clear RBF and RBFIF flag
MOV 0x0C        , A
MOV A           , @0B11100000   ; Select clock edge and
                                ; enable SPI
MOV 0X0D        , A

START:
WDTC
BC 0X0C         , 1             ; Clear RBFIF flag
MOV A           , @0XFF
MOV 0X05        , A             ; Show a signal at Port 5
MOV 0X0A        , A             ; Move FF at read buffer
MOV A           , @0XAA         ; Move AA at write buffer
MOV 0X0B        , A
BS 0X0D         , 4             ; Start to shift SPI data
JBC 0X0D        , 4             ; Polling loop for checking
                                ; SPI transmission completed
JMP $-2
BC 0X03         , 2
CALL DELAY                      ; To receive data from slave
MOV A           , 0X0A
XOR A           , @0X5A         ; Compare the data from
                                  slave
JBS 0X03        , 2
JMP START
```

```
FLAG:
MOV A           , @0X55         ; Show the signal when
                                ; receiving correct data
                                ; from slave
MOV 0X05        , A
CALL DELAY
JMP START
DELAY:
                                ; (User's program)
EOP
ORG 0XFFF
JMP SETTING
```

For Slave

```
ORG 0X0
INITI:
JMP INIT
ORG 0X2
INTERRUPT:                      ; Interrupt address
MOV A           , @0X55
MOV 0X06        , A             ; Show a signal at Port 6
                                ; when entering interrupt
MOV A           , @0B11100110   ; Enable SPI, /SS disabled
MOV 0X0D        , A
BS 0X0D         , 4             ; Keep SSE at 1 to wait
                                ; for SCK signal in order
                                ; to shift data
MOV A           , @0X00         ; Move 00 to write buffer
                                ; in order to keep master's
                                ; read buffer as 00
MOV 0X0B        , A
BS 0X0D         , 4             ; Keep SSE at 1 to wait for
                                ; SCK signal in order to
                                ; shift data
NOP
JBC 0X0D        , 4             ; Polling loop for checking
                                ; SPI transmission
                                  completed
JMP $-2
BS 0X0D         , 4             ; Keep SSE at 1 to wait for
                                  SCK signal in order to
                                  shift data
```

```
BC  0X03        , 2

MOV A           , 0X0A
MOV 0X06        , A             ; Read master's data from
                                ; read buffer
XOR A           , @0XAA         ; Check pass signal from
                                ; Read buffer
JBS 0X03        ,2
JMP $-6
JMP SPI

ORG 0X30
INIT:
CLRA
IOW 0X05
IOW 0X06
MOV 0x05        , A
MOV 0X06        , A
MOV A           , @0XFF
IOW 0X08
MOV A           , @0B11001111   ; Set WDT prescaler
CONTW
MOV A           , @0B00010001   ; Disable wake-up function
IOW 0X0E
MOV A           , @0B00000010   ; Enable external interrupt
IOW 0XF
ENI
MOV A           , @0B00110111
IOW 0x09
BC  0X3F        , 1             ; Clear RBFIF flag
NOP
JBS 0X3F        , 1             ; Polling loop for checking
                                ; interrupt occurrences
JMP $-2
JMP INTERRUPT

SPI:
BS 0X0D         , 4             ; Keep SSE enabled as
                                ; long as possible
WDTC
```

```
MOV A          , @0X0F          ; Show a signal when
                                  entering
                                ; SPI loop
MOV 0X06       , A
JBC 0X08       , 1              ; Choose P81 as a signal
                                ; button
JMP SPI
MOV A          , @0X5A          ; Move 5A into write buffer
                                ; when P81 button is pushed
MOV 0X0B       , A
NOP
JBC 0X0D       , 4              ; Polling loop for checking
                                ; SPI transmission completed
JMP $-2
BS 0XD         , 4
NOP
NOP
MOV A          , @0XF0          ; Display at Port6 when P81
                                  button is pushed
MOV 0X06       , A
MOV A          , @0X00          ; Send a signal to master to
                                ; prevent infinite loop
MOV 0X0B       , A
NOP
JBC 0X0D       , 4
JMP $-2
BS 0X0D        , 4
BS 0x0C        , 7
BC 0x0C        , 1
NOP
JMP SPI
DELAY:
                                ; (User's program)
EOP
ORG 0XFFF
JMP INITI
```

6.14 Oscillator

6.14.1 Oscillator Modes

The device can be operated in four different oscillator modes, such as Internal RC oscillator mode (IRC), External RC oscillator mode (ERC), High Crystal oscillator mode (HXT), and Low Crystal oscillator mode (LXT). User can select one of such modes by programming OSC2, OCS1 and OSC0 in the Code Option register. Table11 depicts how these four modes are defined.

The up-limited operation frequency of the crystal/resonator on the different VDD is listed in Table 11:

Table 11 Oscillator Modes defined by OSC2 ~ OSC0

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode)	0	0	0
HXT (High Crystal oscillator mode)	0	0	1
LXT1 (Low Crystal 1 oscillator mode)	0	1	0
LXT2 (Low Crystal 2 oscillator mode)	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

In LXT, XT, HXT and ERC mode, OSCI and OSCO are used, they cannot be used as normal I/O pins.

In IRC mode, P55 is used as normal I/O pin.

NOTE

1. Frequency range of HXT mode is 16 MHz ~ 6 MHz.
2. Frequency range of XT mode is 6 MHz ~ 1 MHz.
3. Frequency range of LXT1 mode is 1 MHz ~ 100kHz.
4. Frequency range of XT mode is 32kHz.

Table 12 Summary of Maximum Operating Speeds

Conditions	VDD	Max Fxt. (MHz)
Two cycles with two clocks	2.5	4.0
	3.0	8.0
	5.0	16.0

6.14.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78F652N can be driven by an external clock signal through the OSCI pin as shown in Figure 6-34 below.

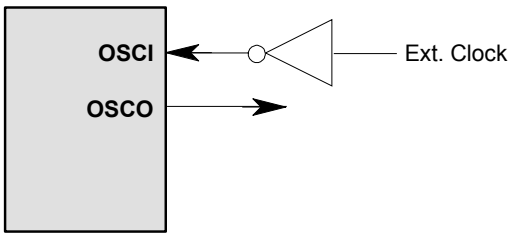


Figure 6-34 Circuit for External Clock Input

In most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Figure 6-35 depicts such circuit. The same thing applies whether it is in the HXT mode or in the LXT mode. Table 13 provides the recommended values of C1 and C2. Since each resonator has its own attribute, user should refer to its specification for appropriate values of C1 and C2. RS, a serial resistor, may be necessary for AT strip cut crystal or low frequency mode.

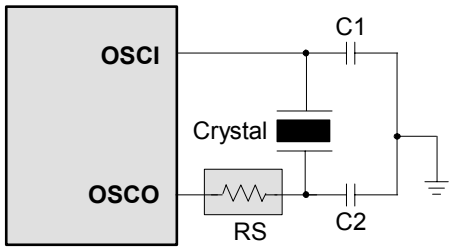


Figure 6-35 Circuit for Crystal/Resonator

Table 13 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100K~1MHz)	100kHz	45pF	45pF
		200kHz	20pF	20pF
		455kHz	20pF	20pF
		1.0 MHz	20pF	20pF
	HXT2 (1M~6MHz)	1.0 MHz	25pF	25pF
		2.0 MHz	20pF	20pF
		4.0 MHz	20pF	20pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768kHz	40pF	40pF
	LXT1 (100K~1MHz)	100kHz	45pF	45pF
		200kHz	20pF	20pF
		455kHz	20pF	20pF
		1.0 MHz	20pF	20pF
	XT (1~6 MHz)	455kHz	30pF	30pF
		1.0 MHz	20pF	20pF
		2.0 MHz	20pF	20pF

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
		4.0 MHz	20pF	20pF
		6.0 MHz	20pF	20pF
	HXT (6~16 MHz)	6.0 MHz	25pF	25pF
		8.0 MHz	20pF	20pF
		10.0 MHz	20pF	20pF
		12.0 MHz	20pF	20pF
		16.0 MHz	15pF	15pF

6.14.3 External RC Oscillator Mode

For some applications that do not need a very precise timing calculation, the RC oscillator (Figure 6-36) offers a cost-effective oscillator configuration. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variation.

In order to maintain a stable system frequency, the values of the Cext should not be less than 20pF, and that the value of Rext should not be greater than 1 MΩ. If they cannot be kept in this range, the frequency is easily affected by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator becomes unstable since the NMOS cannot discharge correctly the current of the capacitance.

Based on the above reasons, it must be kept in mind that all of the supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the PCB layout, will affect the system frequency.

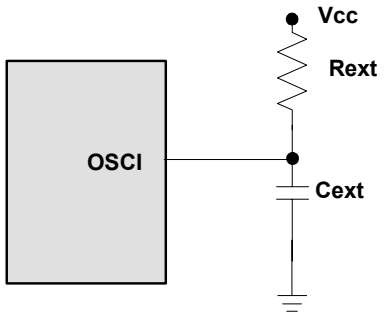


Figure 6-36 Circuit for External RC Oscillator Mode

Table 14 RC Oscillator Frequencies

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140kHz	140kHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850kHz	820kHz
	10k	450kHz	450kHz
	100k	48kHz	50kHz
300 pF	3.3k	560kHz	540kHz
	5.1k	370kHz	360kHz
	10k	196kHz	192kHz
	100k	20kHz	20kHz

Note: [1]: Measured based on DIP packages.

[2]: The values are for design reference only.

6.14.4 Internal RC Oscillator Mode

EM78F652N offers a versatile internal RC mode with default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (3.58MHz, 12MHz and 455kHz) that can be set by Code Option (Word 1), RCM1 and RCM0. All these four main frequencies can be calibrated by programming the Code Option (Word 1) bits, C4~C0. Table 16 describes a typical instance of the calibration.

Table 15 Internal RC Drift Rate (Ta=25°C, VDD=5 V± 5%, VSS=0V)

Internal RC	Drift Rate			
	Temperature (-40°C~85°C)	Voltage (2.3V~5.5V)	Process	Total
12MHz	± 5%	± 5%	± 5%	± 15%
4MHz	± 5%	± 5%	± 3%	± 13%
3.58MHz	± 5%	± 5%	± 5%	± 15%
455kHz	± 5%	± 5%	± 5%	± 15%

Table 16 Calibration Selections for Internal RC Mode

C4	C3	C2	C1	C0	*Cycle Time (ns)	*Frequency (MHz)
1	1	1	1	1	399	2.506
1	1	1	1	0	385	2.6
1	1	1	0	1	371	2.693
1	1	1	0	0	358	2.786
1	1	0	1	1	347	2.879
1	1	0	1	0	336	2.973
1	1	0	0	1	326	3.066
1	1	0	0	0	316	3.159
0	1	1	1	1	307	3.253
0	1	1	1	0	298	3.346
0	1	1	0	1	290	3.439
0	1	1	0	0	283	3.533
0	1	0	1	1	275	3.626
0	1	0	1	0	268	3.719
0	1	0	0	1	262	3.813
0	1	0	0	0	256	3.906
0	0	0	0	0	250	4.00
0	0	0	0	1	244	4.093
0	0	0	1	0	238	4.186
0	0	0	1	1	233	4.279
0	0	1	0	0	228	4.373
0	0	1	0	1	223	4.466
0	0	1	1	0	219	4.559
0	0	1	1	1	214	4.653
1	0	0	0	0	210	4.746
1	0	0	0	1	206	4.839
1	0	0	1	0	202	4.933
1	0	0	1	1	198	5.026
1	0	1	0	0	195	5.119
1	0	1	0	1	191	5.213
1	0	1	1	0	188	5.306
1	0	1	1	1	185	5.4

Note: * 1.Theoretical values are for reference only. It depends on the process.

2. Similar way of calculation is also applicable for low frequency mode.

6.15 Code Option Register

The EM78F652N has a Code option word that is not part of the normal program memory. The option bits cannot be accessed during normal program execution.

Code Option Register and Customer ID Register arrangement distribution:

Word 0	Word 1	Word 2
Bit 12~Bit 0	Bit 12~Bit 0	Bit 12~Bit 0

6.15.1 Code Option Register (Word 0)

Word 0													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	NRM	NRHL	NRE	CYES	CLKS1	CLKS0	ENWDTB	OSC2	OSC1	OSC0	Protect		
1	MOD2	8/fc	Disable	1cycle	High	High	Enable	High	High	High	Enable		
0	MOD1	32/fc	Enable	2cycles	Low	Low	Disable	Low	Low	Low	Disable		

Bit 12 (NRM): Noise rejection mode

1 : Noise reject mode 2, For multi-time circuit using, such as key scan and LED output

0 : Noise reject mode 1. For General input or output using. (Default)

Bit 11 (NRHL): Noise rejection high/low pulse define bit. INT pin is falling edge trigger.

1 : Pulses equal to 8/fc [s] is regarded as signal

0 : Pulses equal to 32/fc [s] is regarded as signal (default)

NOTE

The noise rejection function is turned off in the LXT2 and sleep mode.

Bit 10 (NRE): Noise rejection enable (depend on EM78F652N). INT pin is falling edge trigger.

1 : disable noise rejection

0 : enable noise rejection (default) but in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled

Bit 9 (CYES): Instruction cycle selection bit

1 : one instruction cycle

0 : two instruction cycles (default,ICE652 only)

Bit 8 ~ Bit 7 (CLKS1 ~ CLKS0): Instruction period option bit

Instruction Period	CLKS1	CLKS0
4 clocks	0	0
2 clocks	0	1
8 clocks	1	0
16 clocks	1	1

Refer to the Instruction Set section.

Bit 6 (ENWDTB): Watchdog timer enable bit

1 : Enable

0 : Disable

Bit 5 ~ Bit 3 (OSC2 ~ OSC0): Oscillator Mode Selection bits

Oscillator Modes defined by OSC2 ~ OSC0

Mode	OSC2	OSC1	OSC0
XT (Crystal oscillator mode)	0	0	0
HXT (High Crystal oscillator mode)	0	0	1
LXT1 (Low Crystal 1 oscillator mode)	0	1	0
LXT2 (Low Crystal 2 oscillator mode)	0	1	1
IRC mode, OSCO (P54) act as I/O pin	1	0	0
IRC mode, OSCO (P54) act as RCOUT pin	1	0	1
ERC mode, OSCO (P54) act as I/O pin	1	1	0
ERC mode, OSCO (P54) act as RCOUT pin	1	1	1

NOTE

1. Frequency range of HXT mode is 16 MHz ~ 6 MHz.

2. Frequency range of XT mode is 6 MHz ~ 1 MHz.

3. Frequency range of LXT1 mode is 1 MHz ~ 100kHz.

4. Frequency range of LXT2 mode is 32kHz.

Bits 2 ~ 0 (Protect): Protect Bit

Protect are protect bits, protect type are as follows:

0 : Disable

1 : Enable

6.15.2 Code Option Register (Word 1)

Word 1													
Bit	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonic	–	TCEN	–	–	C4	C3	C2	C1	C0	RCM1	RCM0	LVR1	LVR0
1	–	TCC	–	–	High	High	High	High	High	High	High	High	High
0	–	P77	–	–	Low	Low	Low	Low	Low	Low	Low	Low	Low

Bit 12: Not used, set to "1" at all time

Bit 11 (TCEN): TCC enable bit

0 : P77/TCC is set to be P77

1 : P77/TCC is set to be TCC

Bit 10 ~ Bit 9: Not used, set to "1" at all time

Bit 8 ~ Bit 4 (C4 ~ C0): Internal RC mode calibration bits. C4 ~ C0 must be set to "0" only (auto-calibration).

Bit 3 ~ Bit 2 (RCM1 ~ RCM0): RC mode selection bits

RCM 1	RCM 0	*Frequency (MHz)
0	0	4
0	1	12
1	0	3.58
1	1	455kHz

Bit 1 ~ Bit 0 (LVR1 ~ LVR0): Low Voltage Reset Enable bits

LVR1	LVR0	Reset Level	Release Level
0	0	NA	NA
0	1	2.7V	2.9V
1	0	3.5V	3.7V
1	1	4.0V	4.2V

LVR1, LVR0="0, 1"： LVR disable, power- on reset point of EM78F652N is 2.0V.

LVR1, LVR0="0, 1"： If Vdd < 2.9V, the EM78F652N will be reset.

LVR1, LVR0="1, 0"： If Vdd < 3.7V, the EM78F652N will be reset.

LVR1, LVR0="1, 1"： If Vdd < 4.2V, the EM78F652N will be reset.

6.15.3 Customer ID Register (Word 2)

Bit 12~Bit 0
XXXXXXXXXXXXX

Bits 12~0: Customer's ID code

6.16 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stays has stabilized. The EM78F652N has an on-chip Power-on Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd can rise quick enough (50 ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.17 External Power-on Reset Circuit

The circuit shown in Figure 6-37 uses an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is ±5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) functions as a short circuit at the moment of power down.

The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

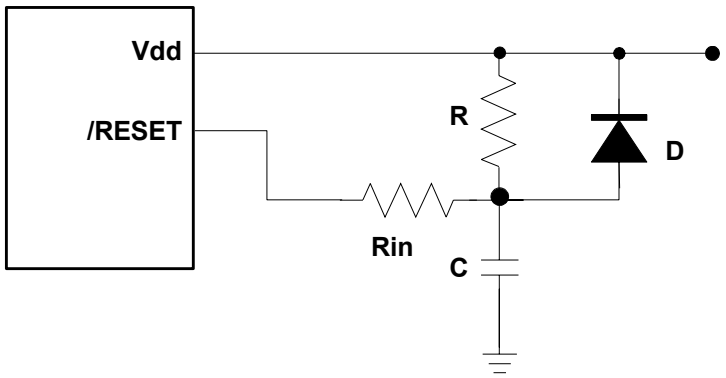


Figure 6-37 External Power-up Reset Circuit

6.18 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-38 and Figure 6-39 show how to build a residue-voltage protection circuit.

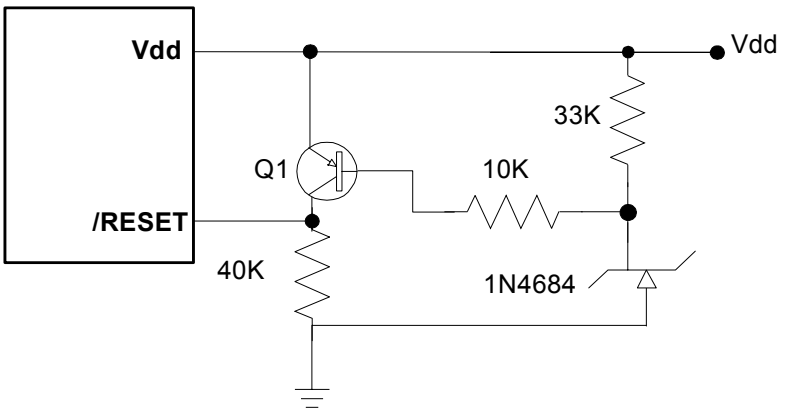


Figure 6-38 Residue Voltage Protection Circuit 1

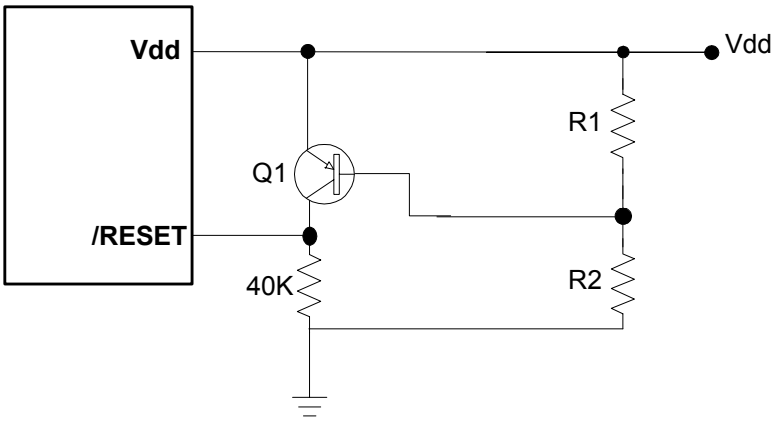


Figure 6-39 Residue Voltage Protection Circuit 2

6.19 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g. "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows:

(A) Change one instruction cycle to consist of four oscillator periods.

(B) "JMP", "CALL", "RET", "RETL", "RETI", or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

Case (A) is selected by the Code Option bit, called CLK. One instruction cycle consists of two oscillator clocks if CLK is low, and four oscillator clocks if CLK is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLK=Fosc/4, instead of Fosc/2 as indicated in Figure 6-10.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None [1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None [1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z, C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z, C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None

Binary Instruction	Hex	Mnemonic	Operation	Status Affected
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None [2]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None [3]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → [SP], (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z, C, DC
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC
1 1110 1000 kkkk	1E8k	PAGE k	K → R5(7:5)	None
1 1110 1001 000k	1E9k	BANK k	K → R3(7:6)	None

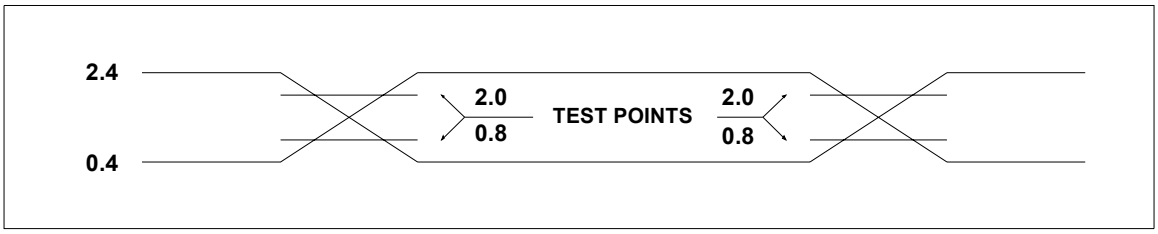
Note: [1] This instruction is applicable to IOC5~IOC7, IOCA ~ IOCF only.

[2] This instruction is not recommended for interrupt status register operation.

[3] This instruction can't operate under interrupt status register.

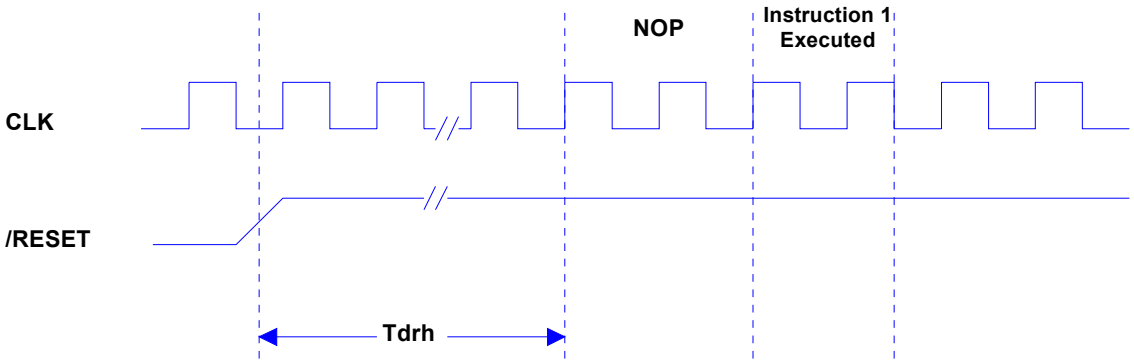
7 Timing Diagrams

AC Test Input/Output Waveform

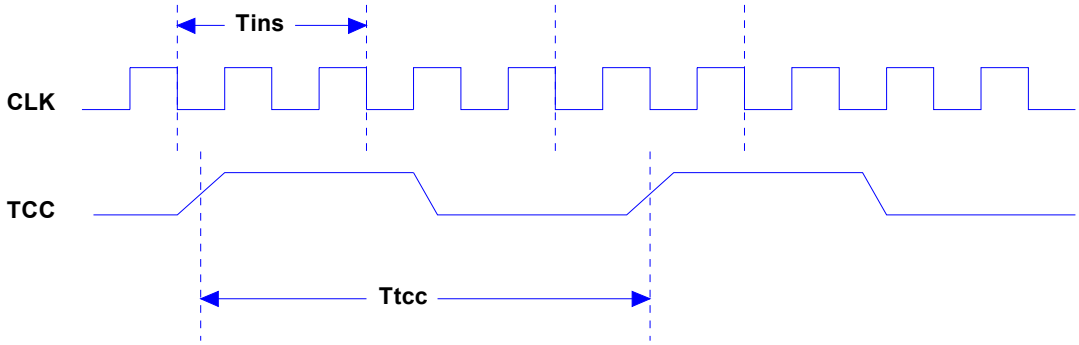


AC Testing : Input is driven at 2.4V for logic "1",and 0.4V for logic "0".Timing measurements are made at 2.0V for logic "1",and 0.8V for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



8 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Working voltage	2.2	to	5.5V
Working frequency	DC	to	16MHz*
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V

Note: These parameters are theoretical values and have not been tested.

9 DC Electrical Characteristic

Ta=25 °C, VDD=5.0V±5%, VSS=0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Fxt	Crystal: VDD to 3V	Two cycle with two clocks	DC	–	8	MHz
	Crystal: VDD to 5V		DC	–	16	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	830	F±30%	kHz
	IRC: VDD to 5 V	4MHz, 3.58MHz, 455kHz, 12MHz	F±30%	F	F±30%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–	–	±1	μA
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	3.5	–	V
IERC1	Sink current	VI from low to high, VI=5V	21	22	23	mA
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	1.5	–	V
IERC2	Sink current	VI from high to low, VI=2V	16	17	18	mA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6	0.75Vdd	–	Vdd+0.3V	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6	-0.3V	–	0.25Vdd	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	0.75Vdd	–	Vdd+0.3V	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	-0.3V	–	0.25Vdd	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	0.75Vdd	–	Vdd+0.3V	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-0.3V	–	0.25Vdd	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.0	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.8	–	V
IOH1	Output High Voltage (Ports 5, 6)	VOH = VDD-0.5V (IOH =3.7mA)	–	-3.5	–	mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IOL1	Output Low Voltage (Ports 5, 7)	VOL = GND+0.5V	–	10	–	mA
IOL2	Output Low Voltage (Ports 6)	VOL = GND+0.5V	–	18	–	mA
IPH	Pull-high current	Pull-high active, Input pin at VSS	-50	-75	-240	μA
IPL	Pull-low current	Pull-low active, Input pin at Vdd	25	40	120	μA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	–	2.0	μA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	–	8	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT disabled, HLP=1	–	–	35	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled, HLP=1	–	–	39	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=455kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled, HLP=0	–	–	270	μA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=455kHz (IRC type, CLKS="0"), Output pin floating, WDT enabled, HLP=0	–	–	640	μA
ICC5	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	–	1.5	mA
ICC6	Operating supply current at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled	–	–	3	mA

Note: These parameters are theoretical values and have not been tested.

* Data in the Minimum, Typical, Maximum (“Min”, “Typ”, ”Max”) columns are based on characterization results at 25°C. This data is for design guidance only and is not tested.

LVD (Low Voltage Detector) Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VHLVD	High Voltage LVD level	Vdd=5V, 4MHz	4.3	4.5	4.7	V
VHRESET	High Voltage Reset level	Vdd=5V, 4MHz	3.8	4.0	4.2	V
VMLVD	Medium Voltage LVD level	Vdd=5V, 4MHz	3.8	4.0	4.2	V
VMRESET	Medium Voltage Reset level	Vdd=5V, 4MHz	3.3	3.5	3.7	V
VLLVD	Low Voltage LVD level	Vdd=5V, 4MHz	3.1	3.3	3.5	V
VLRESET	Low Voltage Reset level	Vdd=5V, 4MHz	2.5	2.7	2.9	V

Data EEPROM Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 2.2V~ 5.5V Temperature = -40°C ~ 85°C	–	6	–	ms
Treten	Data Retention		–	10	–	Years
Tendu	Endurance time		–	100K	–	Cycles

Program Flash memory Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tprog	Erase/Write cycle time	Vdd = 5.0V Temperature = -40°C ~ 85°C	–	4	–	ms
Treten	Data Retention		–	10	–	Years
Tendu	Endurance time		–	100K	–	Cycles

A/D Converter Characteristics (Vdd=2.5V to 5.5V, Vss=0V, Ta=25°C)

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	$V_{AREF} - V_{ASS} \geq 2.5V$	2.5	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	Vdd=VAREF=5.0V, VASS =0.0V (V reference from Vdd)	750	850	1000	μA
	Ivref			-10	0	+10	μA
IAI2	Ivdd	Analog supply current	Vdd=VAREF=5.0V, VASS =0.0V (V reference from VREF)	500	600	820	μA
	IVref			200	250	300	μA
IOP		OP current	Vdd=5.0V, OP used Output voltage swing 0.2V to 4.8V	450	550	650	μA
RN		Resolution	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	10	11	–	Bits
LN		Linearity error	Vdd = 2.5 to 5.5V Ta=25°C	0	±4	±8	LSB
DNL		Differential nonlinear error	Vdd = 2.5 to 5.5V Ta=25℃	0	±0.5	±0.9	LSB

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FSE	Full scale error	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	±0	±4	±8	LSB
OE	Offset error	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	±0	±2	±4	LSB
ZAI	Recommended impedance of analog voltage source	–	0	8	10	KΩ
TAD	A/D clock period	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	4	–	–	us
TCN	A/D conversion time	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	14	–	14	TAD
ADIV	A/D OP input voltage range	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	0	–	V_{AREF}	V
ADOV	A/D OP output voltage swing	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V,RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
ADSR	A/D OP slew rate	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	0.1	0.3	–	V/us
PSR	Power Supply Rejection	Vdd=5.0V±0.5V	±0		±2	LSB

Note: [1] These parameters are theoretical values and have not been tested. Such parameters are for design reference only.
[2] When A/D is off, no current is consumed other than minor leakage current.
[3] The A/D conversion result does not decrease with an increase in the input voltage, and there's no missing code.
[4] Specifications are subject to change without prior notice.

9.1 OP Amplifier Electrical Characteristic

9.1.1 Absolute Maximum Rating

Parameter	Symbol	Limit	Unit	Comment
Supply Voltage	VDD	5	V	-
Input Voltage	VIN	VSS-0.3~VDD+0.3	V	-
Differential Input Voltage	VID	VDD-VSS	V	-
Power Consumption	ICON	10μ	A	-
Operating Temperature Range	TOP	-45~80	Celsius	-

9.1.2 Operational Amplifier

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Comment
VI	Input Voltage Range	Vdd = 5V	0	–	5	V	–
VO	Output Voltage Swing	Vdd =5V, RL=10KΩ	0.1	–	4.9	V	Vss-0.1~Vdd+0.1
PSRR	Power-Supply Rejection Ration For OP	Vdd= 5V	50	60	70	dB	–
CMRR	Common Mode Rejection Ratio	Vdd= 5V Vcm=0V~3.5V	–	75	–	dB	–
Vio	Input Offset Voltage	–	–	10	20	mV	–
Iio	Input Offset Current	–	–	–	0.1	μA	–

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Comment
Ibc	Input Bias Current	–	–	–	0.5	μA	–
Av	Voltage Gain	RL ≥ 15KΩ, (open loop voltage gain)	–	–	80	dB	–
SR	Slew Rate	–	0.1	0.2	–	V/μs	–
Tr	Transient Response	RL=2KΩ, CL=100pF	–	300	600	ns	–
GBW	Gain Bandwidth Product	–	–	1.0	–	MHz	–

9.1.3 Programmable Gain Amplifier

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Comment
IVR	Input Voltage Range	Vdd = 5V	0	–	5	V	–
OVS	Output Voltage Swing	Vd =3.3V, RL=10KΩ	0.1	–	4.9	V	–
PSRR	Power-Supply Rejection Ration For OP	Vdd= 5V	50	60	70	dB	–
Av	Voltage Gain	RL ≥ 15KΩ, (open loop voltage gain)	–	10 25 50 100	–	V/V	–
Vio	Input Offset Voltage	–	–	–	15	mV	–
Fro	Gain Error	Gain=40	–	–	+-15	%	–
Fo	Cutoff Frequency	–	–	100		kHz	–

10 AC Electrical Characteristic

EM78F652N, 0°C ≤ Ta ≤ 70°C, VDD=5V, VSS=0V

-40°C ≤ Ta ≤ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

Note: These parameters are theoretical values and have not been tested. Such parameters are for design reference only. Data in the Minimum, Typical, Maximum (“Min”, “Typ”, ”Max”) columns are based on characterization results at 25°C.

*N = selected prescaler ratio

APPENDIX

A Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM78F652ND16J/S	PDIP	16	300 mil
EM78F652NSO16J/S	SOP	16	300 mil
EM78F652ND18J/S	PDIP	18	300 mil
EM78F652NSP18J/S	SOP	18	300 mil
EM78F652ND20J/S	PDIP	20	300 mil
EM78F652NSO20J/S	SOP	20	300 mil

Green products do not contain hazardous substances.

The third edition of Sony SS-00259 standard.

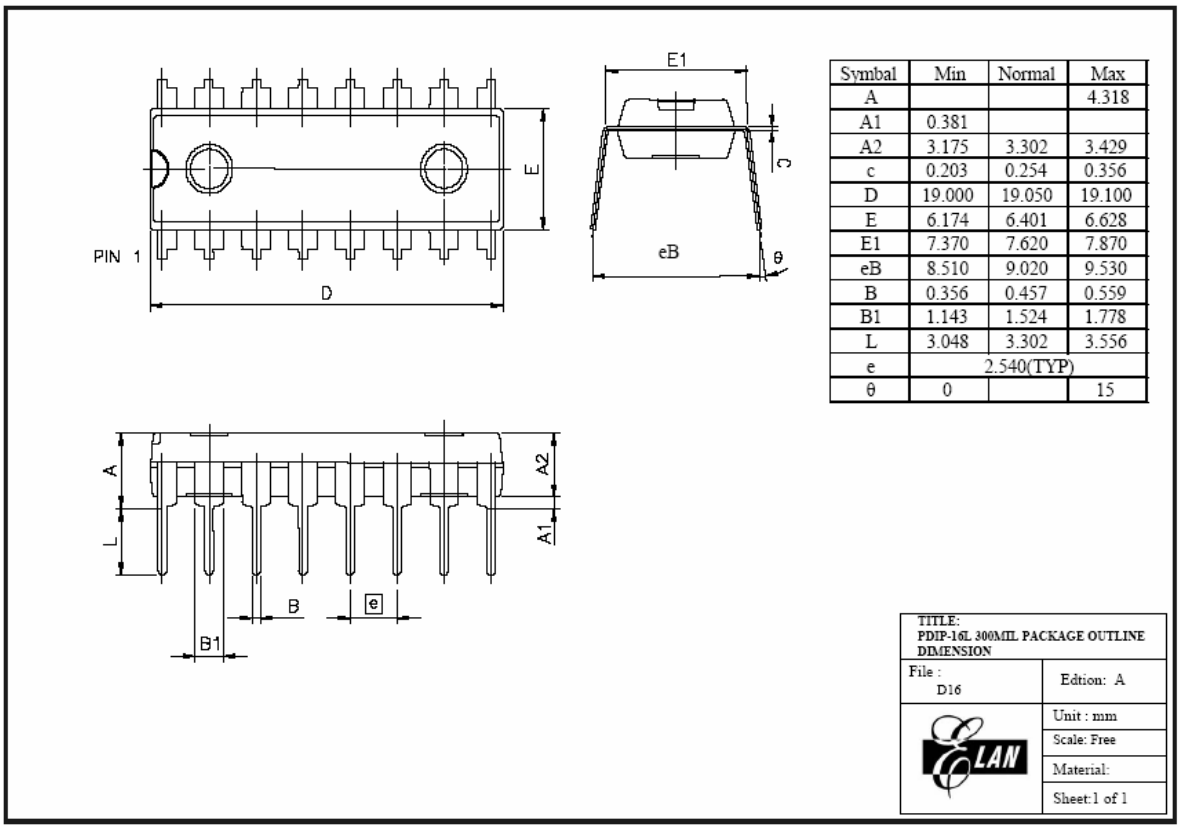
Pb contents should be less the 100ppm

Pb contents comply with Sony specs.

Part no.	EM78F652NJ/S
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

B Package Information

B.1 EM78F652ND16

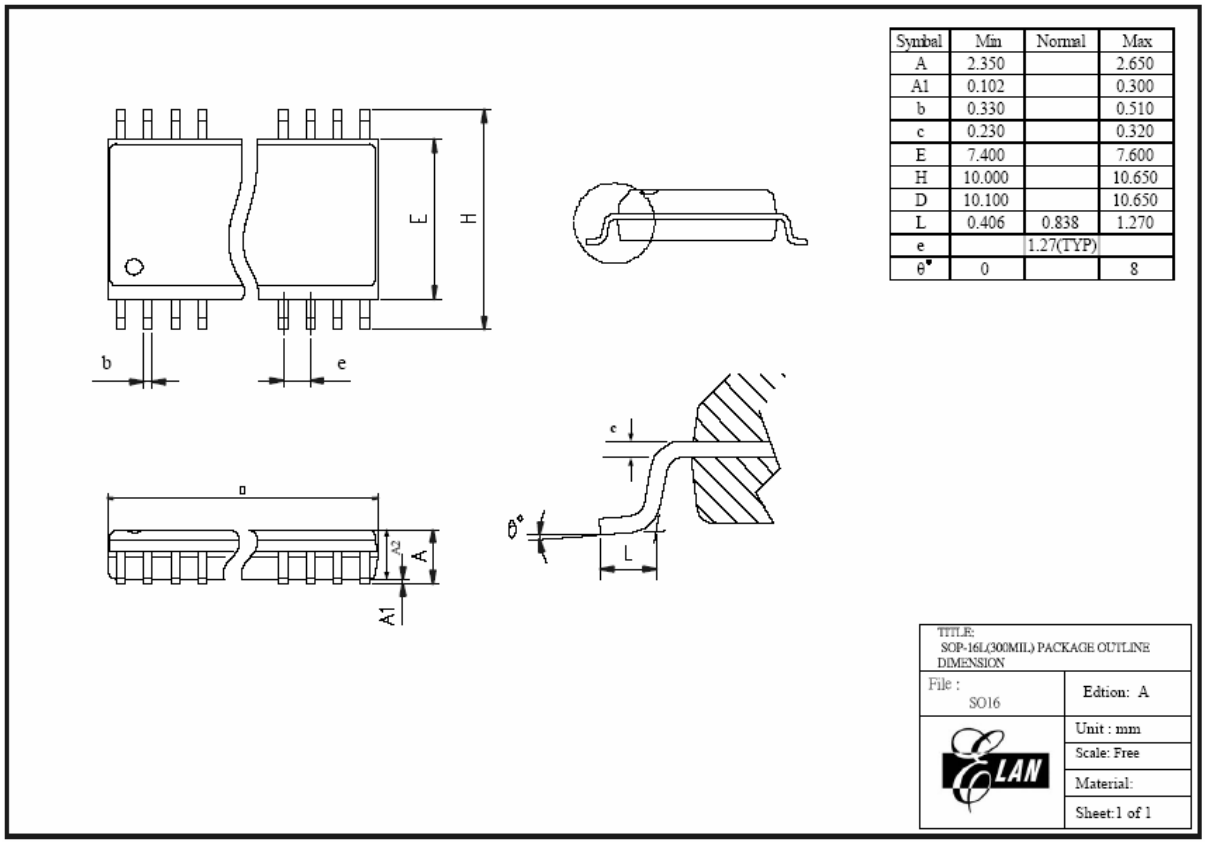


Symbal	Min	Normal	Max
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	19.000	19.050	19.100
E	6.174	6.401	6.628
E1	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-16L 300MIL PACKAGE OUTLINE DIMENSION	
File : D16	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure B-1 EM78F652N 16-pin DIP Package Typ

B.2 EM78F652NSO16



Symbol	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.330		0.510
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	10.100		10.650
L	0.406	0.838	1.270
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-16L(300MIL) PACKAGE OUTLINE DIMENSION

File : SO16 | Edition: A

Unit : mm

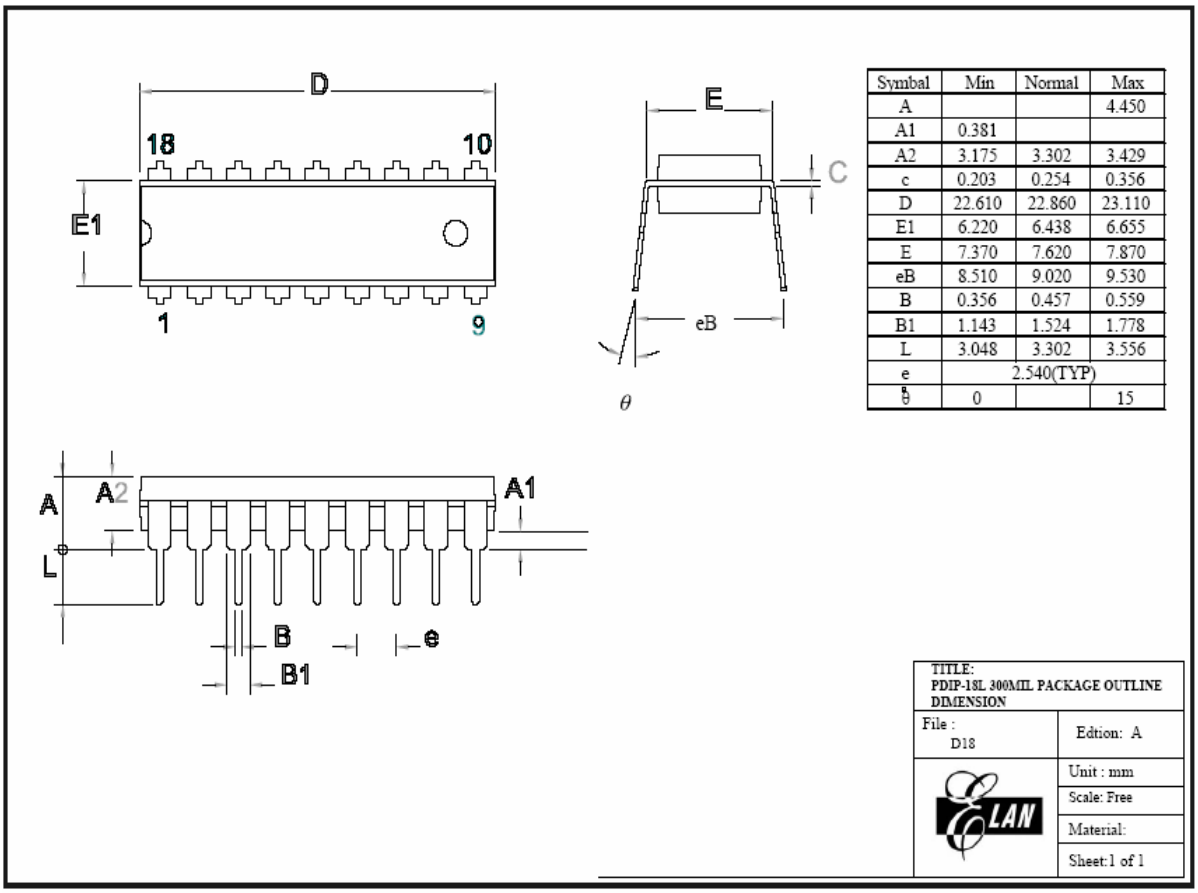
Scale: Free

Material:

Sheet:1 of 1

Figure B-2 EM78F652N 16-pin SOP Package Typ

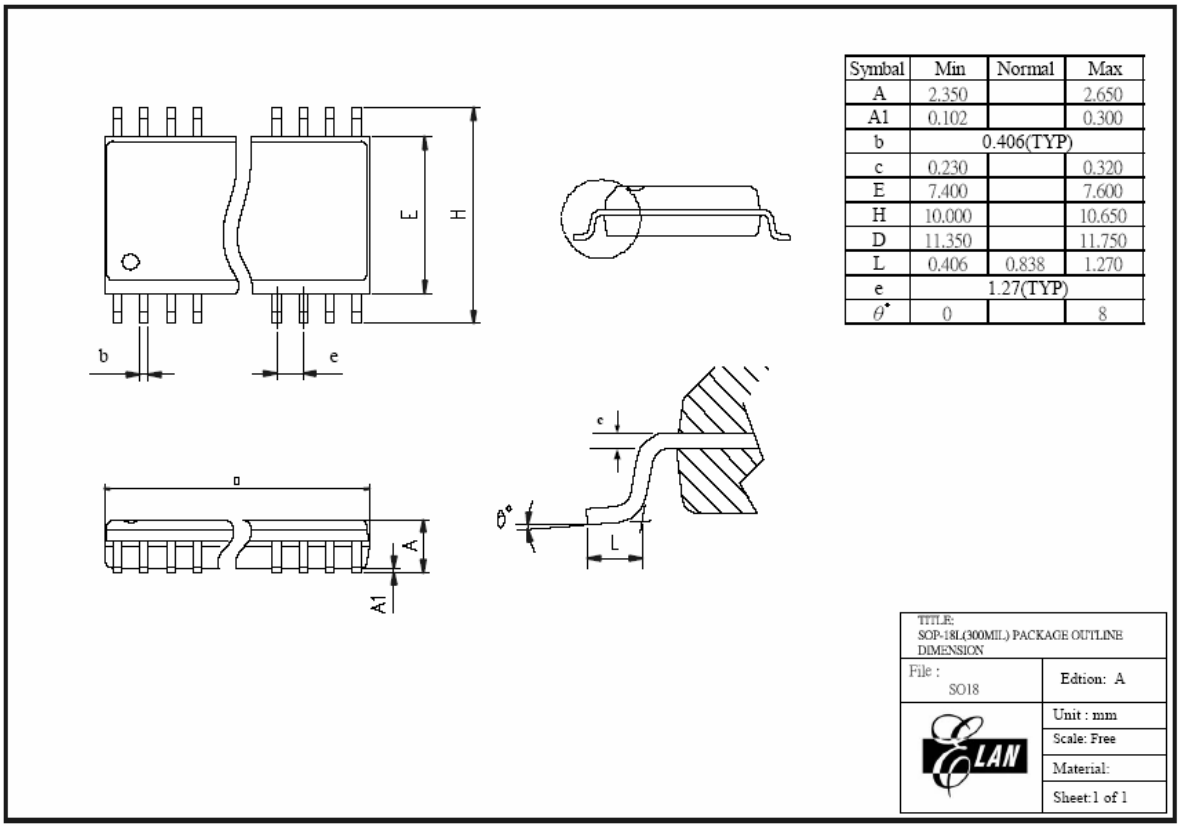
B.3 EM78F652ND18



Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

Figure B-3 EM78F652N 18-pin DIP Package Typ

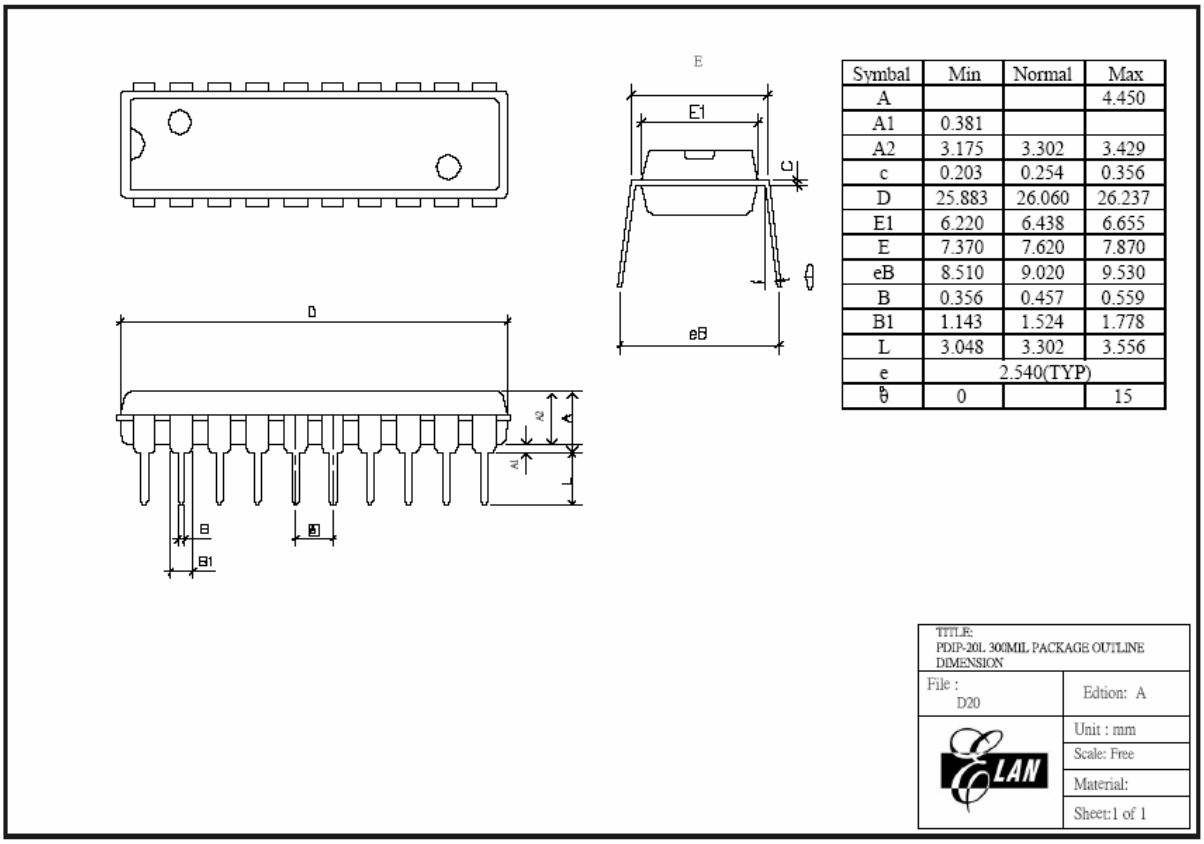
B.4 EM78F652NSO18



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	11.350		11.750
L	0.406	0.838	1.270
e		1.27(TYP)	
θ°	0		8

Figure B-4 EM78F652N 18-pin SOP Package Typ

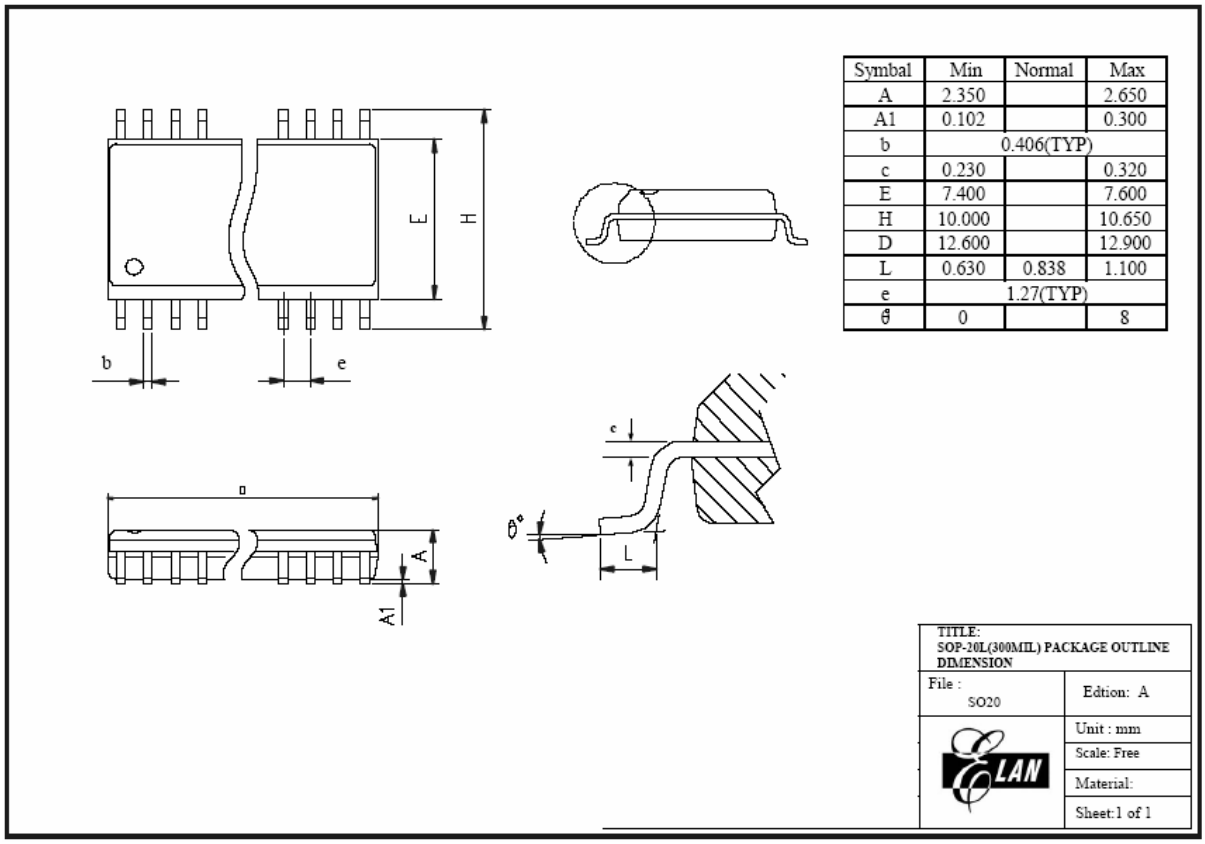
B.5 EM78F652ND20



Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	25.883	26.060	26.237
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ	0		15

Figure B-5 EM78F652N 20-pin DIP Package Typ

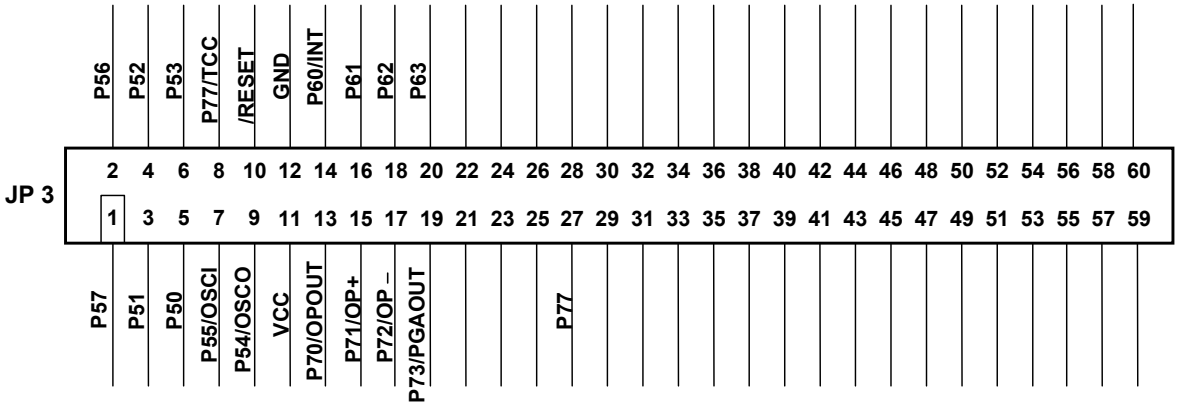
B.6 EM78F652NSO20



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b		0.406(TYP)	
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	12.600		12.900
L	0.630	0.838	1.100
e		1.27(TYP)	
θ	0		8

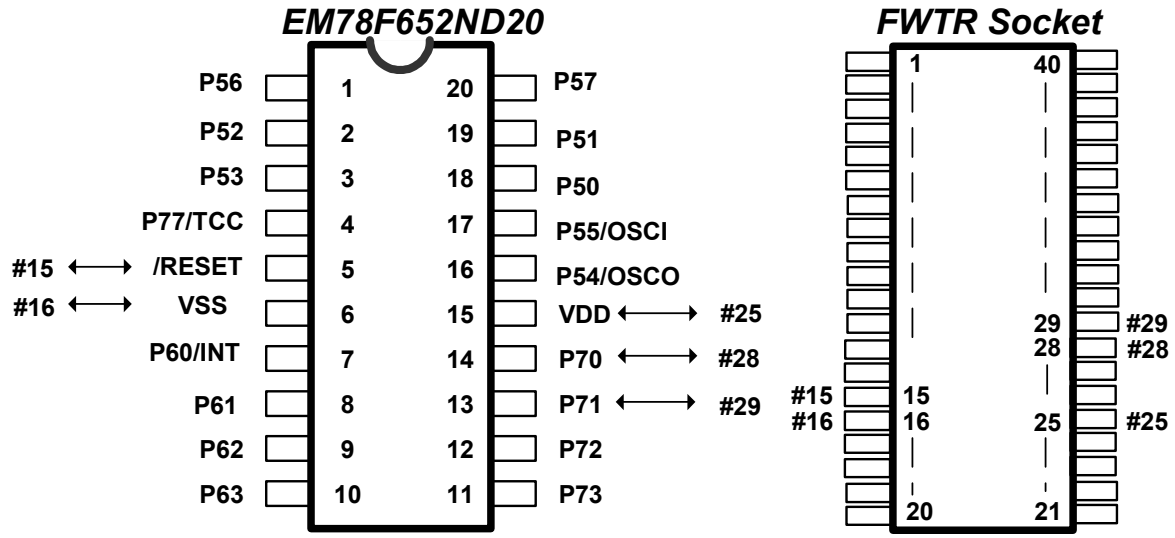
Figure B-6 EM78F652N 20-pin SOP Package Typ

C ICE 652N Output Pin Assignment (JP 3)



D EM78F652N Program Pin

In the following IC diagram, "Pin # number" means the Pin to be connected to the Socket in FWTR.



E Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature=245±5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15 mins)~150°C (1 5mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance)=24 hrs	
	Step 3: Soak at 30°C/60%, TD (endurance)=192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350mm^3 ----225±5°C) (Pkg thickness ≤ 2.5mm or Pkg volume ≤ 350mm^3 ----240±5°C)	
Temperature cycle test	-65°C (15 mins)~150°C (15 mins), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%, TD (endurance) = 168 , 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 150mA/20V	–
ESD (HBM)	TA=25°C, ≥ ± 3KV	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS (-) mode
ESD (MM)	TA=25°C, ≥ ± 300V	

E.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise-caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.