

ISO1042-Q1 Automotive Isolated CAN Transceiver With 70-V Bus Fault Protection and Flexible Data Rate

1 Features

- AEC Q100: Qualified for automotive applications
- Grade 1: -40°C to 125°C ambient temperature
- **Functional Safety-Capable**
 - [Documentation available to aid functional safety system design](#)
- Meets the ISO 11898-2:2016 physical layer standard
- Supports classic CAN up to 1 Mbps and FD (Flexible Data Rate) up to 5 Mbps
- Low loop delay: 152 ns
- Protection features
 - DC bus fault protection voltage: $\pm 70\text{ V}$
 - HBM ESD tolerance on bus pins: $\pm 16\text{ kV}$
 - Driver Dominant Time Out (TXD DTO)
 - Undervoltage protection on V_{CC1} and V_{CC2}
- Common-Mode Voltage Range: $\pm 30\text{ V}$
- Ideal passive, high impedance bus terminals when unpowered
- High CMTI: $100\text{ kV}/\mu\text{s}$
- V_{CC1} voltage range: 1.71 V to 5.5 V
 - Supports 1.8-V, 2.5-V, 3.3-V and 5.0-V logic interface to the CAN controller
- V_{CC2} Voltage Range: 4.5 V to 5.5 V
- Robust Electromagnetic Compatibility (EMC)
 - System-level ESD, EFT, and surge immunity
 - Low emissions
- 16-SOIC and 8-SOIC package options
- Industrial version available: [ISO1042](#)
- Safety-related certifications:
 - 7071- V_{PK} V_{IOTM} and 1500- V_{PK} V_{IORM} (Reinforced and Basic Options) per DIN VDE V 0884-11:2017-01
 - 5000- V_{RMS} Isolation for 1 Minute per UL 1577
 - CQC, TUV and CSA certifications

2 Applications

- [Starter/generator](#)
- [Battery Management System \(BMS\)](#)
- [DC/DC converter](#)
- [On-Board \(OBC\) & wireless charger](#)
- [Inverter & motor control](#)

3 Description

The ISO1042-Q1 device is a galvanically-isolated controller area network (CAN) transceiver that meets

the specifications of the ISO11898-2 (2016) standard. The ISO1042-Q1 device offers $\pm 70\text{-V}$ DC bus fault protection and $\pm 30\text{-V}$ common-mode voltage range. The device supports up to 5-Mbps data rate in CAN FD mode allowing much faster transfer of payload compared to classic CAN. This device uses a silicon dioxide (SiO_2) insulation barrier with a withstand voltage of 5000 V_{RMS} and a working voltage of 1060 V_{RMS} . Electromagnetic compatibility has been significantly enhanced to enable system-level ESD, EFT, surge, and emissions compliance. Used in conjunction with isolated power supplies, the device protects against high voltage, and prevents noise currents from the bus from entering the local ground. The ISO1042-Q1 device is available for both basic and reinforced isolation (see [Reinforced and Basic Isolation Options](#)). The ISO1042-Q1 device supports a wide ambient temperature range of -40°C to $+125^{\circ}\text{C}$. The device is available in the SOIC-16 (DW) package and a smaller SOIC-8 (DWV) package.

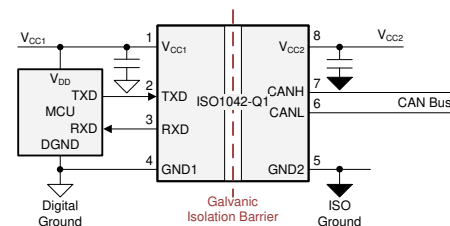
Device Information

| PART NUMBER ⁽¹⁾ | PACKAGE | BODY SIZE (NOM) |
|----------------------------|-----------|--------------------|
| ISO1042-Q1 | SOIC (8) | 5.85 mm × 7.50 mm |
| | SOIC (16) | 10.30 mm × 7.50 mm |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

Reinforced and Basic Isolation Options

| FEATURE | ISO1042x-Q1 | ISO1042Bx-Q1 |
|--------------------|--------------------------------|--------------------------------|
| Protection Level | Reinforced | Basic |
| Surge Test Voltage | 10000 V_{PK} | 6000 V_{PK} |
| Isolation Rating | 5000 V_{RMS} | 5000 V_{RMS} |
| Working Voltage | 1060 V_{RMS} / 1500 V_{PK} | 1060 V_{RMS} / 1500 V_{PK} |



Application Diagram



Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 Features | 1 | 8 Detailed Description | 20 |
| 2 Applications | 1 | 8.1 Overview..... | 20 |
| 3 Description | 1 | 8.2 Functional Block Diagram..... | 20 |
| 4 Revision History | 2 | 8.3 Feature Description..... | 20 |
| 5 Pin Configuration and Functions | 3 | 8.4 Device Functional Modes..... | 23 |
| 6 Specifications | 5 | 9 Application and Implementation | 25 |
| 6.1 Absolute Maximum Ratings..... | 5 | 9.1 Application Information..... | 25 |
| 6.2 ESD Ratings..... | 5 | 9.2 Typical Application..... | 25 |
| 6.3 Transient Immunity..... | 5 | 10 Power Supply Recommendations | 28 |
| 6.4 Recommended Operating Conditions..... | 5 | 11 Layout | 29 |
| 6.5 Thermal Information..... | 6 | 11.1 Layout Guidelines..... | 29 |
| 6.6 Power Ratings..... | 6 | 11.2 Layout Example..... | 29 |
| 6.7 Insulation Specifications..... | 7 | 12 Device and Documentation Support | 31 |
| 6.8 Safety-Related Certifications..... | 8 | 12.1 Documentation Support..... | 31 |
| 6.9 Safety Limiting Values..... | 8 | 12.2 Receiving Notification of Documentation Updates.. | 31 |
| 6.10 Electrical Characteristics - DC Specification..... | 10 | 12.3 Support Resources..... | 31 |
| 6.11 Switching Characteristics..... | 12 | 12.4 Trademarks..... | 31 |
| 6.12 Insulation Characteristics Curves..... | 13 | 12.5 Electrostatic Discharge Caution..... | 31 |
| 6.13 Typical Characteristics..... | 14 | 12.6 Glossary..... | 31 |
| 7 Parameter Measurement Information | 16 | 13 Mechanical, Packaging, and Orderable Information | 31 |
| 7.1 Test Circuits..... | 16 | | |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (January 2020) to Revision B (October 2020) | Page |
|--|-------------|
| • Added Functional Safety Bullets..... | 1 |

| Changes from Revision * (October 2018) to Revision A (January 2020) | Page |
|--|-------------|
| • Changed new safety certification..... | 1 |

5 Pin Configuration and Functions

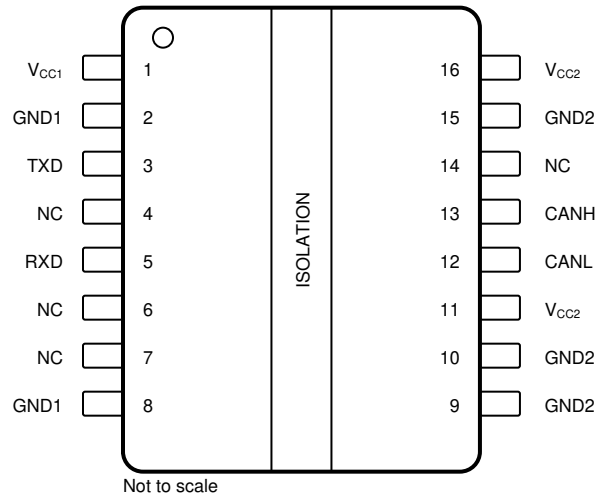


Figure 5-1. DW Package 16-Pin SOIC Top View

Table 5-1. Pin Functions—16 Pins

| PIN | | I/O | DESCRIPTION |
|-----|------------------|-----|--|
| NO. | NAME | | |
| 1 | V _{CC1} | — | Digital-side supply voltage, Side 1 |
| 2 | GND1 | — | Digital-side ground connection, Side 1 |
| 3 | TXD | I | CAN transmit data input (LOW for dominant and HIGH for recessive bus states) |
| 4 | NC | — | Not connected |
| 5 | RXD | O | CAN receive data output (LOW for dominant and HIGH for recessive bus states) |
| 6 | NC | — | Not connected |
| 7 | NC | — | Not connected |
| 8 | GND1 | — | Digital-side ground connection, Side 1 |
| 9 | GND2 | — | Transceiver-side ground connection, Side 2 |
| 10 | | | |
| 11 | V _{CC2} | — | Transceiver-side supply voltage, Side 2. Must be externally connected to pin 16. |
| 12 | CANL | I/O | Low-level CAN bus line |
| 13 | CANH | I/O | High-level CAN bus line |
| 14 | NC | — | Not connected |
| 15 | GND2 | — | Transceiver-side ground connection, Side 2 |
| 16 | V _{CC2} | — | Transceiver-side supply voltage, Side 2. Must be externally connected to pin 11. |

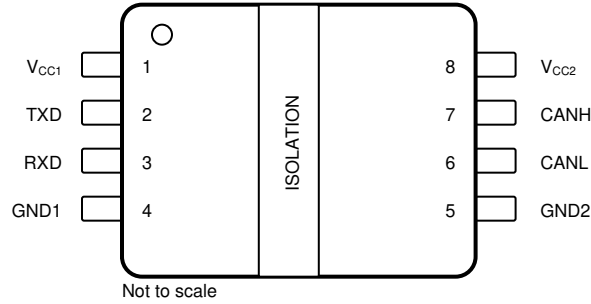


Figure 5-2. DWV Package 8-Pin SOIC Top View

Table 5-2. Pin Functions—8 Pins

| PIN | | I/O | DESCRIPTION |
|-----|------------------|-----|--|
| NO. | NAME | | |
| 1 | V _{CC1} | — | Digital-side supply voltage, Side 1 |
| 2 | TXD | I | CAN transmit data input (LOW for dominant and HIGH for recessive bus states) |
| 3 | RXD | O | CAN receive data output (LOW for dominant and HIGH for recessive bus states) |
| 4 | GND1 | — | Digital-side ground connection, Side 1 |
| 5 | GND2 | — | Transceiver-side ground connection, Side 2 |
| 6 | CANL | I/O | Low-level CAN bus line |
| 7 | CANH | I/O | High-level CAN bus line |
| 8 | V _{CC2} | — | Transceiver-side supply voltage, Side 2 |

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

| | | MIN | MAX | UNIT |
|-----------------------|--|------|--------------------------------------|------|
| V _{CC1} | Supply voltage, side 1 | -0.5 | 6 | V |
| V _{CC2} | Supply voltage, side 2 | -0.5 | 6 | V |
| V _{IO} | Logic input and output voltage range (TXD and RXD) | -0.5 | V _{CC1} +0.5 ⁽³⁾ | V |
| I _O | Output current on RXD pin | -15 | 15 | mA |
| V _{BUS} | Voltage on bus pins (CANH, CANL) | -70 | 70 | V |
| V _{BUS_DIFF} | Differential voltage on bus pins (CANH-CANL) | -70 | 70 | V |
| T _J | Junction temperature | -40 | 150 | °C |
| T _{STG} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
- (3) Maximum voltage must not exceed 6 V

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|---|--------------------------------------|--------|------|
| V _(ESD) | Electrostatic discharge Human body model (HBM), per ANSI/ ESDA/JEDEC JS-001 | All pins ⁽¹⁾ | ±6000 | V |
| | | CANH and CANL to GND2 ⁽¹⁾ | ±16000 | V |
| | Electrostatic discharge Charged device model (CDM), per JEDEC specification JESD22-C101 | All pins ⁽²⁾ | ±1500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Transient Immunity

| PARAMETER | TEST CONDITIONS | VALUE | UNIT | |
|--------------------|--|--|------|---|
| V _{PULSE} | ISO7637-2 Transients according to GIFT - ICT CAN EMC test specification | Pulse 1; CAN bus terminals (CANH, CANL) to GND2 | -100 | V |
| | | Pulse 2; CAN bus terminals (CANH, CANL) to GND2 | 75 | V |
| | | Pulse 3a; CAN bus terminals (CANH, CANL) to GND2 | -150 | V |
| | | Pulse 3b; CAN bus terminals (CANH, CANL) to GND2 | 100 | V |

6.4 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|------------------|--|------|------|------|
| V _{CC1} | Supply Voltage, Side 1, 1.8-V operation | 1.71 | 1.89 | V |
| | Supply Voltage, Side 1, 2.5-V, 3.3-V and 5.5-V operation | 2.25 | 5.5 | V |
| V _{CC2} | Supply Voltage, Side 2 | 4.5 | 5.5 | V |
| T _A | Operating ambient temperature | -40 | 125 | °C |

6.5 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | ISO1042-Q1 | | UNIT |
|-------------------------------|--|------------|------------|------|
| | | DW (SOIC) | DWV (SOIC) | |
| | | 16 PINS | 8 PINS | |
| R _{ΘJA} | Junction-to-ambient thermal resistance | 69.9 | 100 | °C/W |
| R _{ΘJC(top)} | Junction-to-case (top) thermal resistance | 31.8 | 40.8 | °C/W |
| R _{ΘJB} | Junction-to-board thermal resistance | 29.0 | 51.8 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 13.2 | 16.8 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 28.6 | 49.8 | °C/W |
| R _{ΘJC(bot)} | Junction-to-case (bottom) thermal resistance | - | - | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|---|-----|-----|-----|------|
| P _D | Maximum power dissipation (both sides) | See Figure 7-3 , V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, R _L = 50 Ω, A repetitive pattern on TXD with 1 ms time period, 990 μs LOW time, and 10 μs HIGH time. | | | 385 | mW |
| P _{D1} | Maximum power dissipation (side-1) | See Figure 7-5 , V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, R _L = 50 Ω, Input a 2-V pk-pk 2.5-MHz 50% duty cycle differential square wave on CANH-CANL | | | 25 | mW |
| P _{D2} | Maximum power dissipation (side-2) | See Figure 7-3 , V _{CC1} = V _{CC2} = 5.5 V, T _J = 150°C, R _L = 50 Ω, A repetitive pattern on TXD with 1 ms time period, 990 μs LOW time, and 10 μs HIGH time. | | | 360 | mW |

6.7 Insulation Specifications

| PARAMETER | | TEST CONDITIONS | SPECIFICATIONS | | UNIT |
|--|--|--|--------------------|--------------------|------------------|
| | | | DW-16 | DWV-8 | |
| IEC 60664-1 | | | | | |
| CLR | External clearance ⁽¹⁾ | Side 1 to side 2 distance through air | >8 | >8.5 | mm |
| CPG | External Creepage ⁽¹⁾ | Side 1 to side 2 distance across package surface | >8 | >8.5 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | >17 | >17 | μm |
| CTI | Comparative tracking index | IEC 60112; UL 746A | >600 | >600 | V |
| | Material Group | According to IEC 60664-1 | I | I | |
| | Overvoltage category | Rated mains voltage ≤ 600 V _{RMS} | I-IV | I-IV | |
| | | Rated mains voltage ≤ 1000 V _{RMS} | I-III | I-III | |
| DIN VDE V 0884-11:2017-01⁽²⁾ | | | | | |
| V _{IORM} | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 1500 | 1500 | V _{PK} |
| V _{IOWM} | Maximum isolation working voltage | AC voltage (sine wave); time-dependent dielectric breakdown (TDDb) test; | 1060 | 1060 | V _{RMS} |
| | | DC voltage | 1500 | 1500 | V _{DC} |
| V _{IOTM} | Maximum transient isolation voltage | V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production) | 7071 | 7071 | V _{PK} |
| V _{IOSM} | Maximum surge isolation voltage ISO1042-Q1 ⁽³⁾ | Test method per IEC 62368-1, 1.2/50 μs waveform, V _{TEST} = 1.6 × V _{IOSM} = 10000 V _{PK} (qualification) | 6250 | 6250 | V _{PK} |
| | Maximum surge isolation voltage ISO1042B-Q1 ⁽³⁾ | Test method per IEC 62368-1, 1.2/50 μs waveform, V _{TEST} = 1.3 × V _{IOSM} = 6000 V _{PK} (qualification) | 4615 | 4615 | V _{PK} |
| q _{pd} | Apparent charge ⁽⁴⁾ | Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s | ≤ 5 | ≤ 5 | pC |
| | | Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; ISO1042-Q1: V _{pd(m)} = 1.6 × V _{IORM} , t _m = 10 s; ISO1042B-Q1: V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s | ≤ 5 | ≤ 5 | |
| | | Method b1: At routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s; ISO1042-Q1: V _{pd(m)} = 1.875 × V _{IORM} , t _m = 1 s; ISO1042B-Q1: V _{pd(m)} = 1.5 × V _{IORM} , t _m = 1 s | ≤ 5 | ≤ 5 | |
| C _{IO} | Barrier capacitance, input to output ⁽⁵⁾ | V _{IO} = 0.4 × sin(2 πft), f = 1 MHz | 1 | 1 | pF |
| R _{IO} | Insulation resistance, input to output ⁽⁵⁾ | V _{IO} = 500 V, T _A = 25°C | > 10 ¹² | > 10 ¹² | Ω |
| | | V _{IO} = 500 V, 100°C ≤ T _A ≤ 150°C | > 10 ¹¹ | > 10 ¹¹ | |
| | | V _{IO} = 500 V at T _S = 150°C | > 10 ⁹ | > 10 ⁹ | |
| | Pollution degree | | 2 | 2 | |
| | Climatic category | | 40/125/21 | 40/125/21 | |
| UL 1577 | | | | | |
| V _{ISO} | Withstand isolation voltage | V _{TEST} = V _{ISO} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{ISO} , t = 1 s (100% production) | 5000 | 5000 | V _{RMS} |

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.

ISO1042-Q1

SLLSFA5B – OCTOBER 2018 – REVISED OCTOBER 2020

- (2) ISO1042-Q1 is suitable for *safe electrical insulation* and ISO1042B-Q1 is suitable for *basic electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

6.8 Safety-Related Certifications

| VDE | CSA | UL | CQC | TUV |
|---|---|--|--|---|
| Certified according to DIN VDE V 0884-11:2017- 01 | Certified according to IEC 60950-1, IEC 62368-1 and IEC 60601-1 | Recognized under UL 1577 Component Recognition Program | Certified according to GB4943.1-2011 | Certified according to EN 61010-1:2010/A1:2019, EN 60950-1:2006/A2:2013 and EN 62368-1:2014 |
| Maximum transient isolation voltage, 7071 V _{PK} ; Maximum repetitive peak isolation voltage, 1500 V _{PK} ; Maximum surge isolation voltage, ISO1042-Q1: 6250 V _{PK} (Reinforced) ISO1042B-Q1: 4615 V _{PK} (Basic) | CSA 60950-1-07+A1+A2, IEC 60950-1 2 nd Ed.+A1+A2 and IEC 62368-1 2 nd Ed., for pollution degree 2, material group I ISO1042-Q1: 800 V _{RMS} reinforced isolation ISO1042B-Q1: 1060 V _{RMS} basic isolation ----- CSA 60601- 1:14 and IEC 60601-1 Ed. 3.1+A1, ISO1042-Q1: 2 MOPP (Means of Patient Protection) 250 V _{RMS} (354 V _{PK}) maximum working voltage | Single protection, 5000 V _{RMS} | Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V _{RMS} maximum working voltage | EN 61010-1:2010 / A1:2019 ISO1042-Q1: 600 V _{RMS} reinforced isolation ISO1042B-Q1: 1000 V _{RMS} basic isolation ----- EN 60950-1:2006/A2:2013 and EN 62368-1:2014 ISO1042-Q1: 800 V _{RMS} reinforced isolation ISO1042B-Q1: 1060 V _{RMS} basic isolation |
| Certificates: Reinforced: 40040142 Basic: 40047657 | Master contract number: 220991 | File number: E181974 | Certificate: CQC15001121716 (DW-16) CQC18001199096 (DWW-8) | Client ID number: 77311 |

6.9 Safety Limiting Values

 Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|---|-----|-----|------|------|
| DW-16 PACKAGE | | | | | | |
| I _S | Safety input, output, or supply current | R _{θJA} = 69.9°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 6-1 | | | 325 | mA |
| | | R _{θJA} = 69.9°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 6-1 | | | 496 | |
| | | R _{θJA} = 69.9°C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 6-1 | | | 650 | |
| | | R _{θJA} = 69.9°C/W, V _I = 1.89 V, T _J = 150°C, T _A = 25°C, see Figure 6-1 | | | 946 | |
| P _S | Safety input, output, or total power | R _{θJA} = 69.9°C/W, T _J = 150°C, T _A = 25°C, see Figure 6-3 | | | 1788 | mW |
| T _S | Maximum safety temperature | | | | 150 | °C |
| DWW-8 PACKAGE | | | | | | |
| I _S | Safety input, output, or supply current | R _{θJA} = 100°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C, see Figure 6-2 | | | 227 | mA |
| | | R _{θJA} = 100°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C, see Figure 6-2 | | | 347 | |
| | | R _{θJA} = 100°C/W, V _I = 2.75 V, T _J = 150°C, T _A = 25°C, see Figure 6-2 | | | 454 | |
| | | R _{θJA} = 100°C/W, V _I = 1.89 V, T _J = 150°C, T _A = 25°C, see Figure 6-2 | | | 661 | |
| P _S | Safety input, output, or total power | R _{θJA} = 100°C/W, T _J = 150°C, T _A = 25°C, see Figure 6-4 | | | 1250 | mW |
| T _S | Maximum safety temperature | | | | 150 | °C |

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.10 Electrical Characteristics - DC Specification

Over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|----------------------|--------|----------------------|------|
| SUPPLY CHARACTERISTICS | | | | | | |
| I _{CC1} | Supply current Side 1 | V _{CC1} = 1.71 V to 1.89 V, TXD = 0 V, bus dominant | | 2.3 | 3.5 | mA |
| | | V _{CC1} = 2.25 V to 5.5 V, TXD = 0 V, bus dominant | | 2.4 | 3.5 | mA |
| | | V _{CC1} = 1.71 V to 1.89 V, TXD = V _{CC1} , bus recessive | | 1.2 | 2.1 | mA |
| | | V _{CC1} = 2.25 V to 5.5 V, TXD = V _{CC1} , bus recessive | | 1.3 | 2.1 | mA |
| I _{CC2} | Supply current Side 2 | TXD = 0 V, bus dominant, R _L = 60 Ω | | 43 | 73.4 | mA |
| | | TXD = V _{CC1} , bus recessive, R _L = 60 Ω | | 2.8 | 4.1 | mA |
| UV _{VCC1} | Rising under voltage detection, Side 1 | | | | 1.7 | V |
| UV _{VCC1} | Falling under voltage detection, Side 1 | | 1.0 | | | V |
| V _{HYS(UVCC1)} | Hysteresis voltage on V _{CC1} undervoltage lock-out | | 75 | 125 | | mV |
| UV _{VCC2} | Rising under voltage detection, side 2 | | | 4.2 | 4.45 | V |
| UV _{VCC2} | Falling under voltage detection, side 2 | | 3.8 | 4.0 | 4.25 | V |
| V _{HYS(UVCC2)} | Hysteresis voltage on V _{CC2} undervoltage lock-out | | | 200 | | mV |
| TXD TERMINAL | | | | | | |
| V _{IH} | High level input voltage | | 0.7×V _{CC1} | | | V |
| V _{IL} | Low level input voltage | | | | 0.3×V _{CC1} | V |
| I _{IH} | High level input leakage current | TXD = V _{CC1} | | | 1 | μA |
| I _{IL} | Low level input leakage current | TXD = 0V | -20 | | | μA |
| C _I | Input capacitance | V _{IN} = 0.4 x sin(2 x π x 1E+6 x t) + 2.5 V, V _{CC1} = 5 V | | | 3 | pF |
| RXD TERMINAL | | | | | | |
| V _{OH} - V _{CC1} | High level output voltage | See Figure 7-4 , I _O = -4 mA for 4.5 V ≤ V _{CC1} ≤ 5.5 V | -0.4 | -0.2 | | V |
| | | See Figure 7-4 , I _O = -2 mA for 3.0 V ≤ V _{CC1} ≤ 3.6 V | -0.2 | -0.07 | | V |
| | | See Figure 7-4 , I _O = -1 mA for 2.25 V ≤ V _{CC1} ≤ 2.75 V | -0.1 | -0.04 | | V |
| | | See Figure 7-4 , I _O = -1 mA for 1.71 V ≤ V _{CC1} ≤ 1.89 V | -0.1 | -0.045 | | V |
| V _{OL} | Low level output voltage | See Figure 7-4 , I _O = 4 mA for 4.5 V ≤ V _{CC1} ≤ 5.5 V | | 0.2 | 0.4 | V |
| | | See Figure 7-4 , I _O = 2 mA for 3.0 V ≤ V _{CC1} ≤ 3.6 V | | 0.07 | 0.2 | V |
| | | See Figure 7-4 , I _O = 1 mA for 2.25 V ≤ V _{CC1} ≤ 2.75 V | | 0.035 | 0.1 | V |
| | | See Figure 7-4 , I _O = 1 mA for 1.71 V ≤ V _{CC1} ≤ 1.89 V | | 0.04 | 0.1 | V |
| DRIVER ELECTRICAL CHARACTERISTICS | | | | | | |
| V _{O(DOM)} | Bus output voltage(Dominant), CANH | See Figure 7-1 and Figure 7-2 , TXD = 0 V, 50 Ω ≤ R _L ≤ 65 Ω, C _L = open | 2.75 | | 4.5 | V |
| | Bus output voltage(Dominant), CANL | See Figure 7-1 and Figure 7-2 , TXD = 0 V, 50 Ω ≤ R _L ≤ 65 Ω, C _L = open | 0.5 | | 2.25 | V |

Over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--|---|--------|------------------------|-------|------|
| $V_{O(REC)}$ | Bus output voltage(recessive), CANH and CANL | See Figure 7-1 and Figure 7-2 , TXD = V _{CC1} , R _L = open | 2.0 | 0.5 x V _{CC2} | 3.0 | V |
| $V_{OD(DOM)}$ | Differential output voltage, CANH-CANL (dominant) | See Figure 7-1 and Figure 7-2 , TXD = 0 V, 45 Ω ≤ R _L ≤ 50 Ω, C _L = open | 1.4 | | 3.0 | V |
| | Differential output voltage, CANH-CANL (dominant) | See Figure 7-1 and Figure 7-2 , TXD = 0 V, 50 Ω ≤ R _L ≤ 65 Ω, C _L = open | 1.5 | | 3.0 | V |
| | Differential output voltage, CANH-CANL (dominant) | See Figure 7-1 and Figure 7-2 , TXD = 0 V, R _L = 2240 Ω, C _L = open | 1.5 | | 5.0 | V |
| $V_{OD(REC)}$ | Differential output voltage, CANH-CANL (recessive) | See Figure 7-1 and Figure 7-2 , TXD = V _{CC1} , R _L = 60 Ω, C _L = open | -120.0 | | 12.0 | mV |
| | Differential output voltage, CANH-CANL (recessive) | See Figure 7-1 and Figure 7-2 , TXD = V _{CC1} , R _L = open, C _L = open | -50.0 | | 50.0 | mV |
| V_{SYM_DC} | DC Output symmetry (V _{CC2} - V _{O(CANH)} - V _{O(CANL)}) | See Figure 7-1 and Figure 7-2 , R _L = 60 Ω, C _L = open, TXD = V _{CC1} or 0 V | -400.0 | | 400.0 | mV |
| $I_{SO(SS_DOM)}$ | Short circuit current steady state output current, dominant | See Figure 7-9 , V _{CANH} = -5 V to 40 V, CANL = open, TXD = 0 V | -100.0 | | | mA |
| | | See Figure 7-9 , V _{CANL} = -5 V to 40 V, CANH = open, TXD = 0 V | | | 100.0 | mA |
| $I_{SO(SS_REC)}$ | Short circuit current steady state output current, recessive | See Figure 7-9 , -27 V ≤ V _{BUS} ≤ 32 V, V _{BUS} = CANH = CANL, TXD = V _{CC1} | -5.0 | | 5.0 | mA |

RECEIVER ELECTRICAL CHARACTERISTICS

| | | | | | | |
|----------------|---|---|-------|------|--------|----|
| V_{IT} | Differential input threshold voltage | See Figure 7-4 and Table 7-1 , V _{CM} ≤ 20 V | 500.0 | | 900.0 | mV |
| | Differential input threshold voltage | See Figure 7-4 and Table 7-1 , 20 V ≤ V _{CM} ≤ 30 V | 400.0 | | 1000.0 | |
| V_{HYS} | Hysteresis voltage for differential input threshold | See Figure 7-4 and Table 7-1 | | 120 | | |
| V_{CM} | Input common mode range | See Figure 7-4 and Table 7-1 | -30.0 | | 30.0 | V |
| $I_{OFF(LKG)}$ | Power-off bus input leakage current | CANH = CANL = 5 V, V _{CC2} to GND via 0 Ω and 47 kΩ resistor | | | 4.8 | μA |
| C_I | Input capacitance to ground (CANH or CANL) | TXD = V _{CC1} | | 24.0 | 30 | pF |
| C_{ID} | Differential input capacitance (CANH-CANL) | TXD = V _{CC1} | | 12.0 | 15 | pF |
| R_{ID} | Differential input resistance | TXD = V _{CC1} ; -30 V ≤ V _{CM} ≤ +30 V | 30.0 | | 80.0 | kΩ |
| R_{IN} | Input resistance (CANH or CANL) | TXD = V _{CC1} ; -30 V ≤ V _{CM} ≤ +30 V | 15.0 | | 40.0 | kΩ |
| $R_{IN(M)}$ | Input resistance matching: (1 - R _{IN(CANH)} /R _{IN(CANL)}) x 100% | V _{CANH} = V _{CANL} = 5 V | -2.0 | | 2.0 | % |

THERMAL SHUTDOWN

| | | | | | | |
|-----------------|------------------------------|--|--|-----|--|----|
| T_{TSD} | Thermal shutdown temperature | | | 170 | | °C |
| T_{TSD_HYST} | Thermal shutdown hysteresis | | | 5 | | °C |

6.11 Switching Characteristics

Over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|-------|-----|-------|-------|
| DEVICE SWITCHING CHARACTERISTICS | | | | | | |
| t _{PROP(LOOP1)} | Total loop delay, driver input TXD to receiver RXD, recessive to dominant | See Figure 7-6 , R _L = 60 Ω, C _L = 100 pF, C _{L(RXD)} = 15 pF; input rise/fall time (10% to 90%) on TXD = 1 ns; 1.71 V ≤ V _{CC1} ≤ 1.89 V | 70 | 125 | 198.0 | ns |
| | | See Figure 7-6 , R _L = 60 Ω, C _L = 100 pF, C _{L(RXD)} = 15 pF; input rise/fall time (10% to 90%) on TXD = 1 ns; 2.25 V ≤ V _{CC1} ≤ 5.5 V | 70 | 122 | 192.0 | ns |
| t _{PROP(LOOP2)} | Total loop delay, driver input TXD to receiver RXD, dominant to recessive | See Figure 7-6 , R _L = 60 Ω, C _L = 100 pF, C _{L(RXD)} = 15 pF; input rise/fall time (10% to 90%) on TXD = 1 ns; 1.71 V ≤ V _{CC1} ≤ 1.89 V | 70 | 155 | 215.0 | ns |
| | | See Figure 7-6 , R _L = 60 Ω, C _L = 100 pF, C _{L(RXD)} = 15 pF; input rise/fall time (10% to 90%) on TXD = 1 ns; 2.25 V ≤ V _{CC1} ≤ 5.5 V | 70 | 152 | 215.0 | ns |
| t _{UV_RE_ENABLE} | Re-enable time after Undervoltage event | Time for device to return to normal operation from V _{CC1} or V _{CC2} under voltage event | | | 300.0 | μs |
| CMTI | Common mode transient immunity | V _{CM} = 1200 V _{PK} , See Figure 7-10 | 85 | 100 | | kV/μs |
| DRIVER SWITCHING CHARACTERISTICS | | | | | | |
| t _{pHR} | Propagation delay time, HIGH TXD to driver recessive | See Figure 7-3 , R _L = 60 Ω and C _L = 100 pF; input rise/fall time (10% to 90%) on TXD = 1 ns | | 76 | 120 | ns |
| t _{pLD} | Propagation delay time, LOW TXD to driver dominant | | | 61 | 120 | |
| t _{sk(p)} | Pulse skew (t _{pHR} - t _{pLD}) | | | 14 | | |
| t _R | Differential output signal rise time | | | 45 | | |
| t _F | Differential output signal fall time | | | 45 | | |
| V _{SYM} | Output symmetry (dominant or recessive) (V _{O(CANH)} + V _{O(CANL)}) / V _{CC2} | See Figure 7-3 and Figure 9-4 , R _{TERM} = 60 Ω, C _{SPLIT} = 4.7 nF, C _L = open, R _L = open, TXD = 250 kHz, 1 MHz | 0.9 | | 1.1 | V/V |
| t _{TXD_DTO} | Dominant time out | See Figure 7-8 , R _L = 60 Ω and C _L = open | 1.2 | | 3.8 | ms |
| RECEIVER SWITCHING CHARACTERISTICS | | | | | | |
| t _{pRH} | Propagation delay time, bus recessive input to RXD high output | See Figure 7-5 , C _{L(RXD)} = 15 pF | | 75 | 130 | ns |
| t _{pDL} | Propagation delay time, bus dominant input to RXD low output | | | 63 | 130 | ns |
| t _R | Output signal rise time(RXD) | | | 1.4 | | ns |
| t _F | Output signal fall time(RXD) | | | 1.8 | | ns |
| FD TIMING PARAMETERS | | | | | | |
| t _{BIT(BUS)} | Bit time on CAN bus output pins with t _{BIT(TXD)} = 500 ns | See Figure 7-7 , R _L = 60 Ω, C _L = 100 pF, C _{L(RXD)} = 15 pF; input rise/fall time (10% to 90%) on TXD = 1 ns | 435.0 | | 530.0 | ns |
| | Bit time on CAN bus output pins with t _{BIT(TXD)} = 200 ns | See Figure 7-7 , R _L = 60 Ω, C _L = 100 pF, C _{L(RXD)} = 15 pF; input rise/fall time (10% to 90%) on TXD = 1 ns | 155.0 | | 210.0 | ns |

Over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|---|---|-------|-----|-------|------|
| $t_{\text{BIT(RXD)}}$ | Bit time on RXD output pins with $t_{\text{BIT(TXD)}} = 500 \text{ ns}$ | See Figure 7-7, $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{L(\text{RXD})} = 15 \text{ pF}$; input rise/fall time (10% to 90%) on TXD = 1 ns | 400 | | 550.0 | ns |
| | Bit time on RXD output pins with $t_{\text{BIT(TXD)}} = 200 \text{ ns}$ | See Figure 7-7, $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{L(\text{RXD})} = 15 \text{ pF}$; input rise/fall time (10% to 90%) on TXD = 1 ns | 120.0 | | 220.0 | ns |
| Δt_{REC} | Receiver timing symmetry with $t_{\text{BIT(TXD)}} = 500 \text{ ns}$ | See Figure 7-7, $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{L(\text{RXD})} = 15 \text{ pF}$; input rise/fall time (10% to 90%) on TXD = 1 ns; $\Delta t_{\text{REC}} = t_{\text{BIT(RXD)}} - t_{\text{BIT(BUS)}}$ | -65.0 | | 40.0 | ns |
| | Receiver timing symmetry with $t_{\text{BIT(TXD)}} = 200 \text{ ns}$ | See Figure 7-7, $R_L = 60 \Omega$, $C_L = 100 \text{ pF}$, $C_{L(\text{RXD})} = 15 \text{ pF}$; input rise/fall time (10% to 90%) on TXD = 1 ns; $\Delta t_{\text{REC}} = t_{\text{BIT(RXD)}} - t_{\text{BIT(BUS)}}$ | -45.0 | | 15.0 | ns |

6.12 Insulation Characteristics Curves

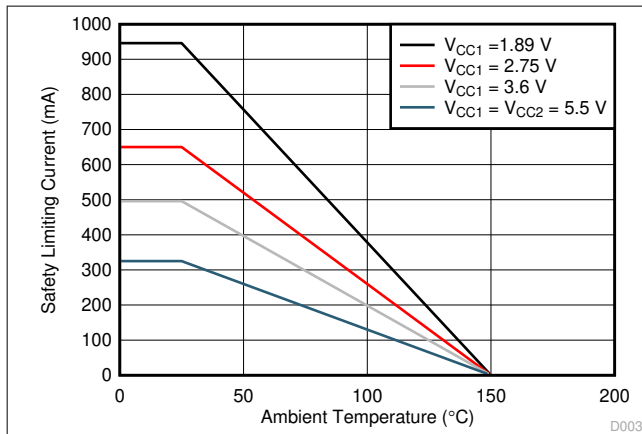


Figure 6-1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

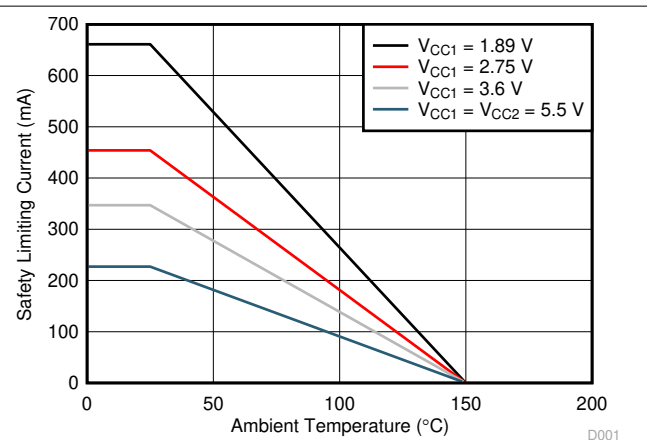


Figure 6-2. Thermal Derating Curve for Limiting Current per VDE for DWV-8 Package

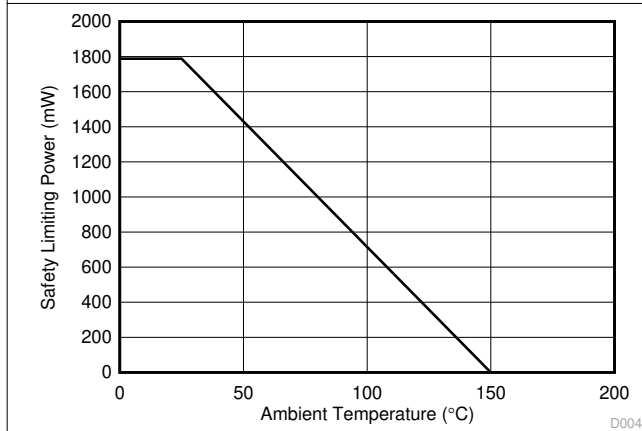


Figure 6-3. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

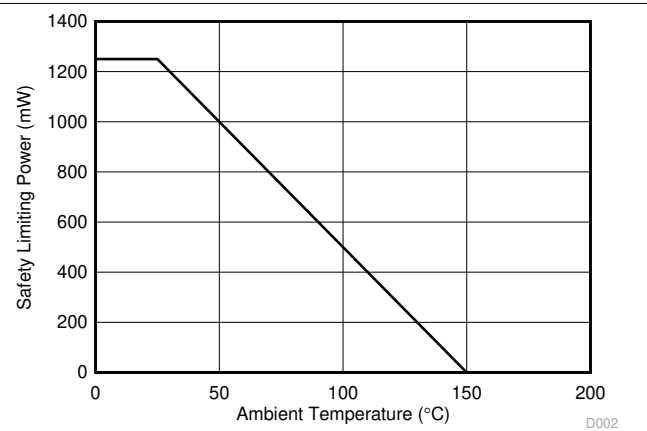


Figure 6-4. Thermal Derating Curve for Limiting Power per VDE for DWV-8 Package

6.13 Typical Characteristics

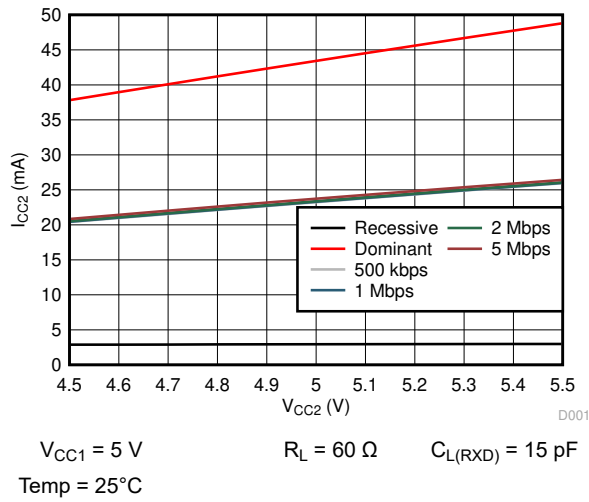


Figure 6-5. I_{CC2} vs V_{CC2} for Recessive, Dominant and Different CAN Datarates

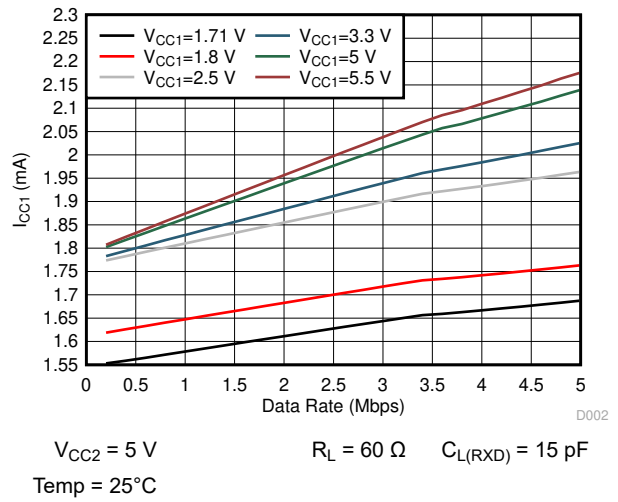


Figure 6-6. I_{CC1} vs Datarate

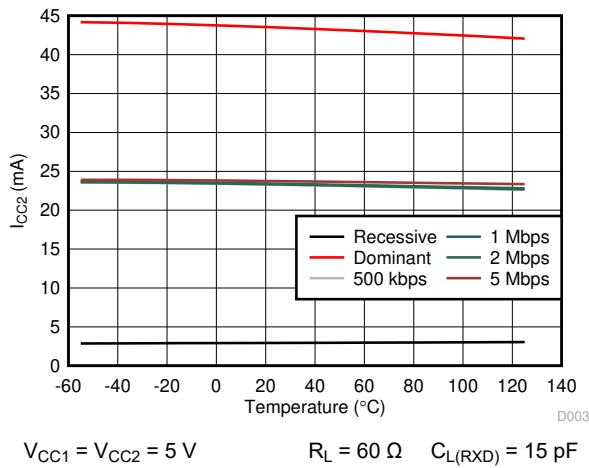


Figure 6-7. I_{CC2} vs Ambient Temperature for Recessive, Dominant and Different CAN Datarates

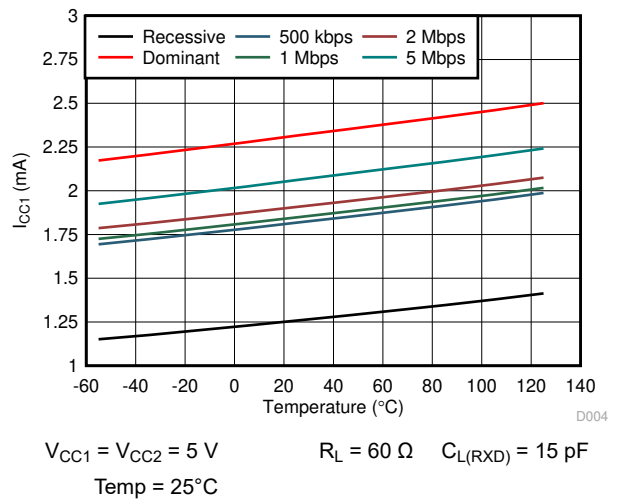
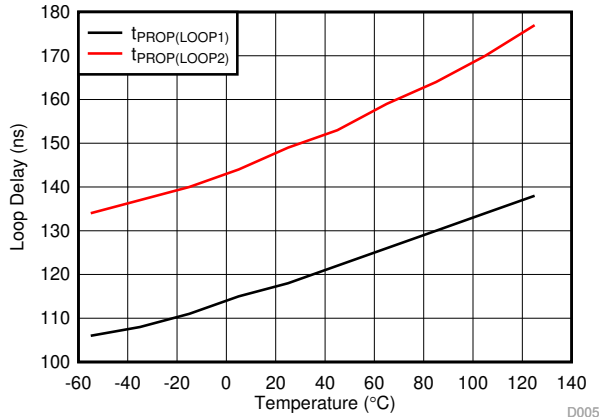
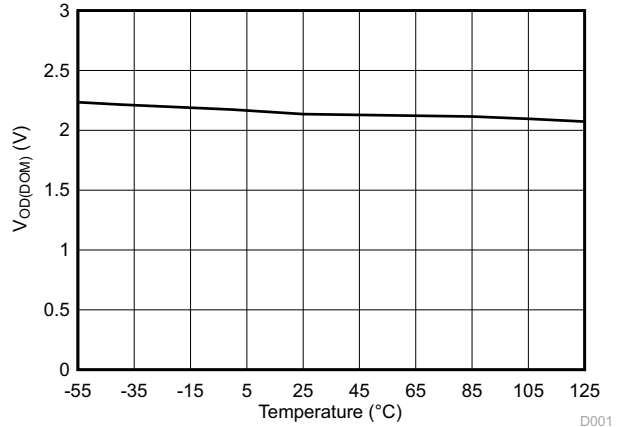


Figure 6-8. : I_{CC1} vs Ambient Temperature for Recessive, Dominant and Different CAN Datarates.



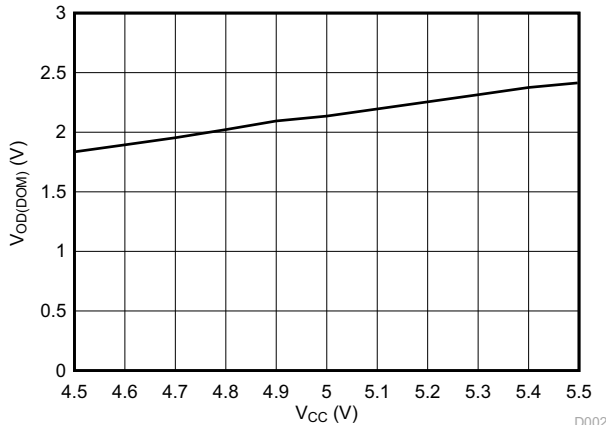
$V_{CC1} = V_{CC2} = 5\text{ V}$ $R_L = 60\ \Omega$ $C_{L(RXD)} = 15\text{ pF}$

Figure 6-9. Loop Delay vs Ambient Temperature



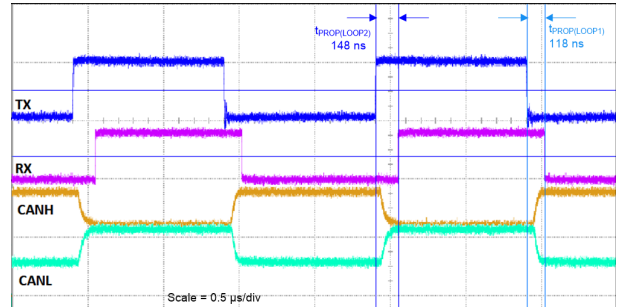
$V_{CC} = 5\text{ V}$ $V_{CC1} = 5\text{ V}$ $R_L = 60\ \Omega$
 $C_L = \text{Open}$

Figure 6-10. $V_{OD(DOM)}$ Over Temperature



$V_{CC1} = 5\text{ V}$ $R_L = 60\ \Omega$
 $C_L = \text{Open}$ Temp = 25°C

Figure 6-11. $V_{OD(DOM)}$ Over V_{CC}



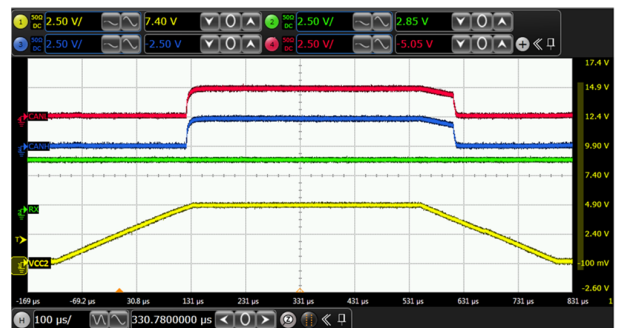
$V_{CC1} = V_{CC2} = 5\text{ V}$ $R_L = 60\ \Omega$ $C_L = 100\text{ pF}$
 $C_{L(RXD)} = 15\text{ pF}$

Figure 6-12. Typical TXD, RXD, CANH and CANL Waveforms at 1 Mbps



TXD = V_{CC1} $R_L = 60\ \Omega$ $V_{CC1} = V_{CC2} = 5\text{ V}$

Figure 6-13. Glitch Free Power Up on V_{CC1} – CAN Bus Remains Recessive



TXD = V_{CC1} $R_L = 60\ \Omega$ $V_{CC1} = V_{CC2} = 5\text{ V}$

Figure 6-14. Glitch Free Power Up on V_{CC2} – CAN Bus Remains Recessive

7 Parameter Measurement Information

7.1 Test Circuits

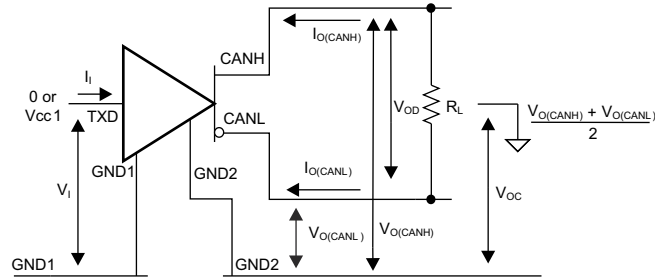


Figure 7-1. Driver Voltage, Current and Test Definitions

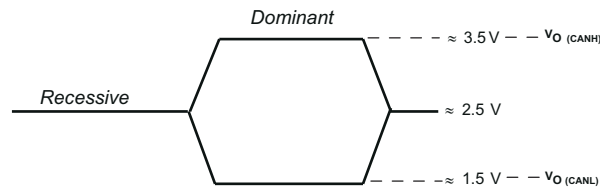
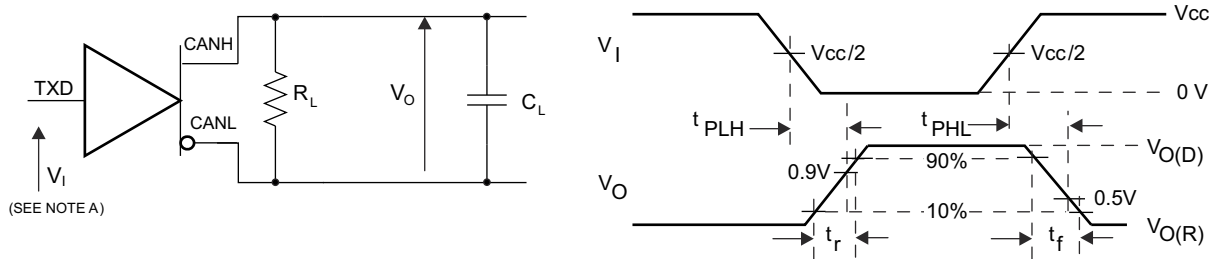


Figure 7-2. Bus Logic State Voltage Definitions



- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 125 kHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, $Z_O = 50 \Omega$.

Figure 7-3. Driver Test Circuit and Voltage Waveforms

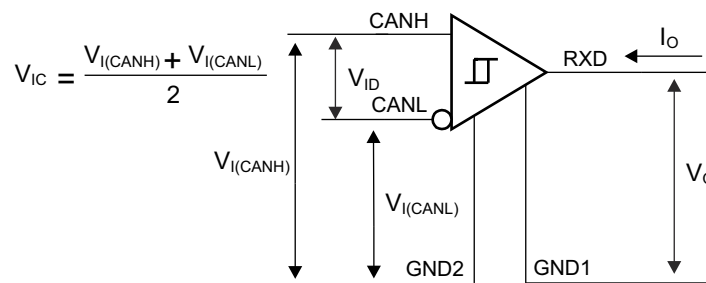
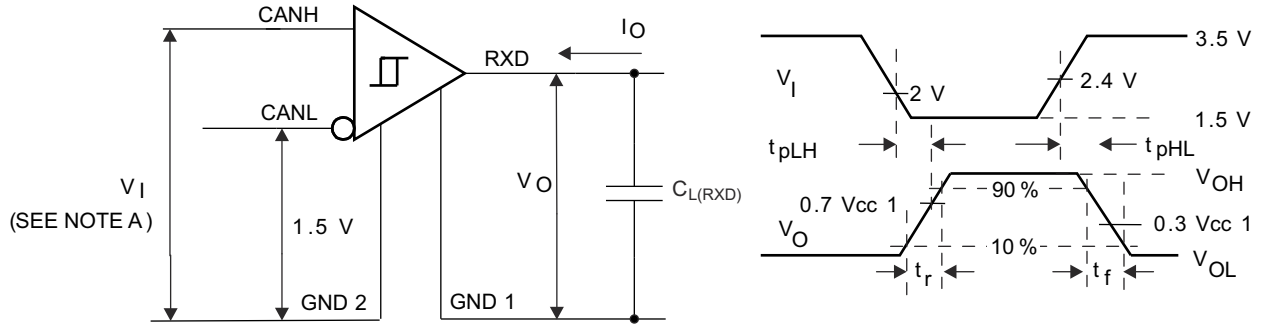


Figure 7-4. Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 125 kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 7-5. Receiver Test Circuit and Voltage Waveforms

Table 7-1. Receiver Differential Input Voltage Threshold Test

| INPUT | | | OUTPUT | |
|------------|------------|------------|--------|----------|
| V_{CANH} | V_{CANL} | $ V_{ID} $ | RXD | |
| -29.5 V | -30.5 V | 1000 mV | L | V_{OL} |
| 30.5 V | 29.5 V | 1000 mV | L | |
| -19.55 V | -20.45 V | 900 mV | L | |
| 20.45 V | 19.55 V | 900 mV | L | |
| -19.75 V | -20.25 V | 500 mV | H | V_{OH} |
| 20.25 V | 19.75 V | 500 mV | H | |
| -29.8 V | -30.2 V | 400 mV | H | |
| 30.2 V | 29.8 V | 400 mV | H | |
| Open | Open | X | H | |

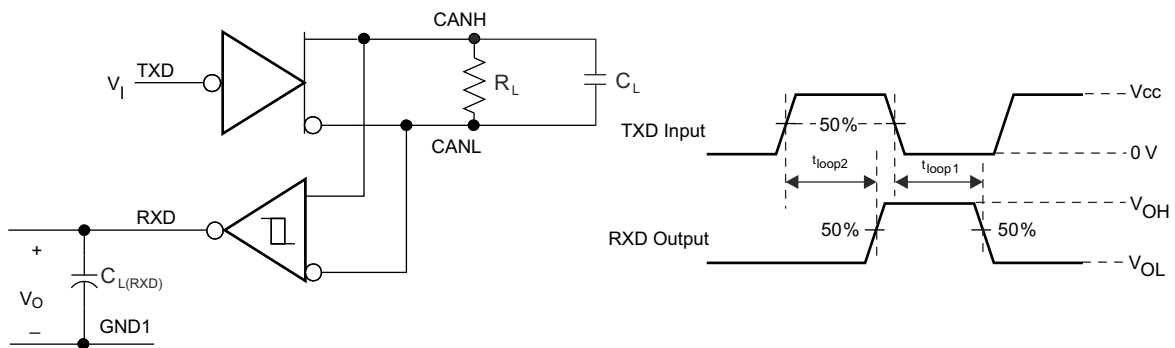


Figure 7-6. t_{LOOP} Test Circuit and Voltage Waveforms

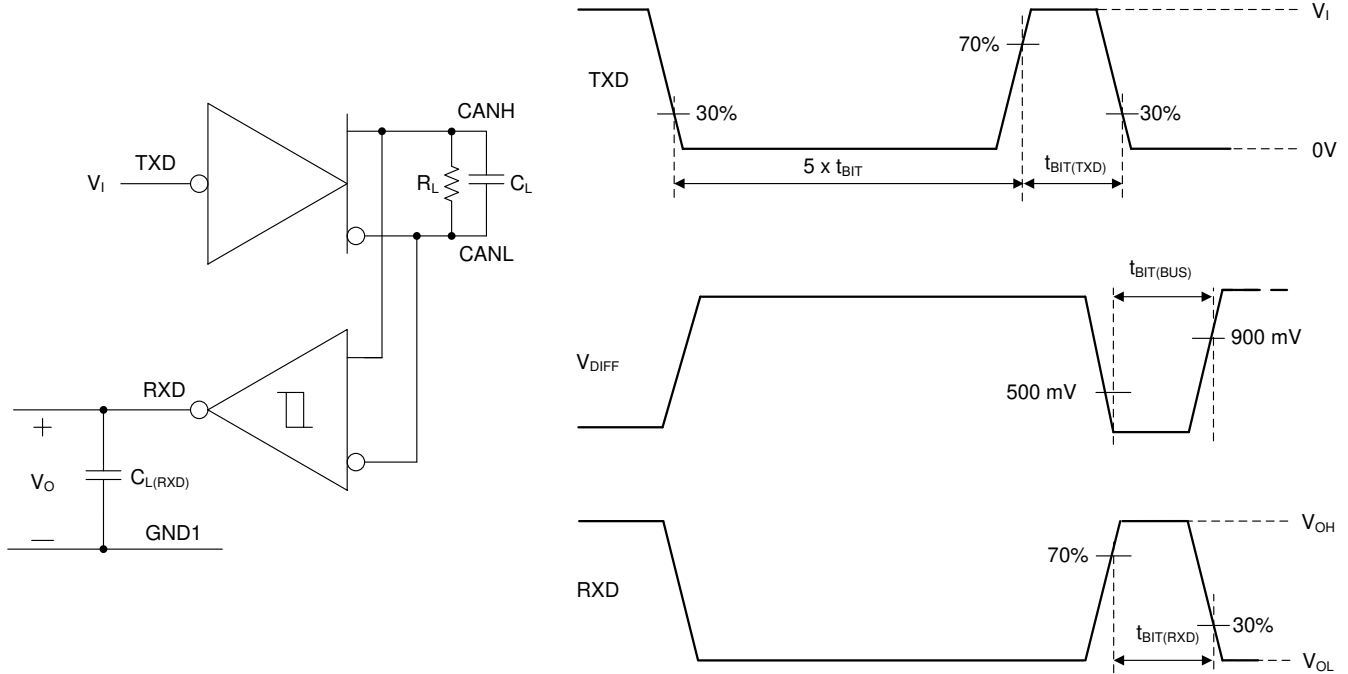
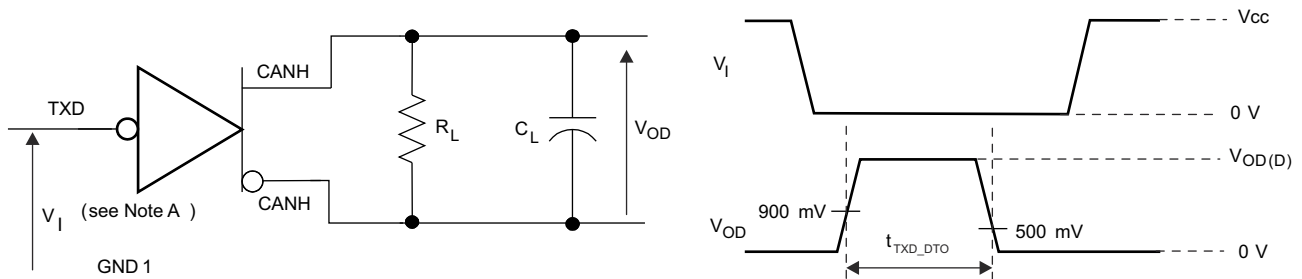


Figure 7-7. CAN FD Timing Parameter Measurement



A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.

Figure 7-8. Dominant Time-out Test Circuit and Voltage Waveforms

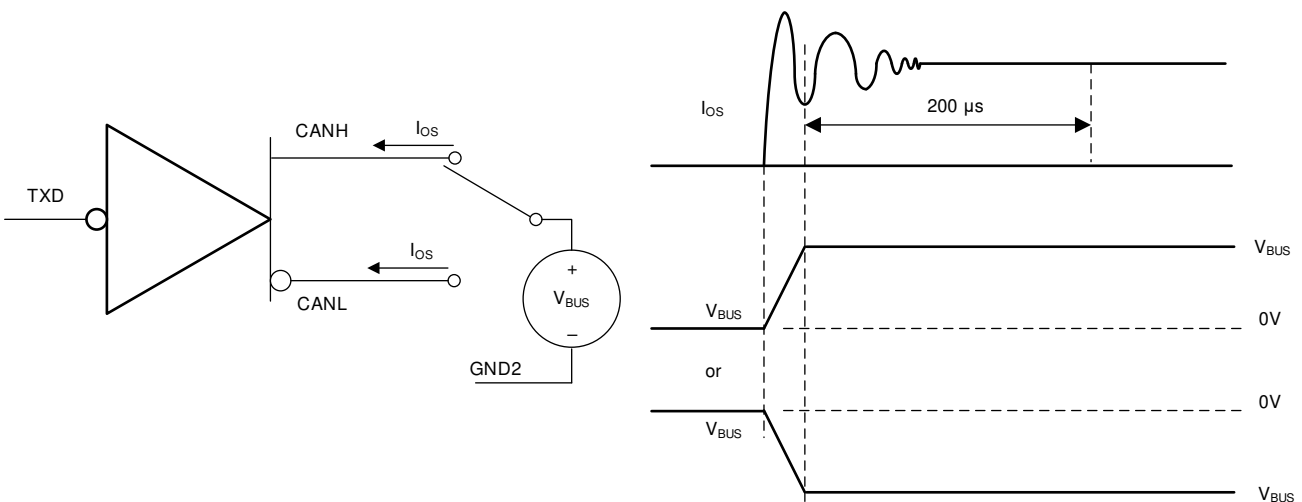


Figure 7-9. Driver Short-Circuit Current Test Circuit and Waveforms

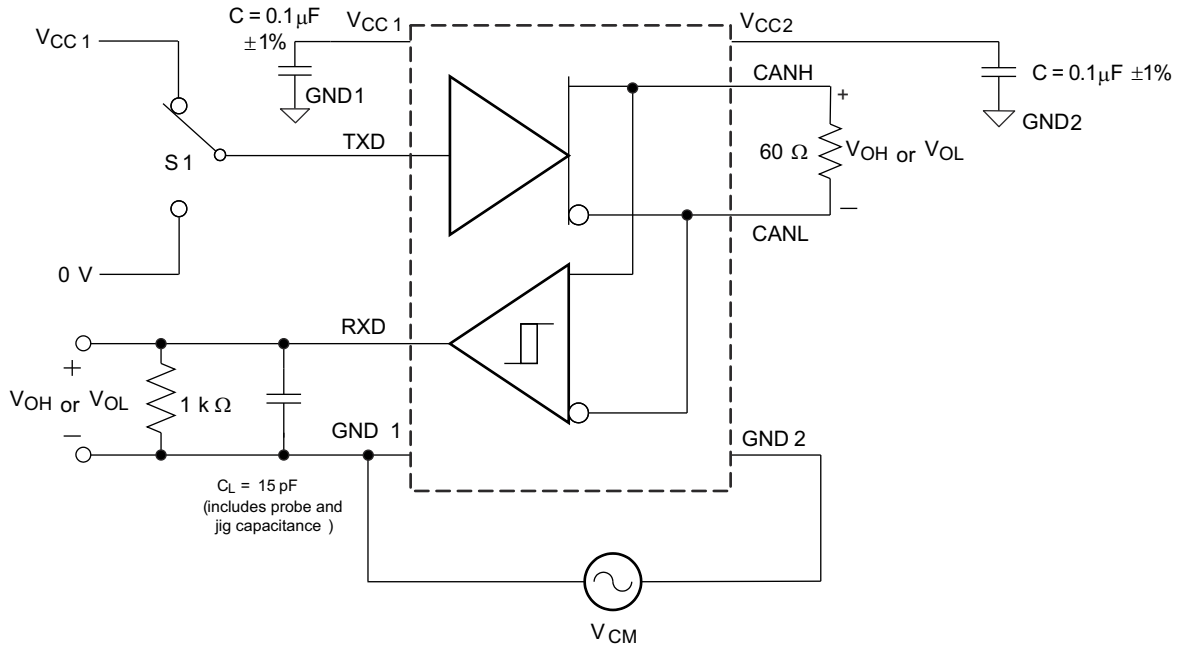


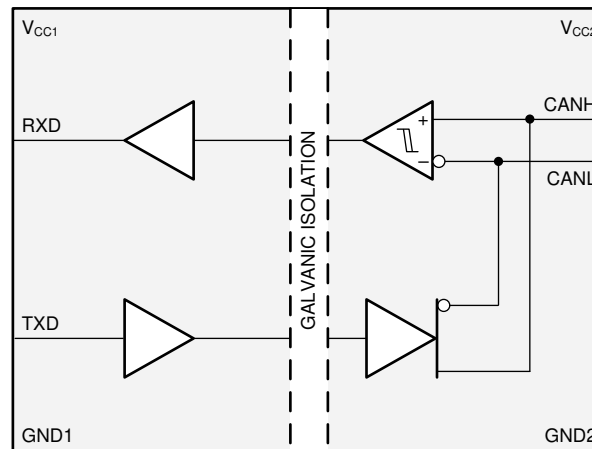
Figure 7-10. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO1042-Q1 device is a digitally isolated CAN transceiver that offers ± 70 -V DC bus fault protection and ± 30 -V common-mode voltage range. The device supports up to 5-Mbps data rate in CAN FD mode allowing much faster transfer of payload compared to classic CAN. The ISO1042-Q1 device has an isolation withstand voltage of 5000 V_{RMS} and is available in basic and reinforced isolation with a surge test voltage of 6 kV_{PK} and 10 kV_{PK} respectively. The device can operate from 1.8-V, 2.5-V, 3.3-V, and 5-V supplies on side 1 and a 5-V supply on side 2. This supply range is of particular advantage for applications operating in harsh industrial environments because the low voltage on side 1 enables the connection to low-voltage microcontrollers for power conservation, whereas the 5 V on side 2 maintains a high signal-to-noise ratio of the bus signals.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 CAN Bus States

The CAN bus has two states during operation: *dominant* and *recessive*. A dominant bus state, equivalent to logic low, is when the bus is driven differentially by a driver. A recessive bus state is when the bus is biased to a common mode of $V_{CC} / 2$ through the high-resistance internal input resistors of the receiver, equivalent to a logic high. The host microprocessor of the CAN node uses the TXD pin to drive the bus and receives data from the bus on the RXD pin. See [Figure 8-1](#) and [Figure 8-2](#).

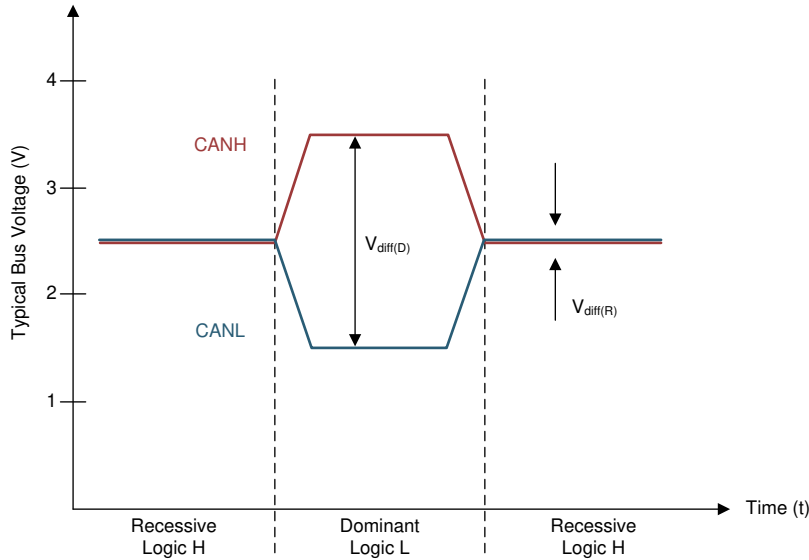


Figure 8-1. Bus States (Physical Bit Representation)

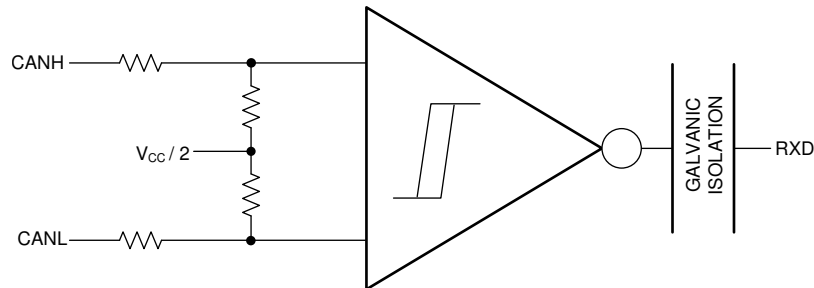


Figure 8-2. Simplified Recessive Common Mode Bias and Receiver

8.3.2 Digital Inputs and Outputs: TXD (Input) and RXD (Output)

The V_{CC1} supply for the isolated digital input and output side of the device can be supplied by 1.8-V, 2.5-V, 3.3-V, and 5-V supplies and therefore the digital inputs and outputs are 1.8-V, 2.5-V, 3.3-V, and 5-V compatible.

Note

The TXD pin is very weakly internally pulled up to V_{CC1} . An external pullup resistor should be used to make sure that the TXD pin is biased to recessive (high) level to avoid issues on the bus if the microprocessor does not control the pin and the TXD pin floats. The TXD pullup strength and CAN bit timing require special consideration when the device is used with an open-drain TXD output on the CAN controller of the microprocessor. An adequate external pullup resistor must be used to make sure that the TXD output of the microprocessor maintains adequate bit timing input to the input on the transceiver.

8.3.3 Protection Features

8.3.3.1 TXD Dominant Timeout (DTO)

The TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where the TXD pin is held dominant longer than the timeout period, t_{TXD_DTO} . The DTO circuit timer starts on a falling edge on the TXD pin. The DTO circuit disables the CAN bus driver if no rising edge occurs before the timeout period expires, which frees the bus for communication between other nodes on the network. The CAN driver is activated again when a recessive signal occurs on the TXD pin, clearing the TXD DTO condition. The receiver and RXD pin still reflect activity on the CAN bus, and the bus terminals are biased to the recessive level during a TXD dominant timeout.

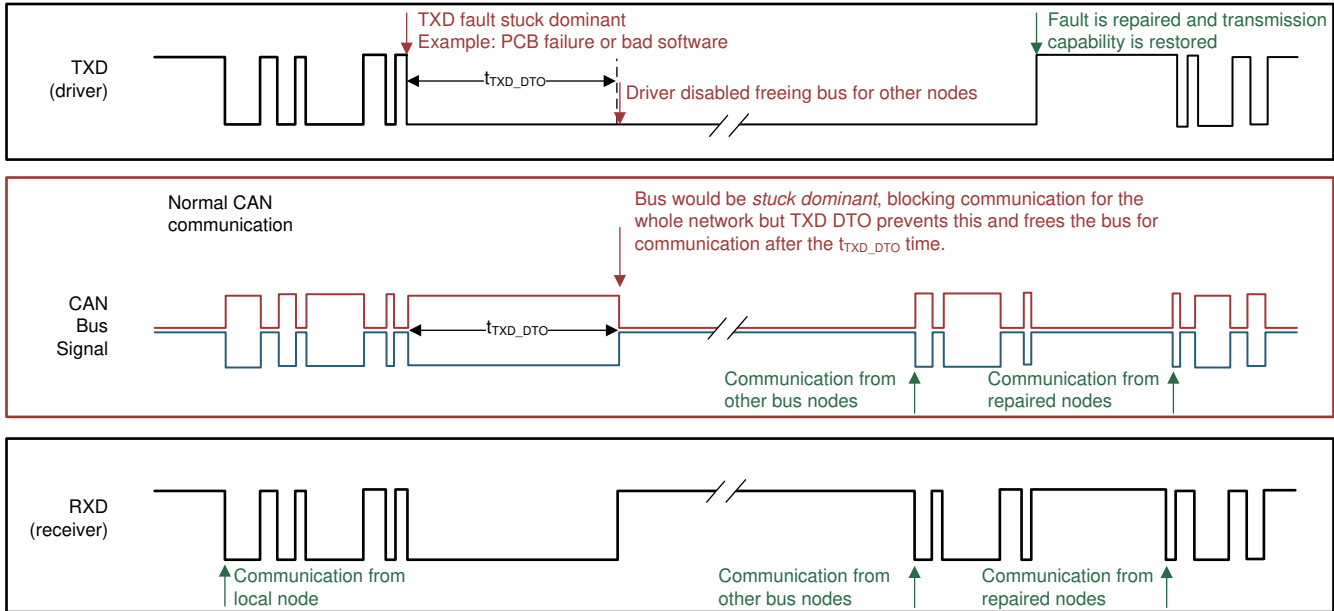


Figure 8-3. Example Timing Diagram for TXD DTO

Note

The minimum dominant TXD time (t_{TXD_DTO}) allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate with [Equation 1](#).

$$\text{Minimum Data Rate} = 11 / t_{TXD_DTO} \tag{1}$$

8.3.3.2 Thermal Shutdown (TSD)

If the junction temperature of the device exceeds the thermal shutdown threshold (T_{TSD}), the device turns off the CAN driver circuits, blocking the TXD-to-bus transmission path. The CAN bus terminals are biased to the recessive level during a thermal shutdown, and the receiver-to-RXD path remains operational. The shutdown condition is cleared when the junction temperature drops at least the thermal shutdown hysteresis temperature (T_{TSD_HYST}) below the thermal shutdown temperature (T_{TSD}) of the device.

8.3.3.3 Undervoltage Lockout and Default State

The supply pins have undervoltage detection that places the device in protected or default mode which protects the bus during an undervoltage event on the V_{CC1} or V_{CC2} supply pins. If the bus-side power supply, V_{CC2} , is less than about 4 V, the power shutdown circuits in the ISO1042-Q1 device disable the transceiver to prevent false transmissions because of an unstable supply. If the V_{CC1} supply is still active when this occurs, the receiver output (RXD) goes to a default HIGH (recessive) value. [Table 8-1](#) summarizes the undervoltage lockout and fail-safe behavior.

Table 8-1. Undervoltage Lockout and Default State

| V_{CC1} | V_{CC2} | DEVICE STATE | BUS OUTPUT | RXD |
|---------------|---------------|--------------|--------------------------|--------------------------|
| $> UV_{VCC1}$ | $> UV_{VCC2}$ | Functional | Per Device State and TXD | Mirrors Bus |
| $< UV_{VCC1}$ | $> UV_{VCC2}$ | Protected | Recessive | Undetermined |
| $> UV_{VCC1}$ | $< UV_{VCC2}$ | Protected | High Impedance | Recessive (Default High) |

Note

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation in 300 μ s.

8.3.3.4 Floating Pins

Pullup and pulldown resistors should be used on critical pins to place the device into known states if the pins float. The TXD pin should be pulled up through a resistor to the V_{CC1} pin to force a recessive input level if the microprocessor output to the pin floats.

8.3.3.5 Unpowered Device

The device is designed to be *ideal passive* or *no load* to the CAN bus if it is unpowered. The bus pins (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus which is critical if some nodes of the network are unpowered while the rest of the of network remains in operation.

8.3.3.6 CAN Bus Short Circuit Current Limiting

The device has two protection features that limit the short circuit current when a CAN bus line has a short-circuit fault condition. The first protection feature is driver current limiting (both dominant and recessive states) and the second feature is TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states, therefore the short circuit current may be viewed either as the instantaneous current during each bus state or as an average current of the two states. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit stuffing
- Interframe space
- TXD dominant time out (fault case limiting)

These factors ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits. The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. Use [Equation 2](#) to calculate the average short circuit current.

$$I_{OS(AVG)} = \%Transmit \times [(\%REC_Bits \times I_{OS(SS)_REC}) + (\%DOM_Bits \times I_{OS(SS)_DOM})] + [\%Receive \times I_{OS(SS)_REC}] \quad (2)$$

where

- I_{OS(AVG)} is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- I_{OS(SS)_REC} is the recessive steady state short circuit current
- I_{OS(SS)_DOM} is the dominant steady state short circuit current

Note

Consider the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

8.4 Device Functional Modes

[Table 8-2](#) and [Table 8-3](#) list the driver and receiver functions. [Table 8-4](#) lists the functional modes for the ISO1042-Q1 device.

Table 8-2. Driver Function Table

| INPUT | OUTPUTS | | DRIVEN BUS STATE |
|-------|--------------------|---------------------|------------------|
| | TXD ⁽¹⁾ | CANH ⁽¹⁾ | |
| L | H | L | Dominant |
| H | Z | Z | Recessive |

- (1) H = high level, L = low level, Z = common mode (recessive) bias to $V_{CC} / 2$. See [Figure 8-1](#) and [Figure 8-2](#) for bus state and common mode bias information.

Table 8-3. Receiver Function Table

| DEVICE MODE | CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$ ⁽³⁾ | BUS STATE | RXD PIN ⁽¹⁾ |
|-------------|--|-----------|------------------------|
| Normal | $V_{ID} \geq V_{IT(MAX)}$ | Dominant | L |
| | $V_{IT(MIN)} < V_{ID} < V_{IT(MAX)}$ | ? | ? |
| | $V_{ID} \leq V_{IT(MIN)}$ | Recessive | H |
| | Open ($V_{ID} \approx 0$ V) | Open | H |

- (1) H = high level, L = low level, ? = indeterminate.

Table 8-4. Function Table

| DRIVER | | | RECEIVER | | | |
|-----------------------|---------|------|-----------|---|------------|-----------|
| INPUTS ⁽¹⁾ | OUTPUTS | | BUS STATE | DIFFERENTIAL INPUTS $V_{ID} = CANH - CANL$ ⁽³⁾ | OUTPUT RXD | BUS STATE |
| | TXD | CANH | | | | |
| L ⁽²⁾ | H | L | DOMINANT | $V_{ID} \geq V_{IT(MAX)}$ | L | DOMINANT |
| H | Z | Z | RECESSIVE | $V_{IT(MIN)} < V_{ID} < V_{IT(MAX)}$ | ? | ? |
| Open | Z | Z | RECESSIVE | $V_{ID} \leq V_{IT(MIN)}$ | H | RECESSIVE |
| X | Z | Z | RECESSIVE | Open ($V_{ID} \approx 0$ V) | H | RECESSIVE |

- (1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance
 (2) Logic low pulses to prevent dominant time-out.
 (3) See Receiver Electrical Characteristics section for input thresholds.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO1042-Q1 device can be used with other components from Texas Instruments such as a microcontroller, a transformer driver, and a linear voltage regulator to form a fully isolated CAN interface.

9.2 Typical Application

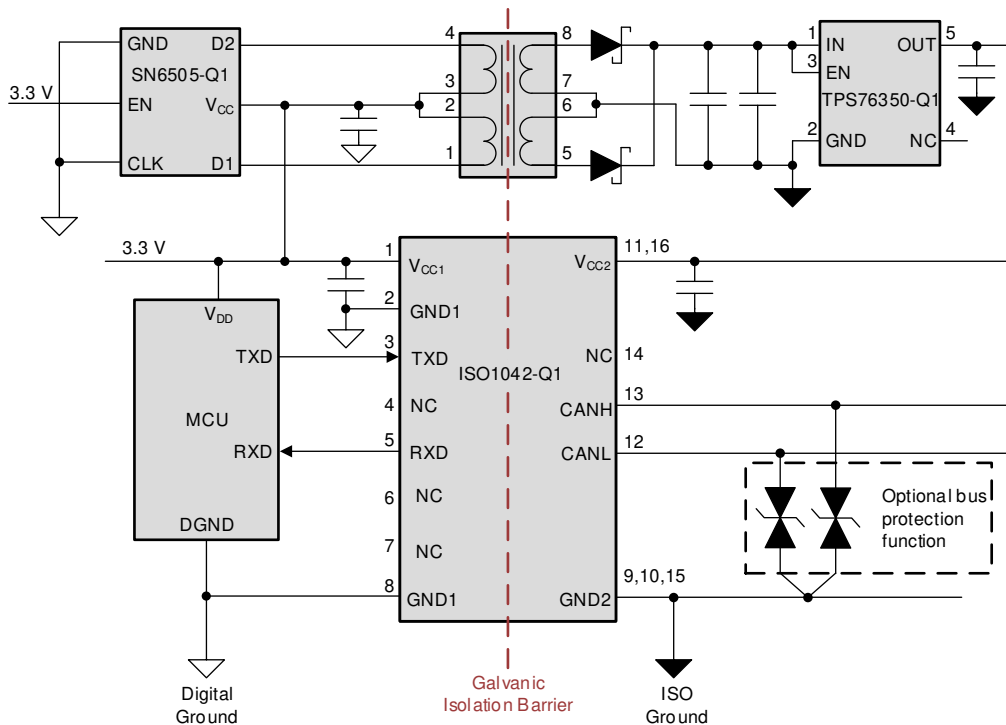


Figure 9-1. Application Circuit With ISO1042-Q1 in 16-SOIC Package

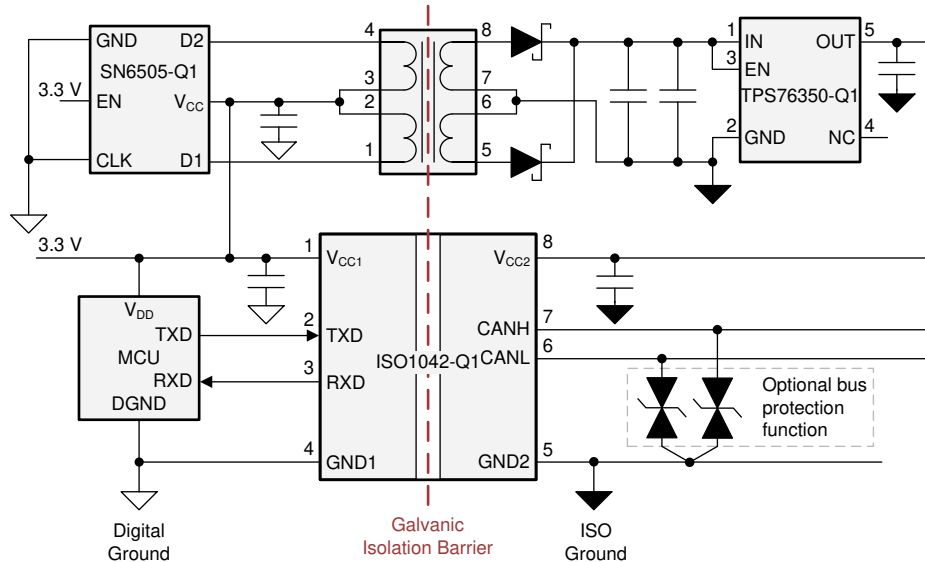


Figure 9-2. Application Circuit With ISO1042-Q1 in 8-SOIC Package

9.2.1 Design Requirements

Unlike an optocoupler-based solution, which requires several external components to improve performance, provide bias, or limit current, the ISO1042-Q1 device only requires external bypass capacitors to operate.

9.2.2 Detailed Design Procedure

9.2.2.1 Bus Loading, Length and Number of Nodes

The ISO 11898-2 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires transceivers with high input impedance such as the ISO1042-Q1 transceivers.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 Standard. These organizations and standards have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet, and NMEA2000.

The ISO1042-Q1 device is specified to meet the 1.5-V requirement with a 50- Ω load, incorporating the worst case including parallel transceivers. The differential input resistance of the ISO1042-Q1 device is a minimum of 30 k Ω . If 100 ISO1042-Q1 transceivers are in parallel on a bus, this requirement is equivalent to a 300- Ω differential load worst case. That transceiver load of 300 Ω in parallel with the 60 Ω gives an equivalent loading of 50 Ω . Therefore, the ISO1042-Q1 device theoretically supports up to 100 transceivers on a single bus segment. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity, therefore a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 m by careful system design and data-rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes, and a significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. Using this flexibility requires the responsibility of good network design and balancing these tradeoffs.

9.2.2.2 CAN Termination

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120- Ω characteristic impedance (Z_0). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting

nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node, but if nodes are removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

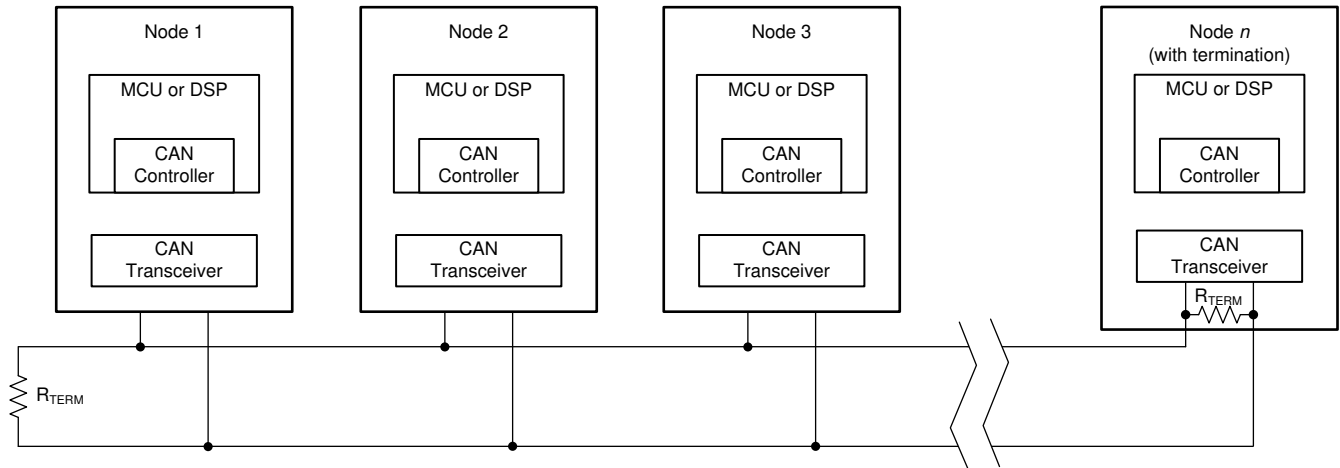


Figure 9-3. Typical CAN Bus

Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination can be used. (See Figure 9-4). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

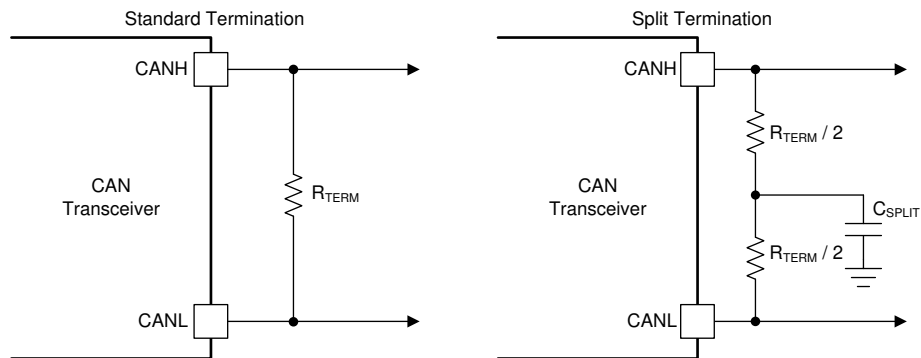


Figure 9-4. CAN Bus Termination Concepts

9.2.3 Application Curve

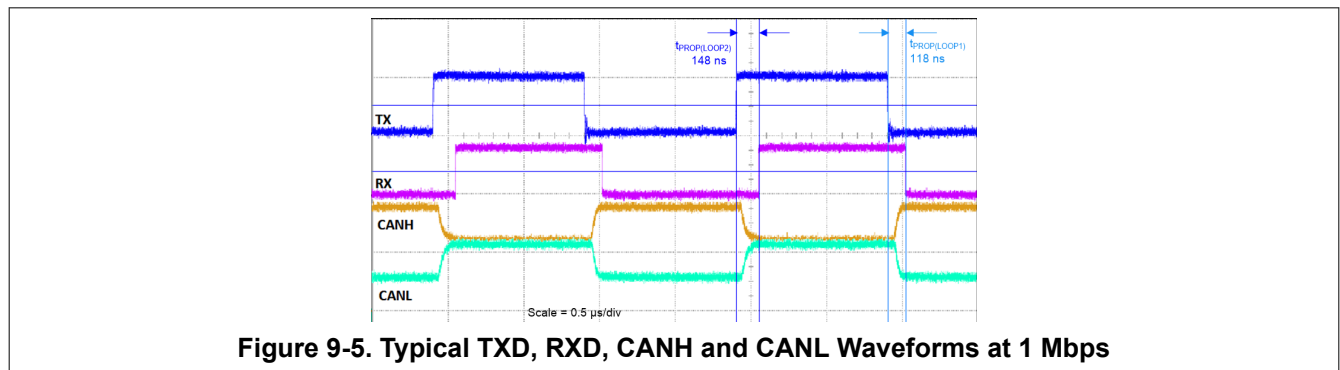


Figure 9-5. Typical TXD, RXD, CANH and CANL Waveforms at 1 Mbps

10 Power Supply Recommendations

To make sure operation is reliable at all data rates and supply voltages, a 0.1- μF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. In addition, a bulk capacitance, typically 4.7 μF , should be placed near the V_{CC2} supply pin. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's [SN6505B](#). For such applications, detailed power supply design, and transformer selection recommendations are available in the [SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Section 11.2](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

Suggested placement and routing of ISO1042-Q1 bypass capacitors and optional TVS diodes is shown in [Figure 11-2](#) and [Figure 11-3](#). In particular, place the V_{CC2} bypass capacitors on the top layer, as close to the device pins as possible, and complete the connection to the V_{CC2} and G_{ND2} pins without using vias. Note that the SOIC-16 variant needs two V_{CC2} bypass capacitor, one on each V_{CC2} pin.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over lower-cost alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

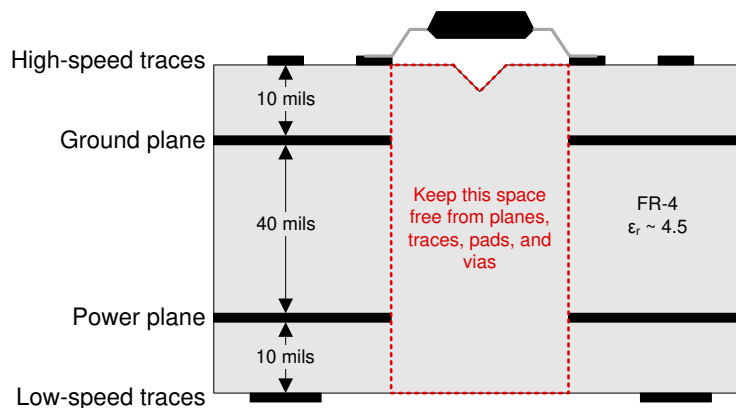


Figure 11-1. Recommended Layer Stack

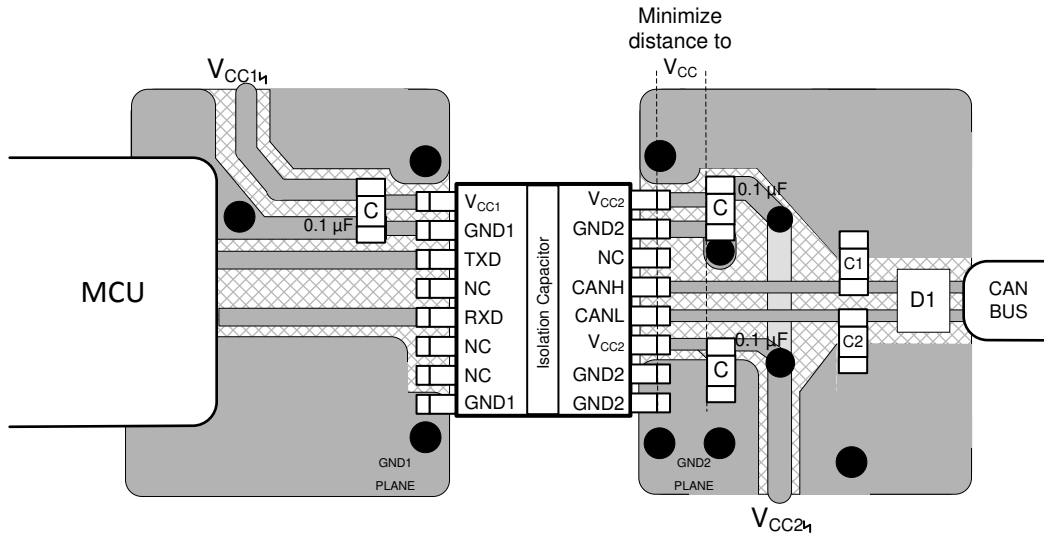


Figure 11-2. 16-DW Layout Example

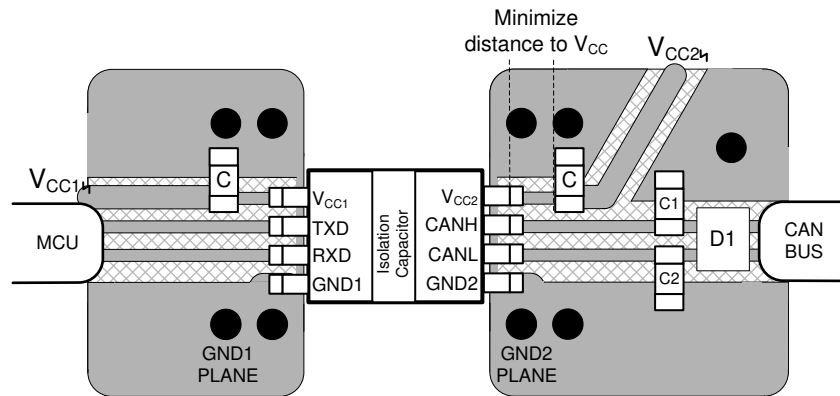


Figure 11-3. 8-DWV Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [ISO1042DW Isolated CAN Transceiver Evaluation Module User's Guide](#)
- Texas Instruments, [Isolate your CAN systems without compromising on performance or space TI TechNote](#)
- Texas Instruments, [Isolation Glossary](#)
- Texas Instruments, [High-voltage reinforced isolation: Definitions and test methodologies](#)
- Texas Instruments, [How to Isolate Signal and Power in Isolated CAN Systems TI TechNote](#)
- Texas Instruments, [How to Design Isolated CAN Systems With Correct Bus Protection Application Report](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| ISO1042BQDWQ1 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO1042BQ1 | Samples |
| ISO1042BQDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO1042BQ1 | Samples |
| ISO1042BQDWVQ1 | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO1042B Q1 | Samples |
| ISO1042BQDWVRQ1 | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO1042B Q1 | Samples |
| ISO1042QDWQ1 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO1042Q1 | Samples |
| ISO1042QDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO1042Q1 | Samples |
| ISO1042QDWVQ1 | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO1042 Q1 | Samples |
| ISO1042QDWVRQ1 | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | ISO1042 Q1 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO1042-Q1 :

- Catalog: [ISO1042](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISO1042BQDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO1042BQDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| ISO1042QDWRQ1 | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO1042QDWVRQ1 | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ISO1042BQDWRQ1 | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO1042BQDWVRQ1 | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| ISO1042QDWRQ1 | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO1042QDWVRQ1 | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |

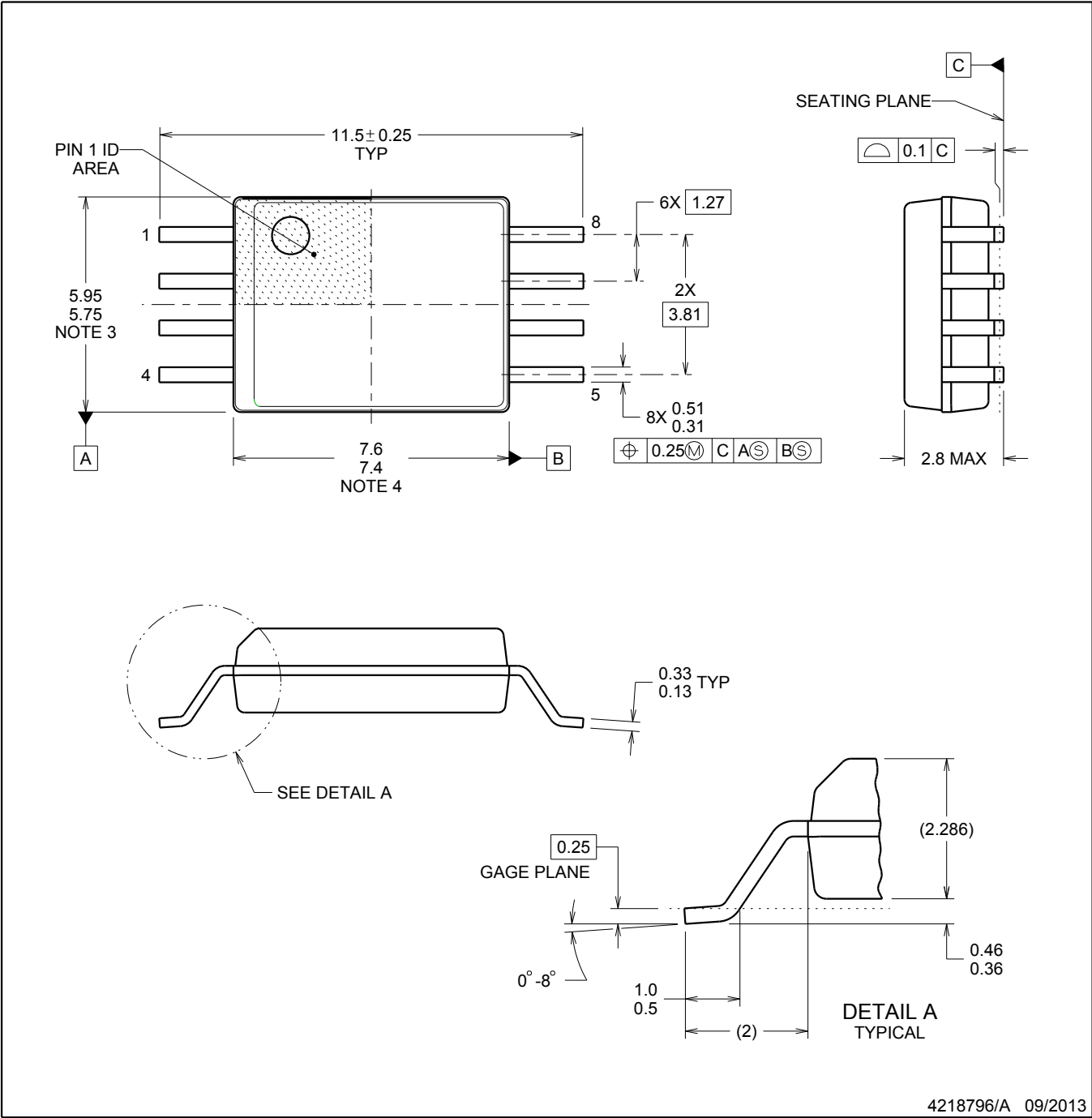
PACKAGE OUTLINE

DWV0008A



SOIC - 2.8 mm max height

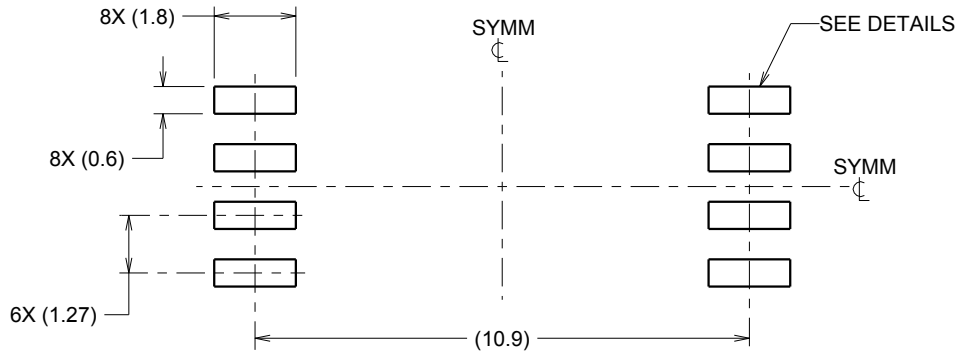
SOIC



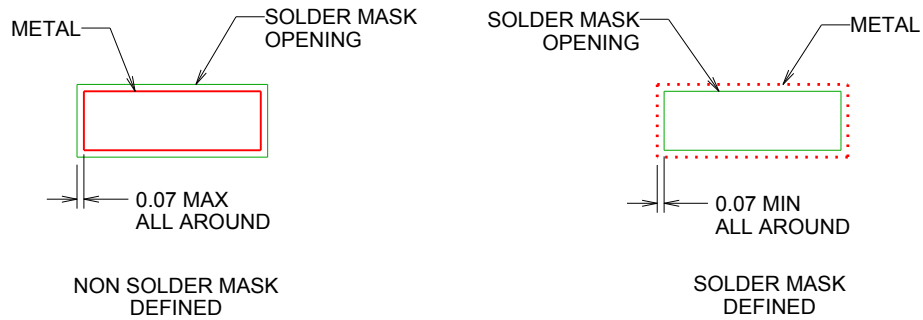
4218796/A 09/2013

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

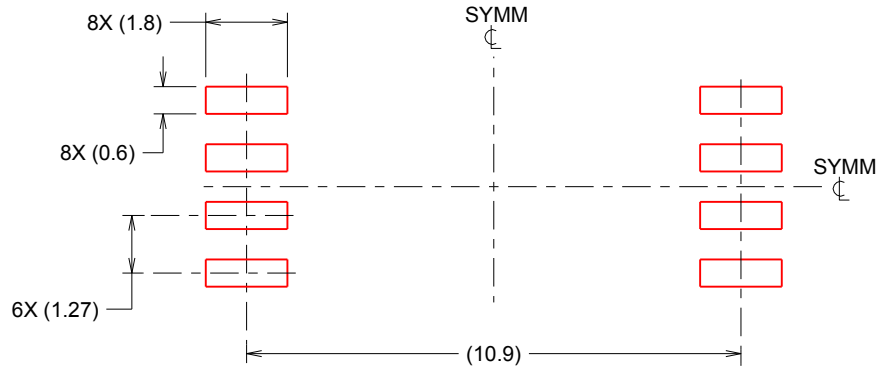


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:6X

4218796/A 09/2013

NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

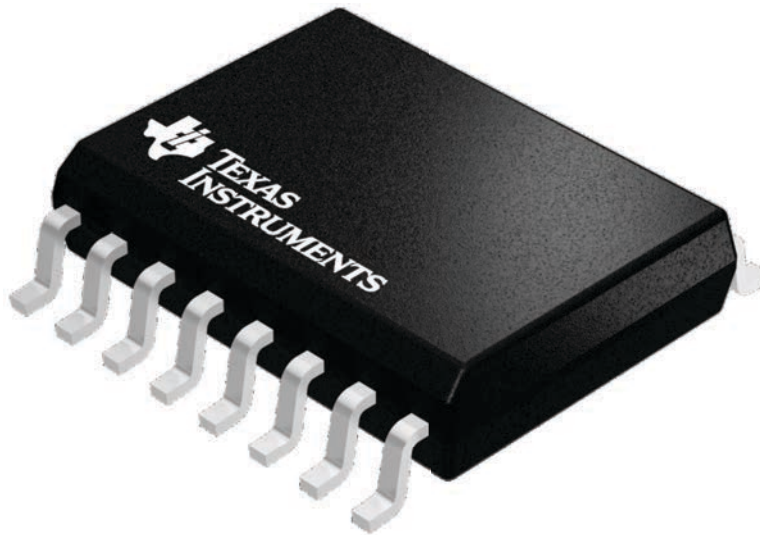
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

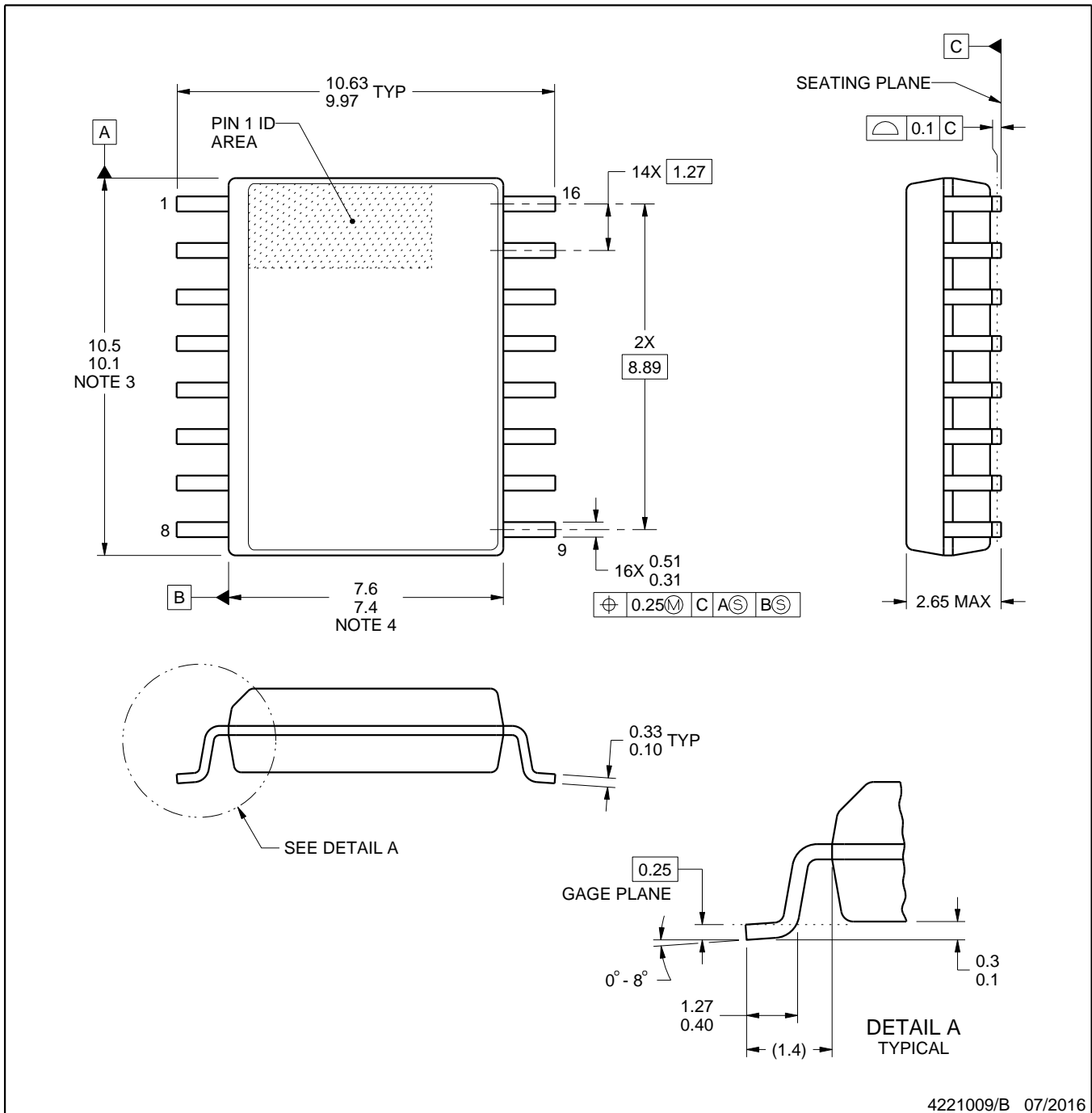


DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

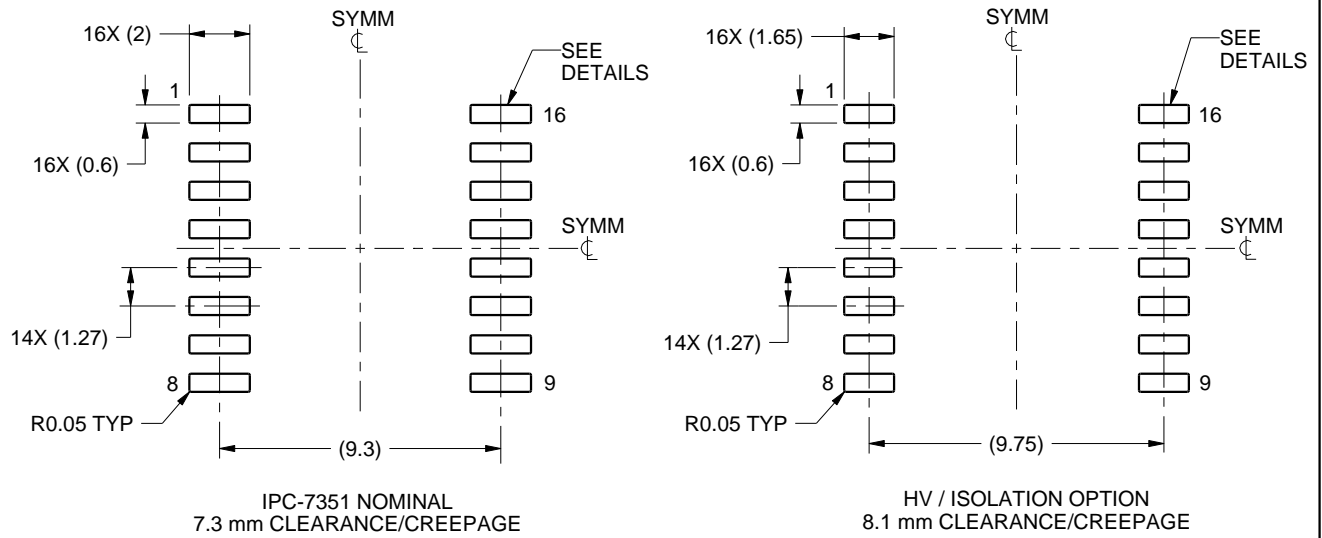
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

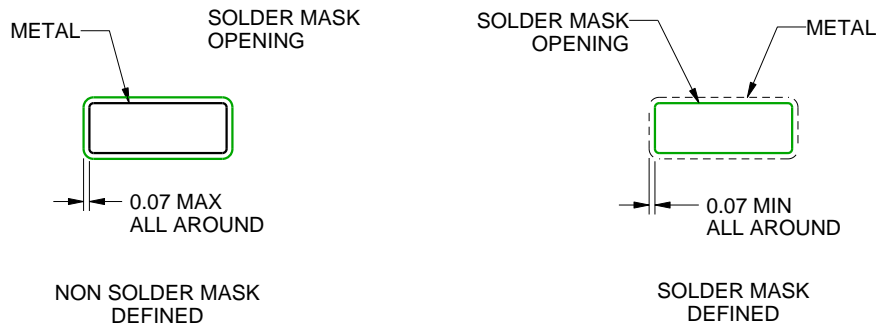
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

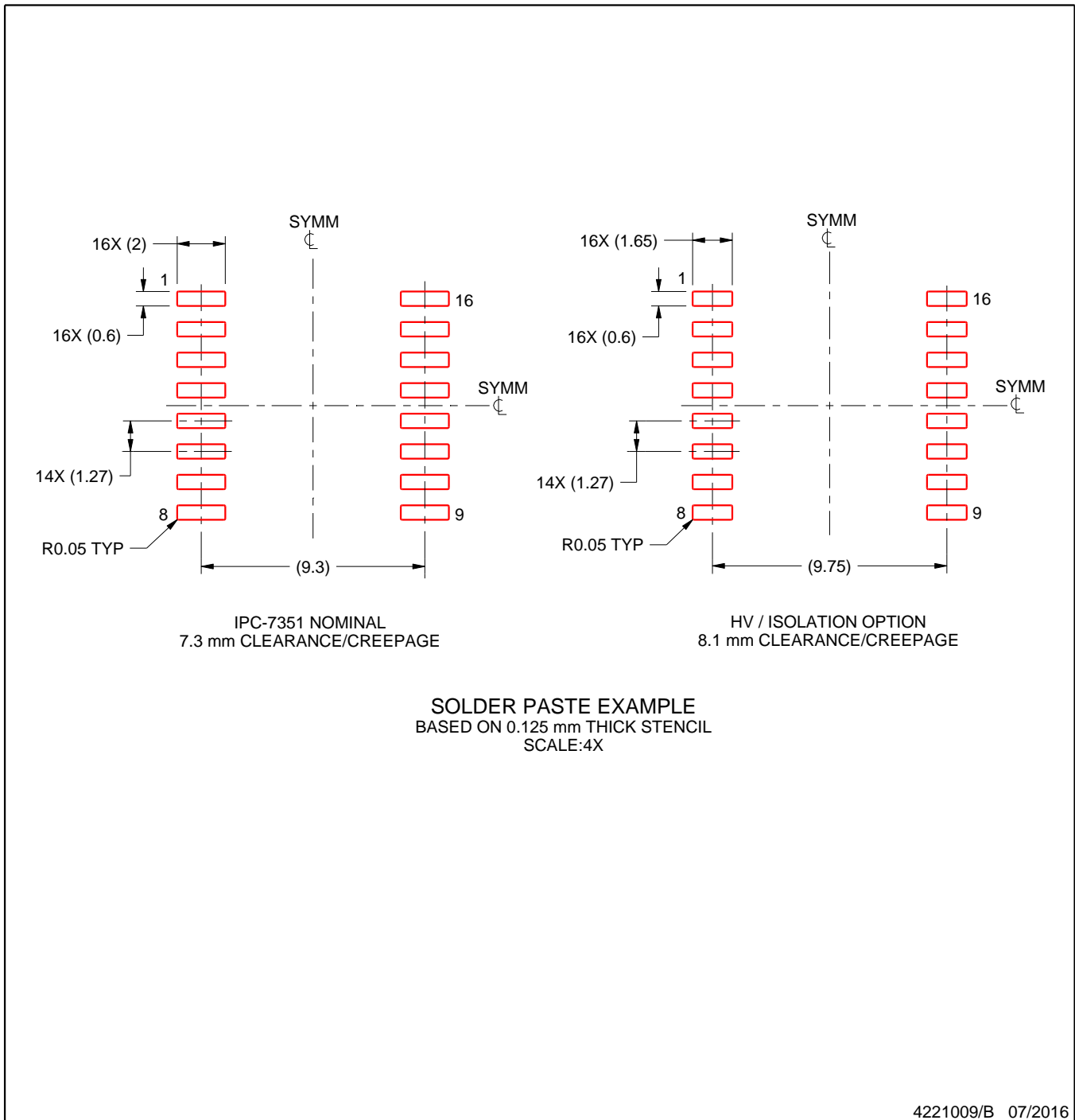
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated